# Ongoing Developments of Future Payload Data Processing Platforms at ESA

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## INTRODUCTION

Data compression is a key technology for many types of space missions. Compression algorithms can be implemented in hardware, software, or a combination of both. For software or combined hardware-software implementation the availability of powerful on-board processors is a key requirement. In the recent past, the data volumes produced by all types of space missions have increased significantly, creating an urgent need for more performant data processing platforms. Although the performance of available processors has increased, in many cases the improvements in performance were not adequate to fully satisfy the application's processing requirements, and developers are forced to invest in expensive dedicated ASICs and programmable hardware. In order to address this situation, ESA is actively supporting the development of high performance payload data processing systems based on existing and future Space ASIC platforms and programmable devices. In this paper, we present the current status and the available options for the development of next generation data processing platforms.
First, the expected needs for processing power on future missions are presented. Then, ongoing and planned ESA development activities for future performant payload data processors are introduced. We present the expected system performances and key characteristics of various development routes, and discuss the envisaged development schedule and relevant constraints.

## DATA PROCESSING AND COMPRESSION ON PAYLOAD PROCESSORS

For Earth Observation and Science missions the data downlink to the ground is traditionally the bottle neck in the system design. This becomes even more severe for the new higher resolution instruments so that data processing and/or data compression becomes mandatory. Often it is not the image produced by the instrument but certain information contained in the image which is of interest, for example

- When using SAR data for naval surveillance, the interesting information is only the position and heading of the ships in the observed area.
- For wild fire surveillance the information of interest is the existence and the location of wild fires.

In such cases the amount of information to be extracted from remote sensing data is usually many orders of magnitude smaller than the remote sensing data themselves. In order to make on-board information extraction attractive, on-board real-time processing is necessary, which often requires very high computational power.

On the other hand, Data Compression of multi/hyperspectral images has recently received a lot of attention. New sensors are generating increasing amounts of data, especially in the spectral dimension, as scenes are imaged at a very fine wavelength resolution. This is particularly useful in terms of potential applications, as spectral features allow extracting important information from the data. However, it also makes the size of the acquired images extremely big. Since many sensors, especially spaceborne ones, cannot store all the data but need to transmit them to a ground station, there is a problem of reducing the data size in order to download all the acquired data.
Image compression techniques can be employed to mitigate this problem, allowing the transmission of more scenes in the same amount of time. Several types of compression are possible. In lossless compression, the reconstructed image is identical to the original. In near-lossless compression, the maximum absolute difference between the reconstructed and original image does not exceed a user-defined value. In lossy compression, the reconstructed image is as similar as possible to the original "on average", i.e., typically in mean-squared error sense, given a target bit-rate.

The RICE algorithm has been standardized by CCSDS 121.0-B-1 [1] as Lossless Data Compression method for space applications. It corresponds basically to an entropy encoder, following a DPCM based de-correlator. This algorithm is

available in software but has also been implemented in hardware by Saab Ericsson, in the PRDC ASIC (Packetising Rice Data Compression). In the area of Wavelet based image compression the CCSDS working group on data compression published a new standard on Image Data Compression CCSDS 122.0-B-1 [2]. This standard defines an image compression algorithm based on a discrete wavelet transform and subsequent bit plane coding. The algorithm can be configured to work in lossless mode and in different levels of lossy compression mode and offers a solution for a large number of applications. A radiation tolerant ASIC implementation of the CCSDS Image Data Compression is currently under development. The PRDC ASIC and the CCSDS Image Data Compression ASIC have a throughput of 20 and 60 Msample/sec, respectively. Even though these devices can cover a wide range of applications, the new generation of high resolution instruments (with data rates in the order of Gbit/sec) very often require dedicated high performance data processing platforms in order to meet the requirements.

## ONBOARD DATA PROCESSING PERFORMANCE NEEDS OF FUTURE PAYLOADS

The data processing requirements of future missions strongly depend on the mission objectives. The following mission categories provide the key drivers for future payload processor performances:

Planetary Science and Astronomy Missions beyond Earth Orbit

This category of missions is characterized by very limited telemetry bandwidths and restricted availability of electrical power due to large distances of the spacecraft orbit from the Sun and Earth. Typical required processing power is in the range of some 10 to some 100 MIPS / MFLOPS on different types of missions ranging from planetary exploration vehicles like the ExoMars rover [3] and orbiters to astronomical observatories such as EUCLID [4] or PLATO [5] which are being studied in ESA's Directorate for Science and Robotic Exploration (SRE). A key driver imposed by those missions is a very low power consumption of only few Watts per GOPS / GFLOPS.

Earth observation missions

For Earth Observation (EO) missions, both available power and telemetry bandwidth are high, typically in the range of some 10 to few 100 Watts, and Mbit/sec to few 100 Mbit/sec, respectively. Therefore these missions have the highest demand for processing power, and will consume all processing power made available by technology for data processing, data reduction and compression. Typical application types demand both fixed-point and floating point processing capability, with some flexibility for choosing between these types. Expected processing power demands for candidate payloads have been analyzed in a recent study [6] and are summarized in the following table:

Table 1. Estimated peak sensor data rates and processing power requirements for future EO payloads

| Candidate payload | peak sensor data rate | peak processing power |
|---|---|---|
| MTG IR sounder | ca 2.2 Gbit/sec | ca 10 GOPS,<br>mixed fixed & floating point operations |
| High Resolution Wide Swath SAR | ca 500 Gbit/sec | ca 1000 GOPS<br>mainly fixed point operations |

In addition to driving the processing power requirements, these missions also drive the requirements for communication interfaces such as High Speed Serial Links (HSSL) that can provide data rates of several Gbit/sec.

Communication payloads

Communication payloads are typically designed for processing very high bandwidth signals. A particular challenge is the flexibility to adapt the payload functionality to evolving and future coding and compression standards, which may in the future be addressed by new technologies such as reconfigurable processors. However, the required payload lifetime (typically of the order of 15 years) and the required extremely high reliability for providing the needed quality of service are major challenges for the introduction of new technologies. Typical performance requirements for a future reconfigurable processor chip providing the flexibility to adapt to evolving communication standards are processing performances of at least several GOPS, several Gbit/sec of streaming data throughput, and power consumption of few Watts. The required processing power is mostly restricted to fixed-point operations. ESA has supported a study for using such a processor (High Performance Data processor, or HPDP) for EO payload data processing [6].

## ONGOING AND PLANNED ESA PAYLOAD PROCESSOR DEVELOPMENT ACTIVITIES

In order to address the hardware needs of both near- and mid-term future missions - within the given constraints of technology and available funding - ESA is actively supporting different lines of technology developments which are summarized in the following paragraphs.

Next Generation Space Digital Signal Processor Systems

The existing space qualified European Digital Signal Processor (DSP), which was derived from the ADI 21020, is not able to meet today's performance requirements. ESA is therefore studying the potential and possibilities of migrating the IP of a state-of-the-art commercial DSP to a performant space qualified ASIC platform [7]. One of the significant advantages of this approach is the possibility to re-use the commercial Software Development Environment (SDE). This is enabled by the foreseen transparency of design modifications to preserve full compatibility with commercial development tools. The key characteristics and expected system performances are summarized in Table 2.

Table 2. Key characteristics of Next Generation Space Digital Signal Processor

| | |
|---|---|
| Performance goal | 1 GFLOP or higher on target ASIC platform |
| Radiation performance | ca 100 Krad (Si), no SEL, design hardened against SEE |
| Power envelope | < 10 Watts |
| Communication | High speed serial links, space standard communication interfaces |
| Software | Re-use of commercial DSP SDE |
| Target ASIC technology | rad-hard 65 nm (under development with STM ), established ATMEL 180nm |

Systems using Massively Parallel Processors

In industry there is a growing trend towards the design of systems on chip that include multiple (often heterogeneous) processors, Network on Chip (NoC), memory elements, and other architectural elements such as specialized co-processors. Computers for space applications are expected to follow that trend with some delay. In addition to very high processor performances, massively parallel processors can provide on-chip redundancy which can be achieved by re-mapping applications to the available pool of processor cores and other redundant architectural elements. The corresponding system properties and achievable performances are currently studied in the framework of a breadboarding activity [8], which aims at achieving the following key performances.

Table 3. Key requirements for Massively Parallel Processor Breadboarding Study

| | |
|---|---|
| Platform | FPGA |
| Performance goal | 1 GFLOP or higher on target ASIC platforms |
| Scalability | Highly scalable (~linear with number of cores) |
| Power envelope | < 10 Watts on target ASIC technology |
| Communication and I/F | Space standard communication interfaces, SDE interfaces, ADC and DAC I/F |
| Software | Commercial SDE, programmability in high level language (C) and assembly code |
| Target ASIC technology | rad-hard 65 nm (under development with STM ), established ATMEL 180nm, or DARE+ 90nm |

As a follow-up of the MPPB activity, a similar processor / NoC design may be part of a test vehicle chip produced for the characterization and validation of the DARE+ (Design Against Radiation Effects) library which aims at the manufacturing of space qualified radiation hard / radiation tolerant chips based on commercial foundry processes [9,10].

COTS based computer for space applications

At any time, scientists and engineers envisage and study applications having processing power requirements that are difficult or impossible to fulfill with space qualified hardware. However, often the required performances are achievable with commercial components due to the typical performance lag of ca 5 - 15 years between commercial state-of-the-art processors and space qualified counterparts. For such cases, the qualification of commercial processor chips for use in space and the design of dedicated software and hardware that allows identifying and correcting radiation-induced errors is a development option that can enable missions that would not be feasible with space qualified components. ESA is therefore supporting a line of developments that establishes the requirements and methods for design, qualification and reliability assessment of COTS Based Computers (CBCs). Furthermore, based on a study phase for high performance COTS based computers [11] a number of demonstrators will be developed via industry contracts.

These demonstrators will prove the validity of the development methods and the performances of the COTS based computers and bring the technology readiness (TRL, [12]) to a level that allows the adoption of the technology for space projects. Some key aspects of the envisaged system are summarized in Table 4.

Table 4. High Performance COTS based computer key requirements

| *High-Performance CBC* | |
|---|---|
| Performance | > 500 MIPS/MFLOPS in high performance mode, > 70 MIPS/MFLOPS in low performance mode available to application software. Expected: ≥ 1 GFLOPS |
| Reliability | > 0.8 over lifetime, recovery from transient errors in < 10 sec |
| Power | < 25 Watt in high performance mode, < 15 Watt in low performance mode |
| Lifetime | 15 years, with 1000 days of high performance mode operation |
| Other | >3 high speed I/F, >3 low speed I/F bus interface, > 144 MB memory |

It is important to note that COTS based computers cannot be seen as a substitute for computers based on space qualified components. However, they are expected to be able to cover the needs of some mission types that have moderate radiation dose requirements as well as high processing power needs. In ESA's technology roadmap they are also needed to bridge the performance gap between outdated existing and more performant future space qualified DSPs.

## DEVELOPMENT CONSTRAINTS

For the development of the envisaged components and technologies the main constraints are availability of funding and time required to complete a successful development. This chapter summarizes the situation as of autumn 2010.

Development schedule

The described activities are performed in parallel. Developments that may lead to a space-qualified chip development based on new ASIC technologies like the ST Microelectronics 65nm technology [13], or the DARE technology [9,10] are scheduled (as far as feasible) to be ready in time for provision of a validated IP design for a test vehicle, which might result in an early component availability in case both the design and the ASIC process are sufficiently mature. For these activities the development of the rad-hard ASIC technology is on the critical path, and availability of first components will not be possible before the 2014–2016 timeframe. For the development of COTS based computers, typical users are expected among the M-class mission projects studied in ESA's science & robotic Exploration department D-SRE [4,5]. For those missions, the demonstrators need to be available before the start of phase C & D around 2014. The parallel schedules of all these activities are illustrated in Figure 1.

For reconfigurable processors aiming at telecom applications a prototyping phase is expected to start in 2011. The results of the activity are expected for 2012/2013.

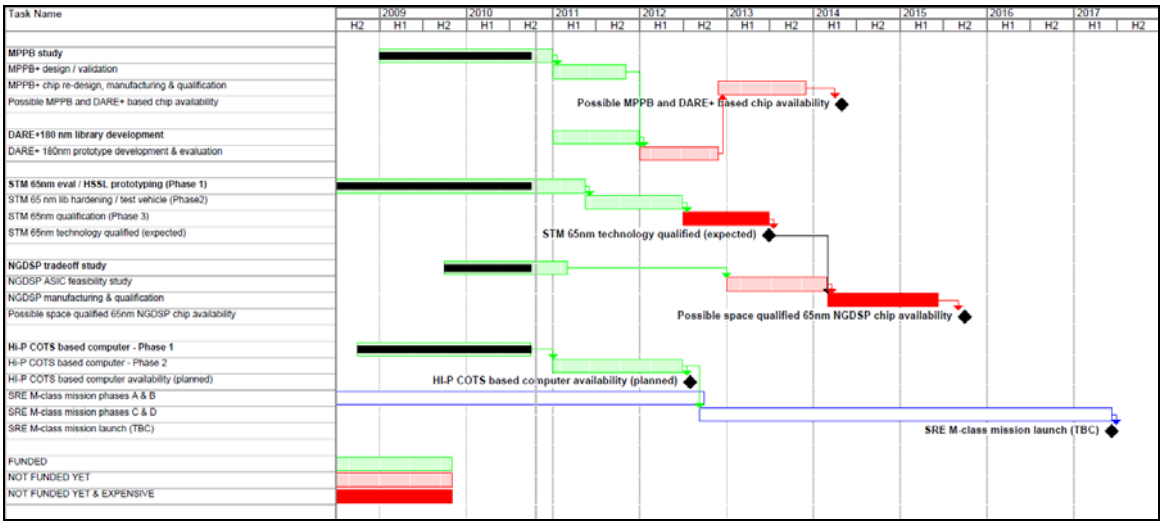


Fig. 1. Schedule for NGDSP, MPPB, CBC and ASIC platform development vs. SRE M-class mission schedule

Funding constraints

For all of the technologies under development the availability of sufficient funds is an essential pre-requisite. The ongoing NGDSP tradeoff study [7] and MPPB breadboard development [8] are being performed with funds from ESA's TRP program. However, funding sources for subsequent steps such as a DSM feasibility study for NGDSP have not yet been identified. In particular the final steps of design, manufacturing and qualification of a space qualified chip require substantial funding for their implementation. The DARE+ prototyping phase which may include an MPPB derived architecture is funded by the ESA's D-SRE Core Technology Program (CTP). The development of a COTS based payload computer demonstrator is based on the feasibility study completed recently [11] and is expected to be confirmed based on national funds (GSTP). The HPDP prototyping phase aiming at high performance chips for the telecom market (not shown in Fig. 1) will be funded by the Greece's Industry Incentive Scheme.

## CONCLUSIONS

The availability of high performance payload data processing platforms is an important pre-requisite for future space payloads and related applications. Onboard data pre-processing and data compression are among the key technologies required to reduce the sensor data volumes sufficiently to be compatible with available downlink bandwidths. High processing performances ranging from hundreds of MIPS/MFLOPS up to thousands of MIPS/MFLOPS in both fixed point and floating point operations are among the key requirements for future processing platforms.

ESA is supporting several parallel lines of technology development with different target applications (Science & Exploration, Earth Observation, and Telecommunications) and utilization timeframes (COTS based computers for near-term missions, NGDSP or Massively Parallel Processors for mid- and long-term utilization). Long-term planning and coherent development of underlying technologies (such as rad-hard / rad-tolerant chip manufacturing technologies) and high performance chip designs (like MPPB, NGDSP, and HPDP) are essential for successful product development.

Next-generation high performance data processing systems and components are among the key elements required for achieving European competitiveness and technology independence in both commercial and scientific areas. The development line for which funding is allocated today are COTS based computers, with an expected TRL of 5-6 in 2012. Technology development plans for other data processing platforms are in place, and will be implemented if the required funding can be made available.

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