ESA'S ROADMAP FOR NEXT GENERATION PAYLOAD DATA PROCESSORS

R. Trautner[(1)]

[(1)] *TEC-EDP, ESA/ESTEC, Keplerlaan 1, 2200AG Noordwijk, The Netherlands*
Email: Roland.Trautner@esa.int

ABSTRACT

A new generation of space borne payload data processors is needed in order to cope with increasing payload data rates and data volumes. ESA has defined a roadmap for the development of future payload processors. A range of technologies are under development and will become available in the coming years. In this paper, we present the key requirements for future onboard payload processors. ESA's development roadmap is introduced. Related ongoing and approved development activities are briefly discussed, and some of their specific characteristics are presented.

1. INTRODUCTION

The on-board processing of payload data from space missions is a demanding task for spacecraft data systems. Data rates and data volumes produced by payloads continue to increase, while the available downlink bandwidth to ground stations is comparatively stable. This results in challenging requirements for future on-board payload data processing systems which cannot be met with space qualified processors available today. ESA's development roadmap aims at the maturization of the required technologies within the given set of constraints such as technology availability and feasibility, budget and schedule. In order to save cost, re-use proven concepts and to support user friendliness the spin-in of commercial technologies is a key element in all development routes. In the following chapters, we first address the requirements from future missions. We then present the established development roadmap that addresses the identified needs. Finally we introduce a number of related development activities.

2. ONBOARD PAYLOAD DATA PROCESSING REQUIREMENTS

The requirements that drive the development of future processing platforms are derived from expected future applications and from expectations of data system developers.

2.1 Next Generation Space DSP Requirements

At the ADCSS workshop held at ESTEC in October 2007 a set of requirements for a new space qualified Digital Signal Processor (DSP) component has been compiled in collaboration with representatives from industry. The resulting requirements, which are recorded and discussed in more detail in a published synthesis document [1], can be summarized as follows:

- Processing power ≥1000 MIPS/MFLOPs
- No access restrictions for European users
- Radiation hardness, > 100krad TID
- High Quality SW Development Environment
- Protected memories (EDAC)
- Support of space standard interfaces
- High reliability, low power consumption

Although these requirements were compiled for a new DSP component, the are generally applicable to next generation payload data processing systems as well.

2.2 Future Science Mission Requirements

Science and Robotic Exploration (SRE) missions are characterized by very limited telemetry bandwidths and restricted availability of electrical power due to large distances of the spacecraft orbit from the Sun and Earth. Typical mission types include planetary exploration missions using vehicles like the ExoMars rover [2] and planetary orbiters, as well as future astronomical observatories such as EUCLID [3] or PLATO [4] which are being studied in ESA's Directorate for Science and Robotic Exploration. Key drivers imposed by those missions are very low mass and minimized power consumption. Table 1 provides some typical performance requirements.

Typical required processing power	Some 10 to some 100 MIPS / MFLOPS
Specific electrical power consumption	Few Watts per 1000 MIPS / MFLOPS

Table 1. SRE Mission Key Requirements

2.3 Future Earth Observation Missions

For Earth Observation (EO) missions, the sensor data rates are often very high. Therefore these missions have the highest performance needs for data processing, data reduction and compression. Typical application types demand both fixed-point and floating point processing capability, with some flexibility for

choosing between these types. Expected processing power needs for candidate payloads have been analyzed in an ESA study (On-Board Data Processor for Optical & Microwave Missions Study, ESA Contract 3-12191, 2008) and can be summarized as follows:

Candidate Payload	MTG IR sounder
Peak sensor data rate	ca 2.2 Gbit/sec
Peak processing power	ca 10 GOPS, mixed fixed & floating point operations
Candidate Payload	High Resolution Wide Swath SAR
Peak sensor data rate	ca 500 Gbit/sec
Peak processing power	ca 1000 GOPS, mainly fixed point data processing

Table 2. EO Candidate Payload Key Requirements

2.4 Telecommunication Missions

Typical requirements for telecom missions include the processing of very high bandwidth signals, and the desire for flexibility allowing an adaptation of the payload functionality to evolving and future coding and compression standards. Further specific needs are the required payload lifetime (typically of the order of 15 years) and the required extremely high reliability for providing the needed Quality of Service (QoS). Typical performance requirements include at least several GOPS (mainly fixed point processing), several Gbit/sec of streaming data throughput, and power consumption not higher than a few Watts.

3. ESA's DEVELOPMENT ROADMAP

In order to address the identified needs, ESA is conducting R&D activities along three parallel main development routes:

[A] Hardening of COTS processors against radiation effects on board / software level

This development option relies on the use of commercial components in order to exploit their superior processing performance. The sensitivity to Single Event Effects (SEE) is mitigated by dedicated hardware and software. High reliability components are preferred, and candidate processors need to be compatible with the radiation requirements. This option offers comparatively short development time and moderate development cost. The recurrent cost is relatively high due to the extra (partially rad-hard) hardware and software needed for error mitigation. The achievable performances in areas such as low mass and power, reliability, and total dose tolerance are lower than those achievable with dedicated space qualified chips that may be developed in routes [B] and [C].

[B] Hardening of a proven COTS processor architecture by using a space qualified ASIC platform and transparent design modifications

This development route for a powerful space processor was used successfully for the now outdated TSC21020 DSP. Transparent design hardening allows the re-use of the high quality commercial SDE. This approach requires a high initial investment in IP licensing, chip level hardening and manufacturing / qualification. However, once the chip is available it allows the development of reliable high performance low mass data processing systems at low recurrent cost. The re-use of the commercial SDE will support very efficient and low cost application development.

[C] Development of a multi-core DSP / massively parallel IP based processor

In the commercial world, multi-core processors are becoming mainstream, and it is expected that space will follow this trend. A combination of powerful processor cores, Network on Chip (NoC) technologies, and on-chip memory elements can lead to processor architectures that are scalable, internally redundant, and very performant. This approach is expected to require a relatively high initial investment similar to (but lower than) option [B]. Recurrent cost of systems based on a massively parallel processor chip is expected to be low. The comparatively complex application development and less sophisticated SDE (as compared to [B]) would result in moderate application development cost.

4. COMPARISON AND BENCHMARKING

A key parameter for the development of next generation processing platforms is the achievable performance of the resulting systems in future application cases. The selection of processor and other components, IP cores, and system architectures as well as associated software development tools needs to be supported by a suitable set of benchmarks that mimic realistic space applications. For this purpose ESA has compiled a set of benchmarks [5] that allows comparing the performance of various, often very different, data processing systems in a range of application cases.

In order to maximize the re-use of benchmark elements in future applications and for avoiding the waste of development resources the specified benchmarks draw most of their elements from the kernel benchmark and application benchmark categories.

They include the following benchmark types:

- I/O performance (throughput of CCSDS packets)
- Analogue data acquisition, filtering / processing (FIR, FFT) and output
- Image data compression (CCSDS lossy & lossless) and packaging (CCSDS packets)
- Optical sensor data (FIR) filtering / decimation and compression (CCSDS RICE algorithm)
- Microwave sensor data IQ demodulation and decimation

The benchmark specification requires that the software shall be programmed in a high level language. The use of assembly code subroutines is allowed if they are provided as part of the SDE libraries. The use of such subroutines needs to be indicated and pointed out in the benchmark result documentation. In order to respect the inherent strengths of different platforms, the algorithms can be implemented in either fixed-point format, floating point format, or both. The implemented data format needs to be clearly specified and documented for all benchmarks.

The benchmark specification is publicly available via ESA's On-board Data Processing website [6]. It is applied in an increasing number of ESA contracts and third-party activities.

5. ONGOING DEVELOPMENTS

The following paragraphs summarize the ongoing development activities, and their relation to the identified development routes.

5.1 High Performance COTS Based Computer

This activity addresses development route [A] as part of a broader development effort that includes the development of highly reliable (Hi-R), highly available (Hi-V) and high performance (Hi-P) COTS based computers. The Hi-P development will be based on COTS DSP chips, with radiation mitigation techniques implemented in a combination of hardware and software.

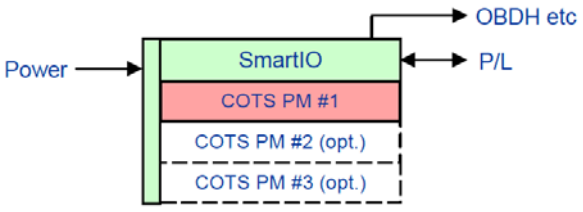

Figure 1. Hi-P CBC modular architecture

A key element of this activity, which will be performed by Astrium France, is an architecture that combines a high reliability control element ("SmartIO") with a scalable number of COTS processing modules (PMs), supporting the tailoring of reliability, performance and application latency according to the user and application requirements. The Hi-P system architecture is shown in Fig. 1, while a candidate architecture for the processing module is depicted in Fig. 2.

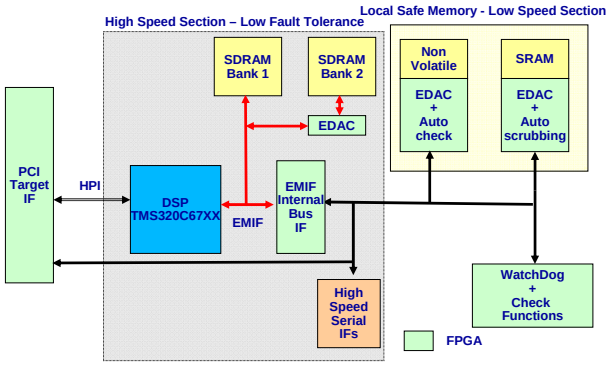

Figure 2. Hi-P PM candidate architecture

Sensitive elements of the PM architecture are planned to be implemented in rad-hard FPGA or ASIC technology, and support data verification as well as monitoring of the COTS processor. Due to the modular design the processing modules in use may be based on COTS DSP, General Purpose Processor (GPP), or FPGA technology according to user needs.
The first part of this development activity has been completed in 2010 (High Performance COTS based Computer for Payload Systems, ESA contract 1-5658, 2008). Part 2, which is aiming at the development of a TRL 5+ demonstrator system, is expected to start in 2011 and finish in 2013. A set of ESA defined performance benchmarks [5] will be implemented, which will allow direct comparisons with performances of other platforms.

5.2 High Processing Power Digital Signal Processor

This activity also addresses development route [A] but with a different technical baseline, and with a specific set of requirements derived from studies of future science missions ([3],[4], and others). Low mass and very low power consumption are among the driving design requirements. The development is performed by Astrium UK (High Processing Performance Digital Signal Processor, ESA Contract 1-6182, 2009), and aims at the development of a TRL 4 breadboard and the implementation of demonstration software including ESA's NGDSP benchmarks [5]. The activity is expected to be completed by 2012.

5.3 European Digital Signal Processor Tradeoff and Definition Study

This study (ESA contract 1-6026, 2009), which follows development route [B], is performed by Astrium UK and aims at the identification of the most promising DSP IP for a possible following migration step to a space qualified ASIC platform. The migration includes removal of IP parts that are not required for space, introduction of SEE mitigation technologies like EDACs or triplication etc. for internal memories and other elements and the addition of space standard interfaces such as SpaceWire (SpW) or SpaceFibre (SpF). A key requirement is to maximize the transparency of modifications to the Software Development Environment (SDE) in order to avoid incompatibilities between commercial chips (which would be used in early hardware and software development phases) and the space qualified version. The following DSPs are assessed:

- Analog Devices ADSP-21469
- ATMEL Diopsis 940HF
- Texas Instruments TMS320C6727B

While the first two DSPs are the main candidates for IP licensing, IP modification and subsequent space qualified ASIC development, the 3rd DSP is a good candidate for COTS based computer developments. Existing ASIC technologies from ATMEL (180nm) as well as the new 65nm technology under development (ST Microelectronics) are considered. The results of this activity, which include the observed performance data on ESA's benchmarks [5] extrapolated to the target ASIC technologies, will be available by mid 2011. However, no funding source has so far been identified for the development of a NGDSP ASIC.

5.4 Massively Parallel Processor Breadboarding Study

This breadboarding and development activity (Massively Parallel Processor Breadboarding Study, ESA contract 21986, 2008) follows development route [C] and is conducted by RECORE b.v. (NL). It is aiming at the development of a NoC based system that combines multiple DSP cores with a LEON2 controller. It includes a set of space standard interfaces and features such as SpW including RMAP protocol support, CCSDS timers, ADC / DAC interfaces, and on-chip as well as off-chip memories. The basic architecture of the developed system is depicted in Fig. 3. All elements requiring high bandwidth connectivity are connected on the 32-bit wide NoC. The Xentium™ DSP cores support up to 4 MACs per clock cycle. The system has been developed on an FPGA platform.

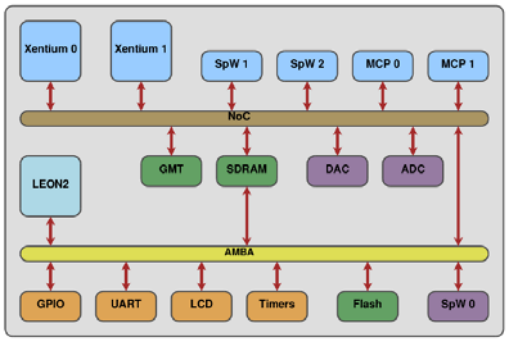

Figure 3. MPPB architecture

The study output will include performance data for the NGDSP benchmarks [5], and first results are expected for mid 2011 [7]. The next development step, which aims at hardening the DSP, NoC and bridge IPs and the manufacturing of a rad-hard prototype chip, may be implemented as part of an ASIC technology development activity in the 2011-2013 timeframe.

5.5 High Performance Data Processor Prototyping and Performance Assessment

This activity has started in 2011 and is performed by ISD (Greece) and Astrium Germany [8],[9]. Following development route [C] it aims at the development of a processor prototype that is based on scalable reconfigurable fixed point processing array technology from PACT. Fig. 4 shows the basic architecture of the envisaged prototype chip.

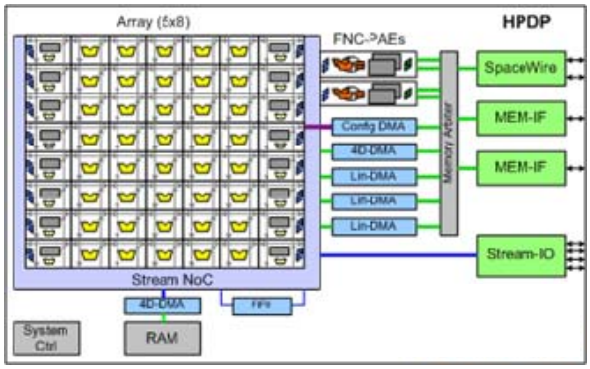

Figure 4. HPDP prototype chip architecture

In this architecture, a large reconfigurable processing core capable of processing high bandwidth data streams is supported by a number of additional processing elements, DMAs, memory and stream I/O interfaces, etc. The chip design is aiming mainly at telecom applications. A set of test applications (various DVB-S processing steps such as encoders/decoders, PSK modulators/demodulators, simple FFT and filter routines) will be demonstrated. Results from this activity are expected around 2013.

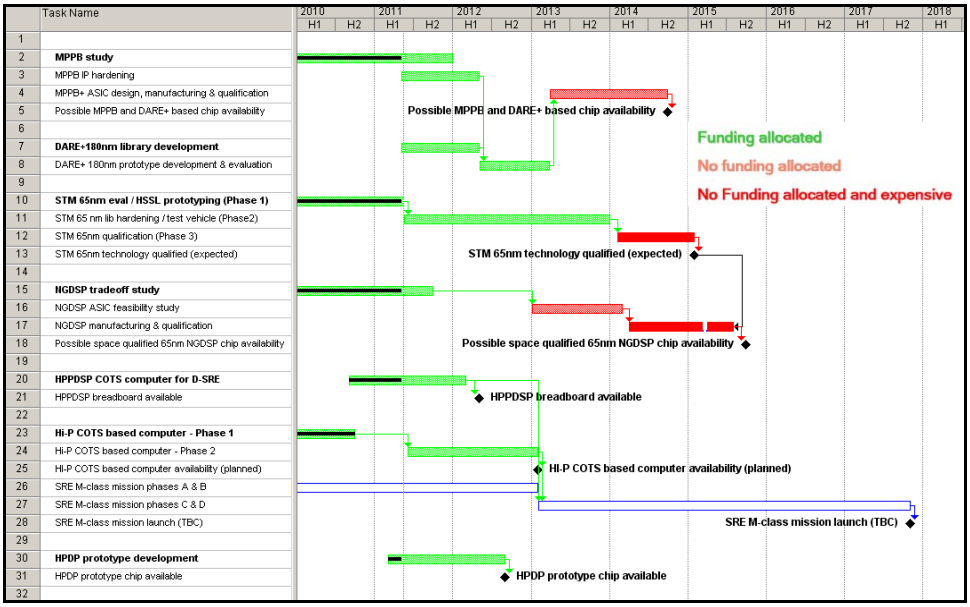

Figure 5. Preliminary mid-term schedule for ESA's payload data processor related developments

6. ROADMAP SCHEDULE

The implementation schedule for the activities introduced in chapter 4 is continually adjusted according to development progress and availability of required funding, and needs to be adapted according to the availability of underlying technologies (space qualified ASIC manufacturing) or availability of suitably qualified processors for COTS based computer developments. Figure 5, which shows the preliminary mid-term schedule for some key activities, must therefore be interpreted as a snapshot taken in early 2011 which will evolve in the future. It is evident that for chip developments that are targeting the STM 65nm process or IMEC's DARE 180nm technology, all schedules hinge on the readiness of these technologies. An important constraint for the completion of COTS based computer developments is the start of the C/D phase for the M-class missions designed in ESA's D-SRE. The funding situation for the proposed developments is illustrated by the color codes, showing that – apart from COTS based computer development activities – funding and/or technology gaps still exist for all proposed chip developments.

7. CONCLUSIONS

Many new missions and applications in the areas of Science and Exploration, Earth Observation and Telecom will require new, more powerful on-board processing platforms. Based on requirements derived from mission studies and discussions with industrial stakeholders, ESA has conceived a roadmap relying on three main development routes: COTS based computers, hardening of licensed mainstream commercial DSP IP, and development / maturization of novel commercial NoC based / highly parallel scalable processor IP. Within the given funding constraints, several R&D activities are conducted, which are expected to lead to the availability of COTS based computer hardware at TRL 5+ and hardened scalable processor IP by 2013. The design of a new generation of European space qualified processor chips (based on IP developed in routes [B] or [C]) may follow but will not start before 2013. The availability of such components mainly depends on the provision of funding and can not be expected before the 2015/2016 timeframe.

8. REFERENCES

1. *Next Generation Processor for On-board Payload Data Processing application – ESA Round Table Synthesis*, TEC-EDP/2007.35/RT, 2007.
2. Hult T. et al, *The ExoMars Rover Vehicle OBC*, proceedings of DASIA 2010 Conference, 2010.
3. *EUCLID M-class mission*, http://sci.esa.int/euclid.
4. *PLATO M-class mission*, http://sci.esa.int/plato.
5. *Next Generation Space Digital Signal Processor Software Benchmark*, TEC-EDP/2008.18/RT, 2008. The document is available via [6].
6. ESA On-board Data Processing Website, http://www.esa.int/TEC/OBDP/
7. K. Walters et al., *Multicore SoC for On-board Payload Signal Processing*, Adaptive Hardware and Systems Conference, San Diego, USA, 2011.
8. M. Syed, *High Performance Data Processor*, Adaptive Hardware and Systems Conference, Noordwijk, The Netherlands, 2008.
9. C. Papadas, *Prototyping the HPDP Chip on STM 65nm Process*, DASIA, Malta, 2011.