Avionics Architectures and Components for Planetary Entry Probe Payloads and Systems

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ABSTRACT

Like all complex spacecraft, planetary entry probes require reliable, performant and resource-efficient avionics to successfully fulfil their mission. Due to specific mission constraints and targets, high integration as well as power and mass efficiency are particularly important.
The Data Systems Division / Electrical Engineering Department of ESA's Directorate for Technical and Quality Management [1] has been actively involved in development of avionics architectures, networks, interfaces, and hardware as well as software and IP core components for a variety of mission types and applications. An important focus of the work was – and continues to be – standardization of interfaces, protocols and algorithms in order to facilitate re-use and compatibility of individual building blocks.

An overview of the ongoing developments on avionics architectures is presented. State of the art network and processing node types and their elements with strong relevance for planetary probe avionics are introduced. New types of interfaces and components under development as well as related technologies are presented. The ESA IP core service is introduced and explained, and the relevance of ongoing and planned developments in the avionics area for planetary entry probes and their systems and payloads is discussed.

1.0 DRIVERS FOR AVIONICS TECHNOLOGY DEVELOPMENT

The development of new avionics technologies is driven by the needs of all areas of space applications. The key drivers can be summarized as follows:

- Increasing data rates: in space science and earth observation, more data generally means more science. Higher sampling rate, higher dynamic range, more spectral and spatial resolution, more channels and more auxiliary data enable scientific results of higher quality.
- More demand for on-board processing power: with growing data rates and data volumes, and physical and technological constraints for the available telemetry bandwidth, data reduction, compression and on-board pre-processing becomes more important.
- Low power consumption: many spacecraft operate in an environment where the availability of electrical power is very limited, and the cost of power in terms of spacecraft mass is very high. Therefore low power consumption is essential.
- Low mass: miniaturization of spacecraft systems is often an enabling factor for demanding space missions. This is also true for avionics elements, where miniaturization often goes hand in hand with a reduction of power consumption which allows achieving further mass savings.
- Low cost: an important factor for reducing avionics systems cost is the standardization of interfaces and building blocks which allows savings due to the re-use of avionics elements. The reduction of mass and power consumption allows savings in other spacecraft system areas (power systems, structural mass, etc.) that may add up and allow significant overall cost savings.

The impact of a significant miniaturization of avionics systems has been studied in the framework of a System on a Chip (SoC) study for a Jupiter Entry Probe (JEP). The effect of replacing traditional avionics elements by a SoC has been analyzed, and the impact on avionics mass, power, volume, operability, complexity, risk and cost of the probe has been studied. The study concluded that the estimated 5 kg saving in avionics mass would lead to a further 15 kg saving on other subsystems (power, structure, batteries, …) and lead to a smaller and lighter probe without a significant risk increase. Furthermore, a saving of 4% on the phase B/C/D cost was estimated, clearly showing the potential of avionics miniaturization for the design and development of challenging space missions.

It is therefore the combination of the requirements coming from current and future missions, and the expected benefits of further miniaturization and standardization, that define the strategies for avionics technology development.

2.0 ESA's STRATEGY & REFERENCE AVIONICS ARCHITECTURE

ESA's strategy for supporting European avionics & payload component developments comprises a number of interrelated efforts. One of the central activities is the development of Application Specific Standard Products (ASSP) that are capable of answering many on-board computing and control needs for present and future applications, such as microprocessors, TM/TC handling components, circuits supporting data acquisition and processing, and related IP development. For these ASSP / ASIC developments, new technology developments such as multi project wafer manufacturing etc are employed to reduce development time and recurring cost. For new components the seamless integration into ESA supported network and bus topologies is a core requirement.

In the ESA reference avionics architecture, the interconnection of avionics elements and their components is achieved by a hierarchical concept that identifies different network and bus types providing specific services and data transfer rates.
The currently existing top layer high speed network connectivity is provided by the SpaceWire (SpW) network as shown in Fig. 1. The MIL1553 bus is an established standard for the low data rate bus system. Another efficient low data rate technology is provided by the Controller Area Network (CAN) bus as an alternative for non-safety critical applications. At the lowest layer of the hierarchy, which is foreseen for hardware diagnostics and debugging, no specific interface or network standard has been developed; instead, the use of industry standard interfaces such as JTAG is encouraged. For very high data rate connections and networks a fiberoptic link (SpaceFibre, SpFi) is being developed, which will provide even higher bandwidths beyond those provided by SpaceWire.

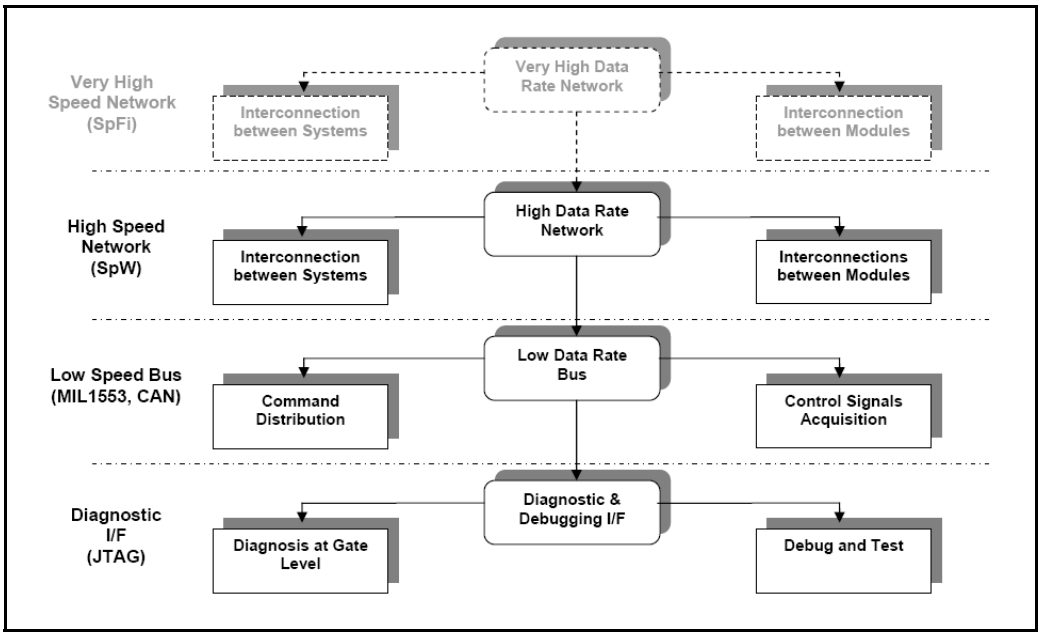

Figure 1. Avionics network and bus hierarchy

The SpaceWire network standard and the CAN bus are supported by an increasing number of avionics elements and components. Their basic characteristics are introduced in the following sections.

3.0 ONBOARD NETWORK TYPES AND COMPONENTS

3.1 MIL-STD-1553-B

The MIL-STD-1553-B bus is used as a system platform bus on many space missions. It supports data rates up to 1 Mbit/sec and is extremely robust with respect to interference due to the high voltage levels and transformer coupling. This comes at the price of high power consumption and high harness mass. A low power and low mass alternative in particular for interplanetary missions is the CAN bus.

3.2 CAN

The Controller Area Network (CAN) bus originates from automotive industry and has been used in space applications for over a decade. The simple 2-wire interface allows low mass bus topologies, and the 1 Mbit/sec maximum data rate is sufficient for many low to medium bandwidth applications. Rad-hard bus interface components such as the ATMEL AT 7908E are available off-the-shelf, and many modern space electronics components provide built-in CAN bus interfaces. ESA has supported the development of IP cores for CAN and the integration of those cores in a range of rad-hard standard components. The ESA CAN bus IP ("HurriCANe") is also available via the ESA IP core service.

3.3 SpaceWire

The SpaceWire (SpW) interface is now a well-established standard interface for high datarate on-board networks. Its key features can be summarized as follows:

- Data rate up to 400 Mbps (200 Mbps typical)
- 9-pin Micro-miniature D-type connector, link cable length up to 10m (point-to-point)
- LVDS signalling, +/-350 mV typical, fault isolation properties
- 100 Ohm termination, power typically 50 mW per driver –receiver pair
- Established ECSS standard
- Simple, small IP (5-7 k logic gates)
- Supports simple P2P connections or complex networks via routers
- Supports time distribution with few μsec resolution
- supports Remote Memory Access Protocol (RMAP) data transfer

SpW interfaces are incorporated in a growing number of space electronics components. ESA is supporting developments by managing standardization, provision of IP cores via the IP core service, and by supporting the development of SpW test and development equipment that is necessary for efficient network design, implementation and AIT.

3.3.1 SpaceWire Router

Complex SpW-based on-board networks need router chips for the interconnection of multiple nodes. Rad-hard chips are available from several manufacturers. ESA has supported the development of a router chip which provides 8 full duplex SpW links supporting data rates of up to 200 Mbps. The following table summarizes the key features of this router chip.

Table 1. SpW router characteristics

Type	ATMEL AT910E
Links	10 full duplex links (8 serial), 2-200 Mbps
Package	196 pin ceramic MQFP
Radiation hardness	300 krad, latch-up immune to 80 MeV/mg/cm2
Hardware features	External time-code and status signals 2 external parallel ports 1 internal configuration port (routing table, priority scheme, status and configuration registers), Time code distribution and management
Routing	Wormhole routing (low memory need) Group adaptive routing (link failure management)
Standard	Compliant to ECSS-E50-12A

The detailed description of the router's functionality and specifications can be found in the standards document [2] and the user manual [3].

4.0 NETWORK NODE COMPONENTS

In this chapter, we present some new avionics electronic components that allow avionics elements to connect to standardized onboard networks. The listed devices are just some examples for a growing number of components that are available for the development of avionics elements.

4.1 Scalable Multi-channel Communication Subsystem for SpW

The Scalable Multi-channel Communication subsystems for SpW (SMCS) [4,5], allow to connect one or more SpW links to various electronics elements such as ADC/DAC, RAM, FIFO, GPIO, and UARTS. It provides a simple way to implement a SpW interface for existing avionics modules (DPUs, mass memories, etc) and allows them to become nodes in state of the art onboard networks. The following table summarizes the characteristics of the SMCS chips.

Table 2. SMCS characteristics

Type	ATMEL AT7912E / AT7911E
Links	1 / 3 full duplex SpW link, up to 200 Mbps
Package	100/196 pin MQFP package
Radiation hardness	50 krad, latch-up immune to 80 MeV/mg/cm2 SEU hardened design
Hardware features	5V and 3.3V operation 0.7/1.7W at 5V, 0.15/0.4W at 3.3 V Supports serial universal protocol (STUP)

4.2 Remote Terminal Controller

The Remote Terminal Controller (RTC) [6] is a versatile and highly flexible chip with a broad application range. The incorporated SPARC compliant LEON2 CPU with 64 Kbytes of on-chip RAM provides a high level of processing power; the SpW links support RMAP (Remote Access Memory Protocol, a SpW protocol that allows remote memory access via SpW links) which can eliminate the need for external memories in some RTC applications. The provision of built-in ADC/DAC, GPIO, UART, memory and CAN bus interfaces greatly simplifies system development and allows implementing avionics elements such as instrument controllers etc with a small number of components.

The RTC is based on IP cores from different sources, including ESA, and is available as a rad-hard standard product. Figure 2 shows the basic architecture of the chip.

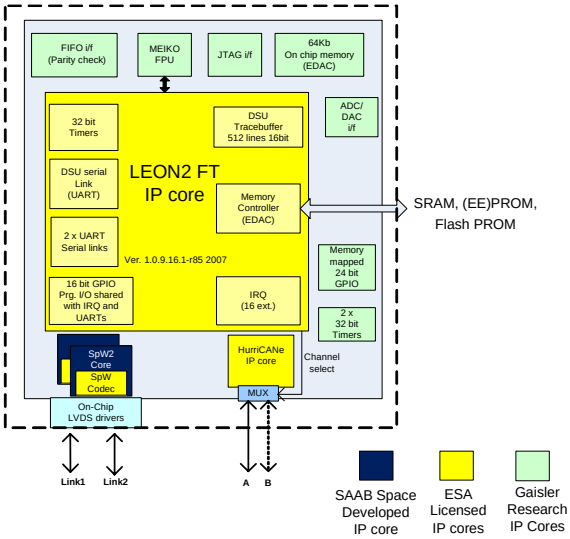

Figure 2. RTC architecture

The characteristics of the RTC are summarized in the following table.

Table 3. RTC characteristics

Type	ATMEL AT7913E
CPU core	LEON2, 35 MIPS / 2.5 MFLOPS, SPARC V8 compliant, floating point unit, 64 Kbtes on-chip RAM
Links	2 full duplex SpW links, up to 200 Mbps, RMAP compliant 2 CAN bus interfaces
Package	349 pin MCGA package
Radiation hardness	100 krad, latch-up immune to 80 MeV/mg/cm2 SEU hardened design
Hardware features	3.3V+1.8V supply 0.6W power consumption ADC/DAC, SRAM, EEPROM, FIFO, GPIO, UART interfaces

4.3 Microprocessor I/O interfaces

While the incorporation of SpW and CAN interfaces on new avionics components is a high priority requirement for new ESA developments, it is important to also provide interfaces to systems and chips that have been designed as a standalone component. The SMCS is one possibility to provide a reliable SpW interface for microprocessors. For processor chips that support a PCI (Peripheral Component Interconnect) interface, like the new LEON2 (ATMEL AT697F) processor, the GR701A interface chip is available as an FPGA-based solution that provides not only SpW but also CAN, 1553, I/O ports, UARTs, and multiple other interfaces.

These components, together with IP cores available from ESA and from industrial sources, provide a range of technological possibilities for the implementation of high performance onboard network interfaces for heritage avionics elements.

5.0 ONGOING AND FUTURE DEVELOPMENTS

ESA is supporting a range of developments in the areas of avionics architectures, components, and onboard networks. Many of these developments are based on currently available design elements, architectural concepts, and standards. Attention is paid to the re-use of IP, standards compliance, backwards compatibility where it seems beneficial, and utilization of state-of-the-art manufacturing technologies.
In the following paragraphs, some developments are presented that seem most relevant for planetary probes and scientific spacecraft. For a more comprehensive list of ESA supported activities please refer to the TEC web pages [1].

5.1 SpW related Developments

Based on the existing standards, protocols and devices the ongoing work on SpW aims at finalizing the standardization (RMAP protocol), and study / prototyping activities for new application areas like SpW-IP tunnelling and SpW real-time services and protocols.
The SpW-IP tunnel is a technology supporting the transparent transmission of SpW packets via IP protocol, which allows connecting SpW nodes located at different places via the internet in a fully transparent way. It is expected that this technology will simplify interface testing and verification activities for SpW nodes, and allow time and costing savings in spacecraft AIT.
The provision of real-time services on SpW networks is another area of great interest for spacecraft avionics; this area is studied at the moment, and protocols and standards may be developed in the near future.

5.2 SpaceFibre

In order to cope with future high on-board bandwidth needs, a fibre-optic link called SpaceFibre (SpFi) is being developed by ESA in cooperation with a number of other space agencies. The objectives and key performance characteristics are

- 1-10 Gbps data rate, 100m cable length, few g/m cable mass
- galvanic isolation (not provided by SpW)
- Copper version for small distances
- Transmission of a scalable number of SpW links over SpFi
- Compliance to SpW protocols and routing mechanisms

A SpW/SpFi demonstrator is already available, providing a data rate of > 2 Gbps. Work on definition and standardization is ongoing; standard documents and commercial hardware are expected to be available after 2010.

5.3 Spacecraft Controller on a Chip

It has been shown that the miniaturization of avionics components can help to achieve significant savings in terms on spacecraft mass and power, and also allow savings on development cost for space missions. The Spacecraft Controller on a Chip (SCOC3) is being developed in view of these expected advantages. It is based on IP from various industrial and ESA sources.

The SCOC3 key specifications are

- LEON3-FT with FPU providing ~80 MIPS
- Dual AMBA=AHB bus architecture
- CCSDS TM/TC interfaces
- OBDH interfaces: 1553, SpW, CAN, UART
- CCSDS time management, housekeeping TM packetizer
- Power management, debug facilities
- Target technology ATMEL ATC18RHA, BGA472 package

The development of this chip is ongoing and a rad-hard chip may be available in the next decade.

5.4 Next Generation Space DSP

Digital signal processing has become a central element of onboard data processing, in particular for payload data. After the highly successful development of the 21020 DSP a new generation with significantly higher performance and state-of-the-art interfaces and Software Development Environment (SDE) is required. The key requirements are

- 1 GFLOP minimum performance
- Radiation hardened design, small footprint, low power
- Easy interfacing to standard DSP system components (ADC/DAC, memories, onboard networks, DSP arrays)
- High quality software development environment
- Availability as a space qualified standard component

The pre-development activities for this chip are planned for the 2008-2009 timeframe. Development and qualification are envisaged for the 2010-2012 timeframe, with a planned availability of the chip after 2013.

5.5 Next Generation Multipurpose Processor

Current rad-hard, highly reliable microprocessors for space applications such as the LEON2 provide processing power in the order of 100 MIPS. For applications that require more performant processors a new generation of processors is needed. ESA's key requirements are

- 400 MIPS minimum
- Standard product implemented in 90 nm or 65 nm silicon technology
- SPARC compliant multi-core architecture
- MMU, debug support unit, large on-chip memory (16-32 B)
- Standardized interfaces like 1553, SpW, CAN and RS422
- Interface to co-processors and companion chips

A preliminary study (GINA) has been completed; the definition of the final architecture still needs to be done. Development and qualification of the chip is expected for the 2008-2012 timeframe, with a planned availability of the chip after 2013.

6.0 ESA'S IP CORE SERVICE

ESA/ESTEC maintains and distributes under ESA licenses a small catalogue of IP Cores [7] which comprise typical digital functions used in space applications (TMTC, EDAC, SpaceWire, CAN, LEON2-FT, OBDH, etc). ESA/ESTEC provides this service to ESA member states as an attempt to:

- counteract obsolescence and discontinuity of existing space standard ASICs, thus helping to guarantee the availability of some key functions in a technology independent format
- reduce costs of large IC developments (e.g. Systems-on-Chip) by re-using already designed and validated IC functions
- promote and consolidate the use of standardized functions, protocols and/or architectures (e.g. SpaceWire, CAN, TMTC, etc)
- centralize IP users' feedback to improve quality of existing IPs and identify future needs

These IP cores were developed in the scope of European Space Agency (ESA) activities, ranging from in-house developments to contractor work and from simple Field Programmable Gate Arrays (FPGA) to complex System-On-a-Chip (SOC) devices. The IP cores provided by ESA are "soft-cores", i.e. technology independent. They can be synthesized and targeted to any ASIC or FPGA technology.
The ESA VHDL IP cores can be licensed for space research and/or commercial use, under specific conditions (depending on the IP ownership) to companies based in ESA member and participant states. Companies and institutions outside the ESA member states may utilize the technologies via contracts with companies that are based in member states, provided that the conditions associated with the ESA license are respected.

7.0 AVIONICS FOR PLANETARY ENTRY PROBES

In addition to the general aspects of spacecraft avionics systems there are some specific ones that are of particular relevance for planetary entry probes. In many cases, these vehicles are sent to targets that present a very challenging mission environment in terms of temperature, radiation, availability of energy and required autonomy. Distances to earth, and required delta v for the launch and cruise vehicles, are often very large. Therefore the following aspects are even more important for entry probes than for conventional spacecraft:

- Avionics mass: a notable reduction of avionics mass usually leads to significant savings in probe mass, fuel mass and therefore launch mass
- Power consumption: entry probes often run on batteries for extended periods of time during a cruise phase preceding the entry phase. A reduction in avionics power consumption therefore often leads to savings in battery mass and volume that may lead to an additional size and mass reduction of vehicle structures
- Avionics size: planetary probes are usually highly integrated vehicles where volume is a scarce resource. Furthermore, the often very demanding radiation environment may require shielding of critical components or even complete systems. A reduction in avionics size not only reduces volume requirements with associated potential probe structure mass savings, it can also significantly reduce the mass required for radiation shielding. Finally, small size is also advantageous for the thermal conditioning of onboard systems.
- Autonomous operation: long communication delays due to significant spacecraft-earth distances create the need for on-board autonomy, coupled with high reliability. Systems providing these features often have increased needs in terms of on-board computing resources in comparison to less autonomous systems.

All these aspects can be addressed at the same time by investing in the integration and further miniaturization of avionics components. Reduction in size naturally leads to savings in mass on electronics, boxes, harness, and shielding. The utilization of deep sub-micron manufacturing technologies for semiconductors usually goes hand in hand with reductions in power consumption, but also provides the option of higher processing power. Savings on power lead to further mass savings on power generation, storage and conditioning systems.
It is this clear advantage of electronic systems integration and miniaturization that will make elements such as systems on a chip and versatile processing elements like the RTC excellent candidates for future probe system developments. In combination with reliable, low mass onboard networks and buses such as CAN and SpW these will be the building blocks for future highly integrated systems that will enable cost-efficient missions to many exciting destinations.

8.0 SUMMARY

ESA is actively supporting the development of avionics architectures and elements through the definition, standardization and development of avionics networks and nodes. Onboard networks such as CAN bus and SpaceWire cover many of the needs of modern avionics systems, and a range of components have been developed for the implementation of new avionics elements and for interfacing existing designs to modern networks. The re-use of design elements is promoted through the development of IP cores that are employed in various types of devices. ESA's IP core service makes those IP cores available to companies and contractors in ESA member states.
For satisfying the needs of future applications, ESA is continuing the development and support of existing networks and nodes, and investing in the development of new, higher performance avionics elements such as fibre-based networks, highly integrated data handling systems, and next generation onboard processors. For planetary entry probes, the most relevant trends will be further electronics miniaturization, higher integration and reduction in power consumption.
In addition to the development of avionics nodes and networks, ESA is also investing in the development of support equipment and protocols that simplify the development and AIV/AIT of avionics systems.

This paper addresses only a small subset of the actually supported activities; readers are encouraged to visit the ESA web pages for more comprehensive, detailed and up to date information.

9.0 REFERENCES

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