NGDSP Benchmarking & SDE Evaluation Final Report

European DSP Trade-off and Definition Study (ref. 22645/09/NL/LvH)

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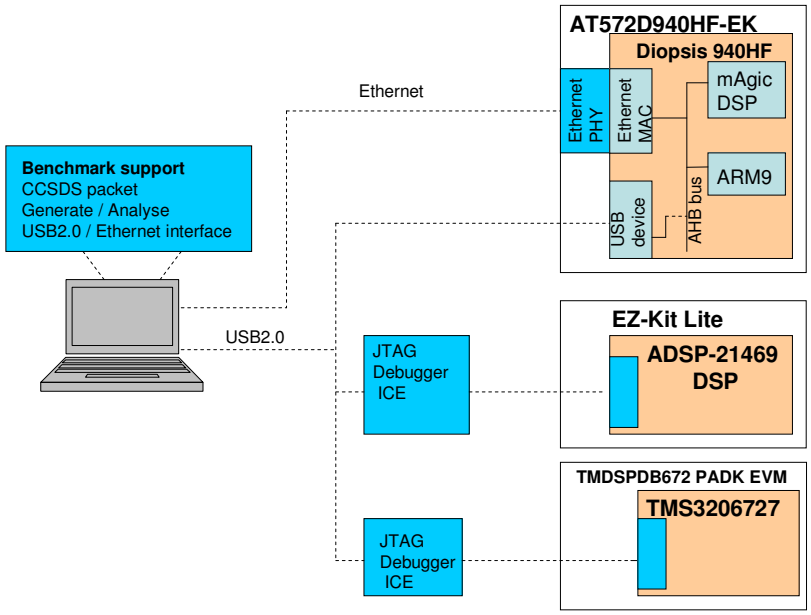
Evaluation of 4 DSPs

- Benchmarking evaluation of initially 3 DSPs
  - Texas Instruments TMS320C6727
  - Analog Devices ADSP-21469
  - Atmel DIOPSIS 940
  - Common benchmarking structure
  - Used manufacturer libraries,
  - or same software on all
- COTS manufacturer evaluation boards
  - TI C6727 – Lyrtech PADK EVM
  - ADSP-21469 EZ-Kit Lite
  - DIOPSIS AT572D940HF-EK board



- Partial software evaluation of Recore MPPB (Xentium)
  - Analysis of provided benchmarks only – some benchmarks missing
  - Two Xentium cores, targeted migration to many-core NoC, performance figures presented as single-core. Fixed-point, not floating-point

Comparison of DSP hardware features

	ADSP-21469	DIOPSIS	TI C6727
Clock Rate (MHz)	400	100	350
Performance	1.6 GFlops	1 GFLops	2.1 GFlops
Feature Size	65nm	130 nm	90 nm
Memory B/W	6.4 GB/s	2 GB/s	5.6 GB/s
Internal memory	625kB,4-bank	Data 80 kB, Program 128 kB	32 kB L1P, 256 kB (P & D)
On-chip functions	FFT & FIR accel., timers, interrupts	Timers, interrupts	Timers, interrupts
External memory	DDR2 DRAM, SRAM, Flash	8 MB SDRAM SRAM, DMA only	128 MB SDRAM, SRAM, Flash
DMA	Stride, chain, ping-pong,scatter/gather	Stride, circular	Stride, circular, 2D & 3D
Core features	Address generation zero-overhead loop	40-bit float, 512 registers	Address generation zero-overhead loop

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Xentium hardware features

	Xentium
Clock Rate (MHz)	50 MHz (FPGA), 200? (STM 65nm)
Performance	200 MMAC per core (Xilinx) x 2 cores
Memory B/W	800 MB/s local, 200 MB/s memory-tile
Internal memory	32 kB data, 8kB L1P cache per core + 256 kB memory-tile per N cores
On-chip functions	Timers, interrupts, LEON2 controller
External memory	2x DDR2 SDRAM, Flash
DMA	Yes. No chain, stride or 2D
Core features	VLIW, 10 units, packed 16-bit ops including MAC, hardware loop, bit-swap for FFT, complex-multipl

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Benchmarks Performed

- Benchmarks – “kernel” and “application”
  - Forward & Return I/O data-rate of CCSDS packetisation
  - FIR filter: 16,64,256 taps (1024 samples)
  - FFT: 1024, 1960, 4096 points
  - Lossless data compression (CCSDS 121.0-B-1)
  - Lossy image compression (CCSDS 122.0-B-1)
  - Onboard processing #1 – filtering, decimation, compress
  - Onboard processing #2 – demodulate, polyphase-decimate
- Measured on COTS evaluation boards
  - Scaled to 65 nm ASIC process
  - Process generation => 30% ↑ F_{MAX} , 30% ↓ Power
  - Except Xentium scaled to F_{MAX} = ADSP, from 50 MHz Xilinx
  - Excludes I/O. Includes “overheads” e.g. fixed-to-float, DMA, LEON / ARM co-processor interaction for DIOPSIS & Xentium

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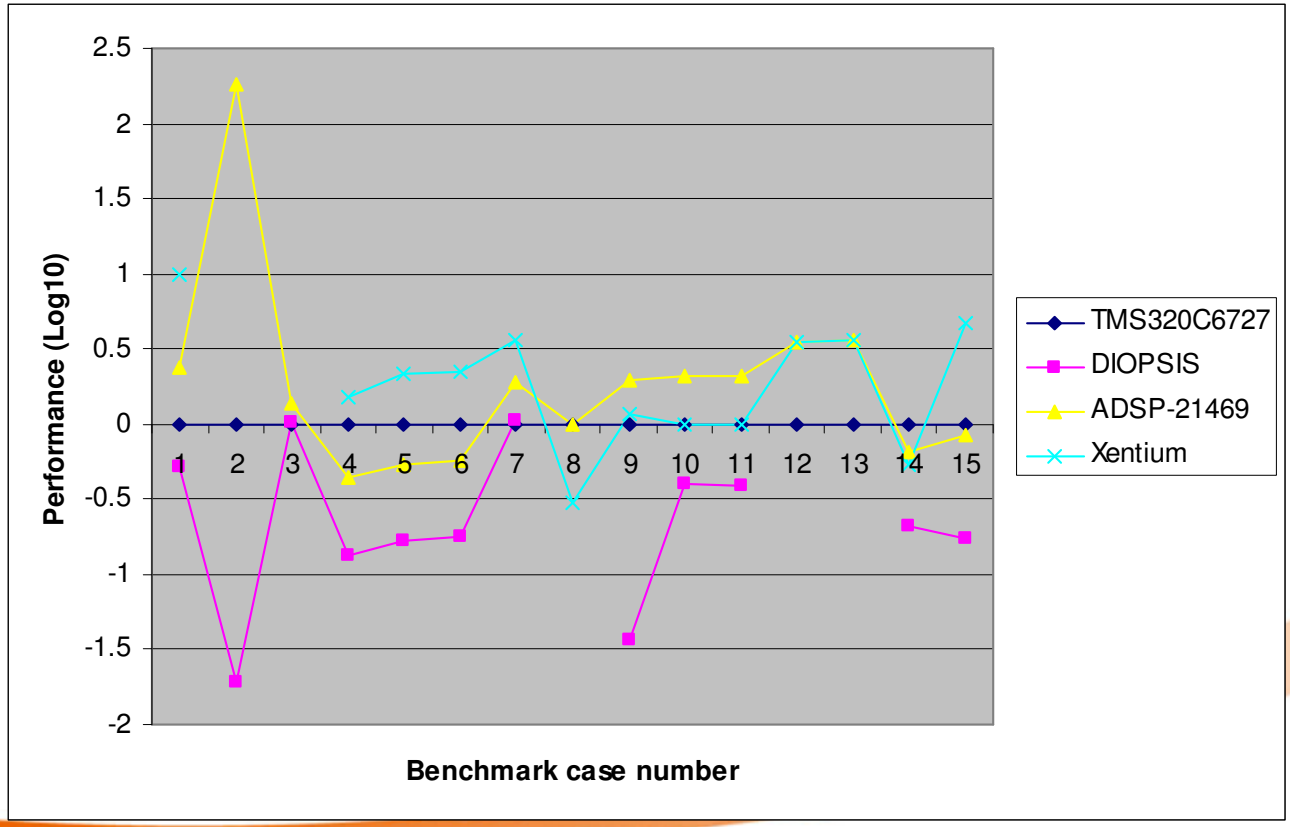
Benchmark Performance graph

- Performance re-based to TMS320C6727 nominal comparison
  - C6727@350 MHz,ADSP-24169 @307 MHz,DIOPSIS940 @130 MHz, Xentium single-core @307 MHz



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Benchmark Performance comments

- I/O Benchmark (0.3 Mpacket/s)
  - DMA moves data from I/O to memory: packet header processing
  - DIOPSIS transfers ARM:DSP using buffer. Latency & payload data
- FIR / FFT benchmarks (~10 MSPS 64-tap FIR, 4096-pt FFT)
  - TI C6727: 1.9 (out of 2) MAC/cycle
  - ADSP21469: SIMD 1.25 (out of 2) MAC/cycle. Optimal complex FFT
  - Xentium: 16-bit int. MAC vs 32-bit float – twice as many MACs per unit
    - FFT 1960-pt and FFT-4096 extrapolated – not efficiently coded
  - DIOPSIS: low clock-rate. Can't use effectively many instruction units
    - Small internal memory & no direct-read external RAM
- Lossless data compression (~1 MSPS)
  - Compiler mapping on complicated code: ADSP-21469 133 cycles per sample, DIOPSIS = 290, TI C6727 =104
  - DIOPSIS also has lower clock frequency

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Benchmark Performance comments

- OBP cases #1 (~2 MSPS) and #2 (~7 MSPS)
  - Similar issues to FIR filters / data compression
  - ADSP-21469, TI C6727, Xentium approach their core efficiency
  - DIOPSIS cannot use most of its core units, and has low clock-rate
  - Also tests compiler efficiency for polyphase FIR filter coded in 'C'
    - Performance ~20% lower than assembly library-code
    - Except DIOPSIS which is 60-80% slower

- Image compression (0.06 Mpixel/s)
  - Legacy code: 1 Mpixel data does not fit in internal memory
  - COTS Performance determined by external RAM rather than core (ADSP-21469 has DDR2, TI 6727 has only SDR SDRAM)
  - DIOPSIS can't direct-read external RAM => full code re-write on legacy code to DMA random-access data-words individually
  - Xentium peak performance is estimated: benchmark S/W performs the bit-encoding on the *LEON* (99% of the processing time)

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Hardware Performance bottlenecks (1)

- Analog Devices ADSP-21469
  - FFT / FIR accelerators offload the core – but are slower
    - For multi-functional code un-typical of space applications
    - Recommend not to port accelerators to space NGDSP
  - Compiler can't SIMD vectorise most applications (half performance)
    - Improve compiler to identify SIMD opportunity
- Texas Instruments TMS320C6727
  - None seen

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DIOPSIS Hardware bottlenecks

- Low clock-frequency (100 MHz)
  - 10 instruction units are rarely used / usable on applications. Target 300 MHz
- Low memory-bandwidth
  - More instruction units need more bandwidth / clock to feed them
- On-chip data RAM too small (80 kB data)
  - Forces applications to external memory. 256 kB is minimum
  - 80 kB data / 128 kB program hard-coded in ISA address-space
- Can't execute program or data from external memory
  - DMA only – random-access requires complex code re-factoring
  - Data is not relocatable – must be decided at SW architecture stage
  - Many applications impractical to implement
  - 40-bit float (only), 32-bit mem-access. Float inaccessible in external memory
- DMA with stride not supported
  - Or rather, only with non-blocking call, with no RTOS to schedule it
- Endian-ness of ARM and mAgic does not match
  - Inefficient data exchange – especially as ARM / LEON mediates I/O

MPPB / Xentium Hardware bottlenecks

- Xentium can be targeted for many-core NGDSP
  - Scaleability is crucial – Network-on-Chip architecture
  - Number of cores for space NGDSP not assessed within Astrium analysis
  - Performance figures include LEON, DMA, NoC
  - Some scaling issues on MPPB configuration.If addressed, linear performance-scaling possible
- Xentium instruction cache-size
  - Xentium 8 kB I-cache should be enlarged to >16 kB (too small for 'C' code)
  - FIR kernels fit, 'C' tight loops do not (e.g. 1960-point FFT, lossless compression)
- LEON stall issues
  - MPPB – LEON barely fast enough to trigger DMA to feed Xentium
  - LEON ISR stalls on I-cache miss. 25% single-core overhead, not scaleable
- DMA Stride capability
  - Needs separate source & destination, for FFT & image-processing
- RAM cacheability
  - Data transfer to LEON in non-LEON cacheable RAM (coherence)
  - Very slow LEON data processing
  - Should be made cacheable – LEON can flush the cache when necessary

Many-core Architecture Recommendations

- Implement one memory-tile per NoC row of Xentium cores
  - Data-flow is routed primarily horizontally
  - Prevent bottleneck on cores access to internal memory
- Implement one HSSL I/O per NoC row
  - Prevent I/O bottleneck to cores
- Implement at least 2 DMA channels per Xentium core
  - LEON is too slow to reconfigure DMA channels dynamically
  - MPPB has total 8 channels, would support up to 4 cores
  - Enlarge DMA controller to scale number of channels with cores

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Power consumption

- COTS board => space process extrapolation
  - Very approximate
- Analog Devices ADSP-21469
  - 0.6-0.8 W measured
  - “Non-arithmetic” processing consumes most power
- Atmel DIOPSIS
  - 0.2 W measured, almost independent of application
  - Since the performance is low, not power-efficient
  - Clock-frequency scaled to same as ADSP-21469, more power
- Texas Instruments TMS320C6727
  - 1.2-1.6 W (power-spreadsheet => worst-case)
  - “Arithmetic” processing consumes most power

SDE features and components

- ADSP-21469 and Texas Instruments C6727
  - Project editor, C/C++ compiler, assembler, linker, script engine,simulator
  - RTOS (VDK or DSP/BIOS respectively) – threads, priority
  - Graphical trace (event-timing)
- MPPB
  - Xentium: Compiler, assembler, simulator (single-core), I/O lib
  - Xentium compiler based on gcc. Stable and functionally correct
  - Eclipse-compliant tool-chain, IDE project-editor available
- Atmel DIOPSIS
  - ARM tool-chain in Windows, mAgic DSP tool-chain in Linux
  - mAgic Command-line compiler, linker, simulator (no project-editor)
  - Separate for ARM and mAgic core (no co-simulation)
  - RTOS is Linux for ARM, DBIOS for mAgic (interrupts,mutexes, no threading)

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SDE Libraries

- ADSP-21469
  - I/O (including printf), time, board support, basic maths
  - Complex arithmetic, FFT (arbitrary size)
  - FIR & IIR filters, matrix operations
  - Auto- and cross-correlation, histograms, inverse sqr-root
- Atmel DIOPSIS
  - ARM has Linux, I/O (including printf), time, board support
  - Limited signal-processing functions:
  - Selected FFT sizes up to 1024, FIR filtering
  - Matrix multiplication & inversion, inverse sqr-root
- Texas Instruments C6727
  - I/O (including printf), board support, basic maths
  - FIR & IIR filters, arbitrary FFT, auto- and cross-correlation (single & double precision)
  - Vector and matrix operations, inverse sqr-root
- MPPB / Xentium
  - Drivers / API for I/O, timers, interrupt / mailbox, DMA engine
  - As delivered: specific-length FIR filters, generic FFT (un-optimised for memory)
  - Plans for digital radio – e.g. Viterbi, modems, filters

Debugging capabilities

- Both ADSP-21469 and Texas Instruments C6727
  - Not Eclipse-compliant editors, but good GUI project environment – hyperlinking, brace-matching, source-code auto-complete / errors
  - On-target debug over JTAG debugger
  - Breakpoints (conditional), single-stepping
  - Memory / variable visibility & setting, simulation & target
  - ADSP21469 has Background Telemetry Channel (BTC)
  - TI C6727 has stack overflow monitoring
- Atmel DIOPSIS
  - ARM – gcc, Eclipse-compliant; mAgic – no editor development support
  - No breakpoint or single-step
  - No co-simulation between ARM and mAgic
  - No memory / variable setting or visibility on target
  - Debug process: Printf (unstable), or use ARM to handshake and report mAgic data
- Xentium
  - Eclipse: good project editor (function hyperlinking, source error highlight, etc)
  - Single-core (only) simulator of Xentium with I/O lib
  - No on-target Xentium breakpoint, single-step or visibility
  - No real-time LEON co-simulation (NoC, DMA not included)

Code optimisation support

- Both ADSP-21469 and TI C6727
  - Compiler provides cycle-counts & hint comments
  - Pragma's for compiler vectorisation hints
  - Statistical profiler to identify code bottlenecks
  - TI C6727 additionally provides "Compiler Consultant"
    - Statistical analysis tool to trade-off speed vs code-size
- Atmel DIOPSIS
  - Compiler cycle-count information (buried), but no hints
  - No statistical profiling
- Xentium
  - No compiler loop cycle-counts or profiler
  - Trace, but excludes memory & bus overheads

SDE issues seen

- ADSP-21469
  - SIMD unused by compiler on most code – not fully used even on library code for single-channel FIR filter. Action to improve compiler recommended
  - Optimisation keyword for data location reduces code portability (non ANSI)
    - Preferably handled by linker or #pragma
  - BTC interface to Visual Basic script not fully supported at time of testing
- TI C6727 (No issues seen)
  - User-friendly development & debug environment

DIOPSIS SDE issues

- Critical
  - Compiler is very unstable – crashes most of the time even on known good code. Very slow (half hour for a few hundred LOC). Requires frequent #pragma code-modification to allow it to compile functions >100 lines
- Major
  - Compiler output uninformative and lengthy Information & Error messages
  - Non-integrated SDE for mAgic and ARM (even different OS)
  - Debug very difficult– no co-simulation, breakpoint or single-step
  - Poor code development environment (no IDE)
  - Poor library performance: simple FIR filter uses less than half the processor
- Acceptable
  - Compiler-specific behaviour between ARM & mAgic does not match
  - Passing data between ARM and mAgic requires the developer to “link by hand” – header-define the address of each variable. No mailbox available

Xentium / MPPB SDE issues

- Strong need for tool for graphical trace
  - To debug timing & event synchronisation on multicore, DMA, NoC
  - Simulation of Xentium does not include NoC, memory, cache
- Compiler performance should be improved
  - Performance penalty ~2-3x on complicated code
- Need for Xentium on-target breakpoint debug
  - Plus single-step / visibility of variables & memory
- Signal processing libraries not mature
  - Scope and Performance of currently provided routines well below achievable hardware performance. Needs development effort

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Performance Conclusions

- Comparison: ADSP-21469 and Atmel DIOPSIS 940
  - ADSP-21469 higher performance by factor ~3x-5x
  - Some applications much slower on DIOPSIS (~50x) or not executable, due to architecture limitations
- Comparison: C6727 and ADSP-21469
  - Benchmark-dependent (~2x factor either way)
- NGDSP memory interface migration
  - SDRAM bandwidth may be critical to overall performance (DDR2 / DDR3) – particularly for highest performance processors

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Performance conclusions (2)

- Comparison: Xentium vs. ADSP-21469
  - Xentium achieves near ADSP-21469 on most applications, better on some
  - Many instruction units used per clock, wide register & memory bandwidth
  - Xentium doubles performance from use of packed 16-bit integer arithmetic, achieving better than ADSP-21469 on those cases
- Xentium system performance
  - To meet the system-level performance on space applications, the design configuration should be upgraded in some simple but key aspects:
  - Xentium I-cache size. LEON I-cache stalling. DMA stride feature. RAM cacheability
- Network on chip approach is a significant advantage
  - Scaleable performance, if the above points are met
  - Predict linear performance with number of cores, up to I/O capability
  - Number of cores feasible on STMicro 65 nm not assessed (inc. memory)

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Conclusions (SDE Quality)

- User-friendliness
  - TI C6727 & ADSP-21469 have user-friendly development & debug environment
  - Both have good signal-processing libraries supporting space industry needs
- Atmel DIOPSIS
  - Too unstable & slow to use.
  - Very user-unfriendly development & debug environment
  - Poor performance of library benchmarks
- ADSP-21469
  - Hand-optimisation of code needed to use SIMD – otherwise performance is halved from peak on arithmetic applications
  - Non-ANSI Program/Data memory linker
- Xentium
  - Good single-core development environment.
  - Recommend to improve development and debug tools for many-core. On-target breakpoint debug and event timing / synchronisation trace tool.
  - Compiler performance adequate, but should be improved to match H/W performance
  - Xentium signal-processing libraries should be developed