R&D Name : NGDSP
European Digital Signal Processing Trade-off and Definition Study

reference number : 22645/09/NL/LvH

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FINAL PRESENTATION – PUBLIC SESSION

ESA – 28 August 2012

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ISD S.A. Integrated Systems Development

ASTRIUM AN EADS COMPANY

Content of the Presentation

- Objectives of the study
- Content & Activities performed
- Results of the SW Evaluation → John Franklin
- Migration study of the ATMEL Diopsis
- Migration study of the ADSP 21469
- Design flow of the Migration
- Ressource and Risk, Schedule
- Conclusion

NGDSP OBJECTIVE OF THE STUDY

Objectives of the study (1/2)

- **3 candidate DSPs identified in the SOW:**
  - Texas Instruments TMS320C6727
  - Analog Devices ADSP-21469
  - ATMEL DIOPSIS 940

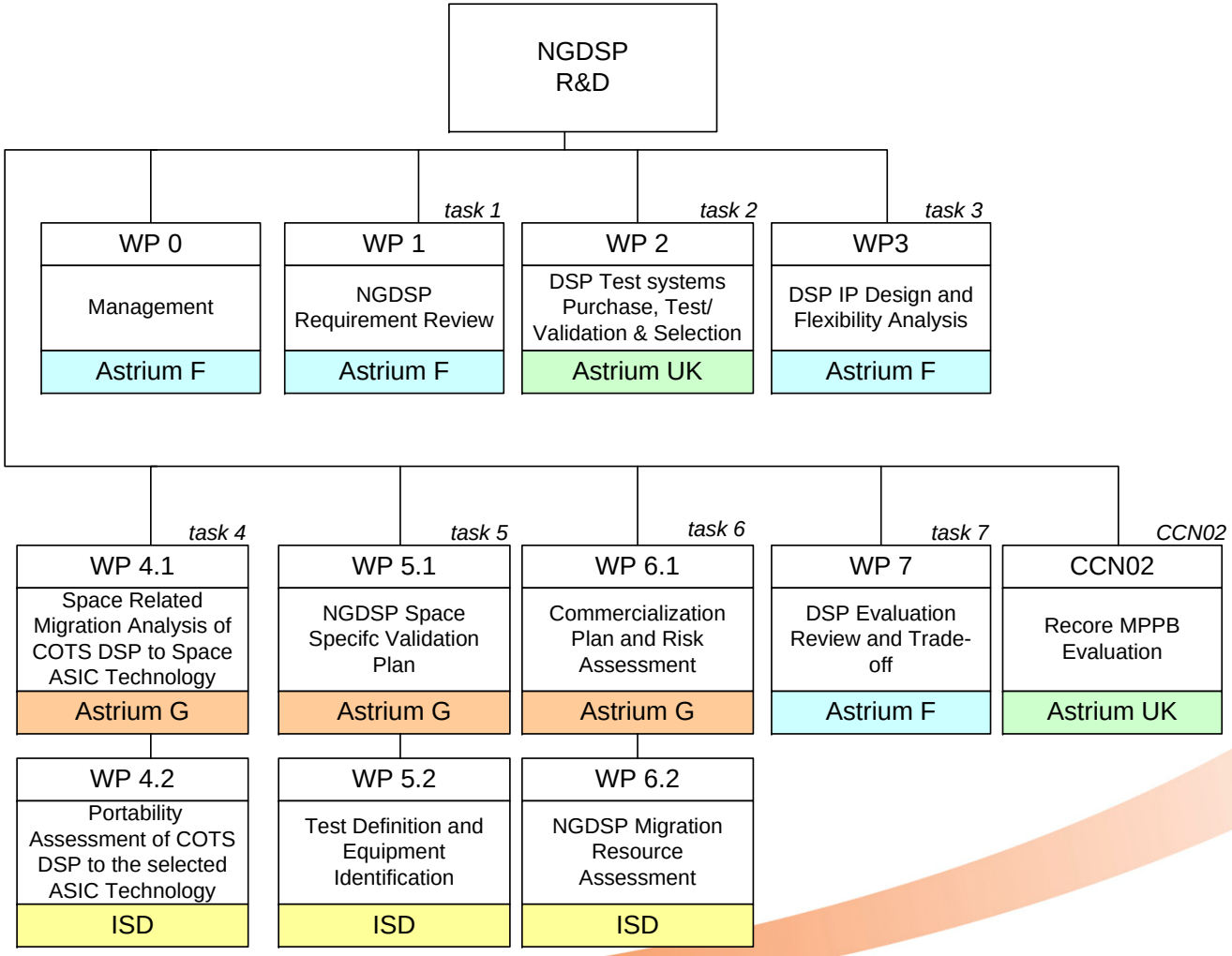
- ***For the 3 DSPs***
- **The review and consolidation of the requirements for the NGDSP .**
- **The performance assessment of the COTS DSP and corresponding SDE using the software benchmarks**

Objectives of the study (2/2)

- *For a selection of 2 DSPs*
- **the assessment of the enhancement of the DSP IP with respect to functionality, interfaces and radiation hardening**
- **the assessment of the portability of the enhanced DSP IP to the specified European space ASIC technologies**
- **the assessment of the cost and schedule required for the IP enhancement and the ASIC implementation up to the successful qualification of the space DSP and the commercialization as a standard component**
- **the execution of a trade-off and the recommendation of a baseline and a backup solution**

CONTENT - ACTIVITIES

NGDSP Work Breakdown Structure



Work Breakdown and Status

- WP1 : Requirement Analysis of the Space DSP
- WP2: SW Evaluation of the 3 DSPs
- WP3/WP4 : Migration Study of the 2 DSP selected
- WP5 : Validation of the Space DSP study
- WP6 : Ressource and Risk Assessment
- WP7 : Final Trade-off
- CCN02 : Software Evaluation of the RECORE solution

- WP1-WP6 : achieved - some reports in review
- WP7 : Final report to be issued
- CCN02 : achieved – reports in review

Activities Performed (1/2)

- R&D kick off Q4 2009
- At the kick-off confirmation that TI does not want to sell their DSP as an IP core.
- Software Evaluation draft report provided on Q2 2010.
- DSP selection possible in June 2010 : ADI ADSP-21469 and ATMEL Diopsis retained for next WPs
- WP3/WP4 Migration : difficulty to get information from ATMEL and ADI.
- Diopsis : Work started after ATMEL send data in August 2010. But ATMEL has stopped their DSP activities in November 2010 leading to a lack of support for the end of the migration study

Activities Performed (2/2)

- Migration reports for ATMEL DIOPSIS delivered to ESA in January 2011.
- ADSP-21469 – First data received in January 2011. Support from ADI good but latency very long.
- Migration reports for ADSP21469 delivered to ESA in July 2011.
- Validation Plan and Commercialization Plan and Risk Assessment report delivered to ESA in 2011

Activities Performed related to CCN02

- CCN02 related to RECORE MPPB evaluation.
- CCN02 has been limited to a SW evaluation due to budget. HW migration not studied (would have been interesting).
- CCN02 signed in January 2012
- Work completed - Draft report sent in July 2012

Access to information & NDA

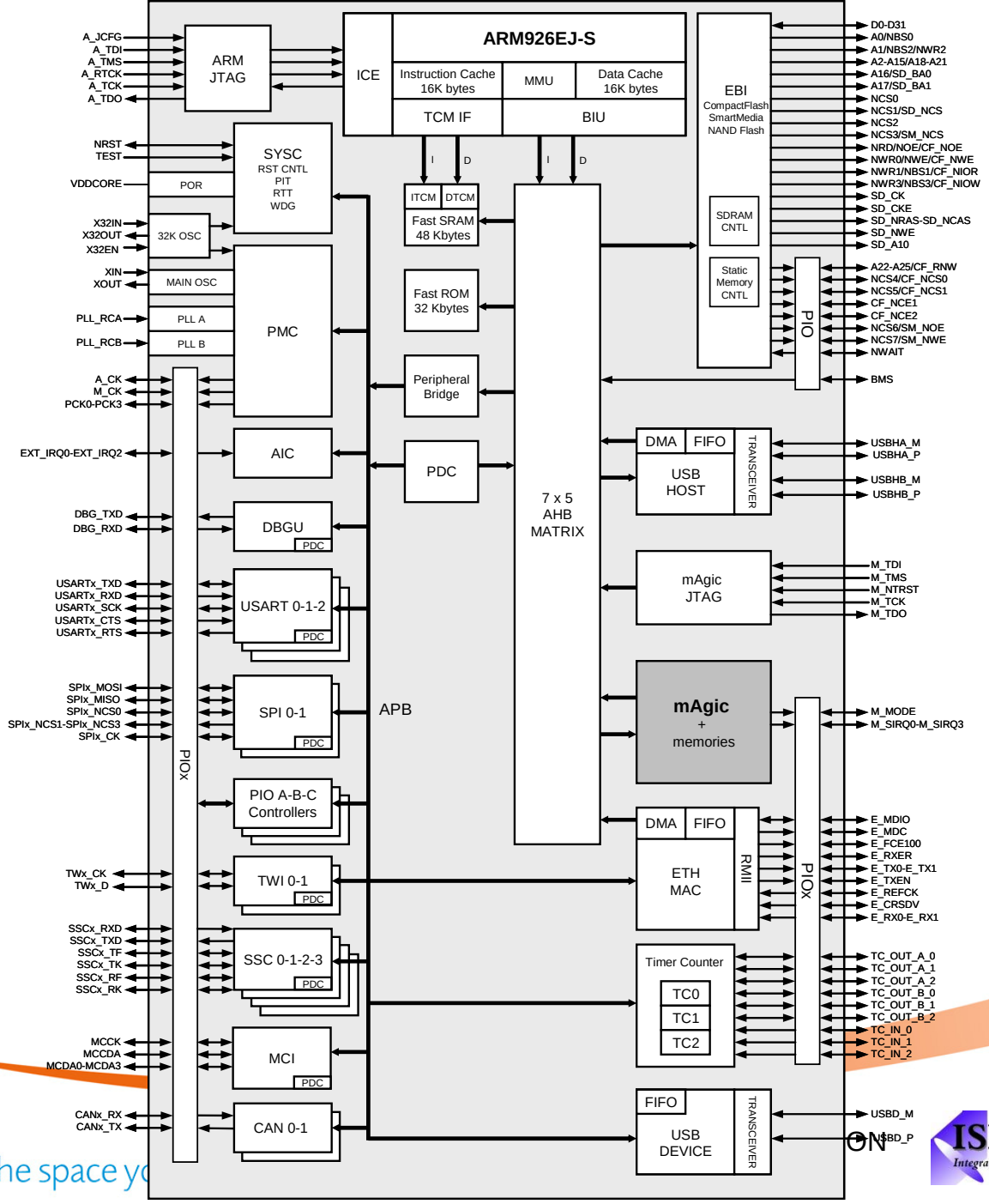
- Astrium and ISD have signed an NDA with ATMEL, Analog Devices, Recore and Texas Instruments to get information on the DSPs.
- So all the DSP characteristics that have been used for the analysis cannot be provided in this presentation.
- But these characteristics have been included in the reports delivered to ESA that have also signed NDA with the DSP vendors.
- STM 65 nm process and library characteristics are not easily available. For this activity Astrium has only used public presentations made at ESA and radiation reports. The evaluation related to STM 65 nm has been made by ISD.

RESULTS OF THE SOFTWARE EVALUATION of the 3 DSPs & RECORE solution

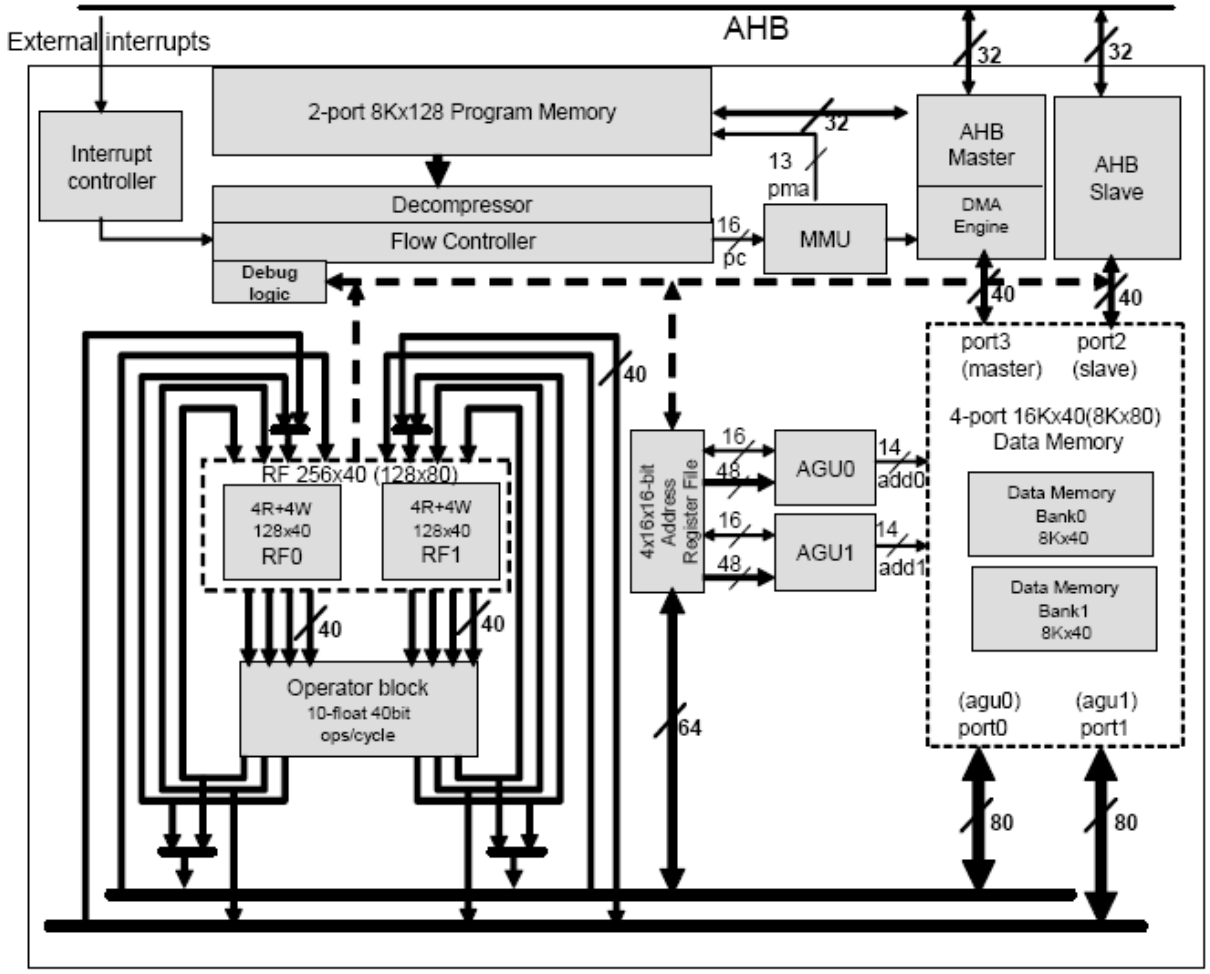
open John FRANKLIN's SW presentation

ATMEL DIOSPIS 940
Main Characteristics

ATMEL Diopsis block diagram



ATMEL Diopsis – mAgic Core structure



ATMEL Diopsis characteristics

- Based on an ARM926 + a DSP core called mAgic
- Techno 130 nm CMOS
- 160/ 200 MHz ARM926 - Half speed for the mAgiC Core
- 1 GFLops, DSP + 220 MIPS
- Data memory = 16kwords by 40-bit
- Program memory = 8kwords x 128-bit
- IO no High Speed Serial Link – but Ethernet & USB
- SRAM, SDRAM, E2PROM I/F
- 8.0 Gbytes/second bandwidth @ 100 MHz between core and register file.

ATMEL DIOSPIS 940
Migration Analysis

ATMEL DIOPIS Migration (1/2)

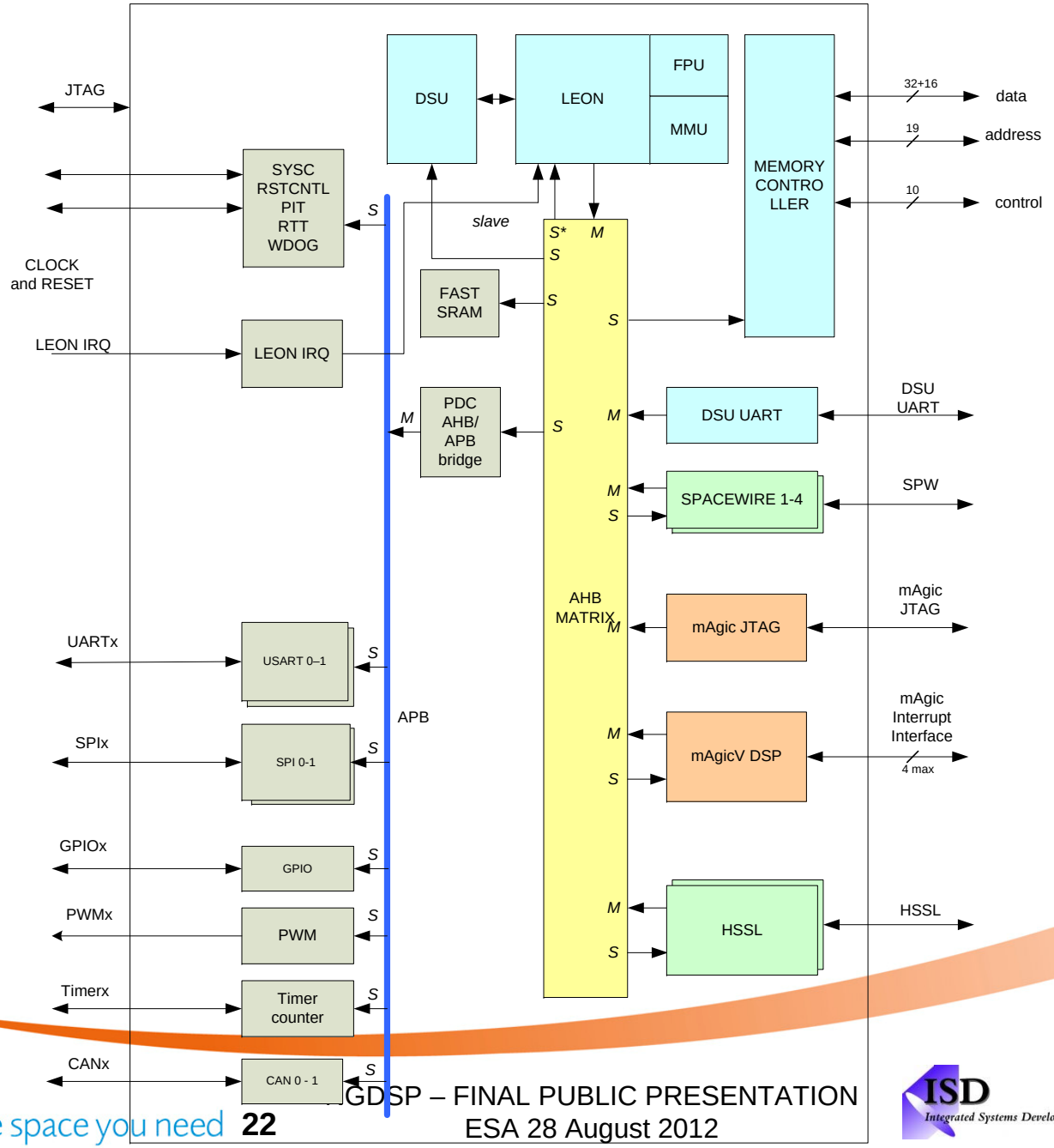
- **Migration quite "easy" from a HW point of view since the Diopsis structure is similar to SOC ASIC embedding a LEON processor + AMBA bus (e.g. SCOC3, MDPA…)**
- **ARM to be replaced by LEONx-FT that is hardened**
  - Trade-off between LEON2-FT LEON3-FT LEON4-FT open
- **Hardening of internal Memories**
  - EDAC and scrubbing engine insertion
- **Implementation of a synchronous reset**
- **Introduction of glitch free clock Muxs**

ATMEL DIOPIS Migration (2/2)

- Useless peripherals suppressed as TWI, USB, Ethernet
- Fast Space Peripherals connected to the AXI matrix as Spacewire
- HSSL link also connected to the AXI matrix via the SpaceFibre Protocol Management IP
- Slow Peripherals connected to the APB bus

Migrated DIOPSIS

a possible Architecture



ATMEL DIOPIS Migration Issues

- **Issues related to the migration:**
- **The Memory Controller has to be developed if a DDR I/F is implemented**
- **The SpaceFibre IP core managing the protocol on the HSSL link has to be available.**
- **The support concerning the mAgic is problematic due to the stop of ATMEL DSP business unit**
- **The mAgic DSP architecture suffers from limitations that would lead to a space DSP having poor performances.**

The mAgicDSP core limitations

FLOATING POINT VARIABLES IN 40 BITS vs EXTERNAL RAM 32 BITS

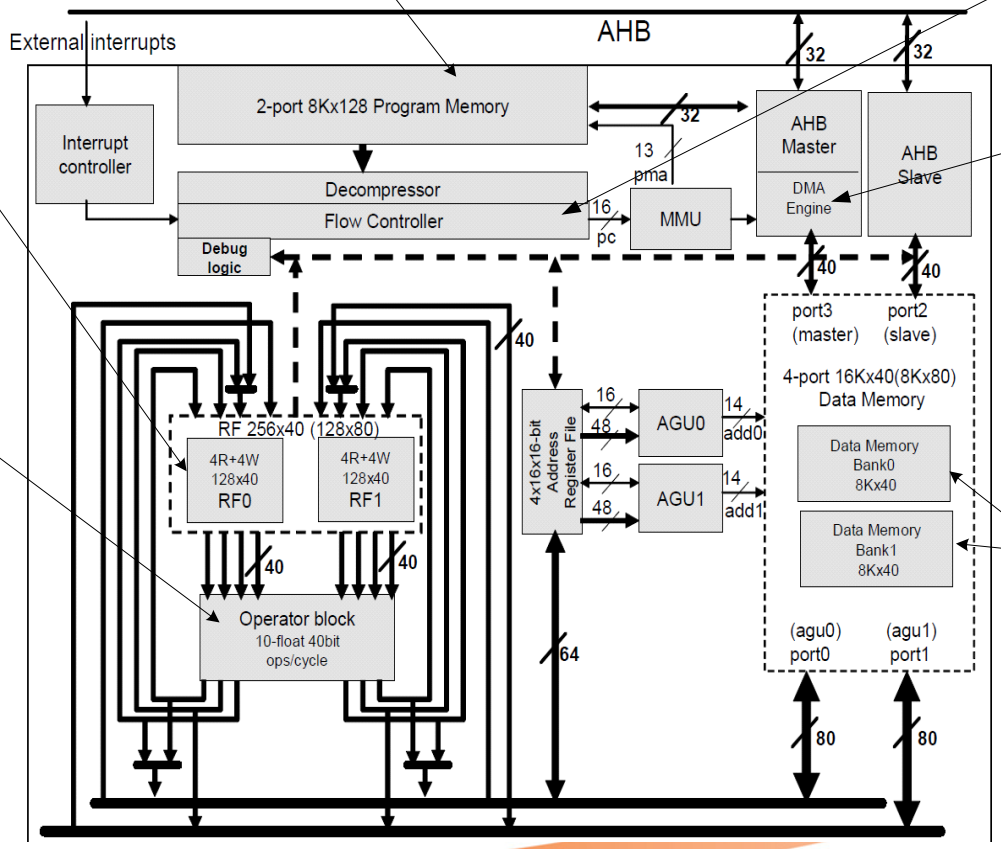
NO STALL OF PROCESSING TO FETCH DATA IN MEMORY

EXTERNAL MEMORY DMA ACCESS NO DIRECT ACCESS

TOO MANY REGISTERS FOR THE COMPILER

USE OF ¼ to ½ of HW

INTERNAL RAM TOO SMALL



Improving the mAgicDSP Core is difficult

- **The data memory should be increased by a factor of 2 or 4.**

-> In this case, the AGU (Address generation Unit) has to be modified and the size of the ad0/add1 busses increased to 16 or 17 bits.

-> the VLIW (Very Long Instruction Word) structure has to be increased

-> the SDE (Software Development Environment) is deeply modified.

<u>It impacts significantly the cost and the risks of the project.</u>

Migration Summary: STM vs. Atmel

Feature	STM	Atmel
Process availability	> 2014 (TBC)	Now
Operating frequency	200 MHz	65 MHz
DDR Memory support	Problematic	No
High Speed IOs	HSSL 6.25 Gbit/s	No IP macro available
No. of ASIC gates	2,436,000	2,380,000
Power consumption	1.1 W	3.1 W
Radiation mitigation technique	TMR FFs	Hardened FF
Radiation figure (first estimations)	6E-5 (hypothesis from KIPSAT1)	8 E -5

→If ever this device is ported it makes sense to use th STM65 technology

→Pre-requisites are : Technology needs to be qualified for space.

Package Assessment

- **If the chip is without the HSSL then any classical low pin count, space qualified package is suitable for this device**
  - Both STM and Atmel offer this kind of packages.
- **If the chip is with the HSSL then in order to get the maximum throughput from the serial links, a flip-chip approach should be used.**
  - This requires a more advanced packaging technology like the one proposed by E2V

IP cores for the Space DIOPSIS

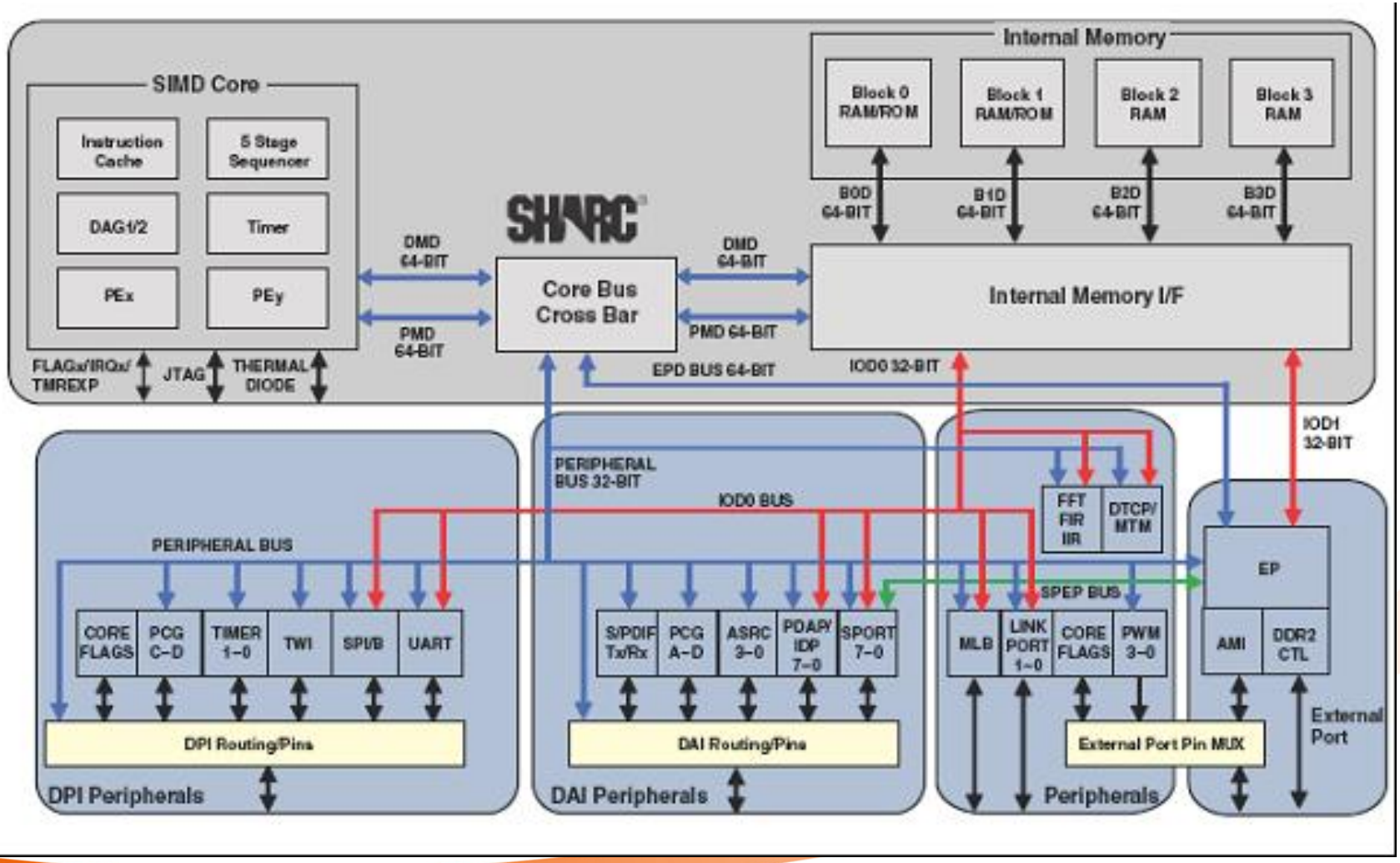
Function	Hard/Soft	IP core	Provider/Comments
LEONxx + DSU + FPU	S	Available	From AE/GR
SDRAM/E2PROM controller	S	Available	From AE/GR and some space companies
DDR controller	S	Not available	Problematic (1)
Service function (IT,..)	S	Available	From AE/GR GRLIB
mAgic core and its JTAG	S	Problematic	Provider/support unclear
High Speed Link	H	Available for STM	Only available from STM
SpaceFibre I/F	S	Not yet available	From UoD ?
AHB Matrix	S	Available	Can be redeveloped or purchased from IP vendors (2)
Spacewire-RMAP	S	Available	Many sources
Slow peripherals	S	Available	Many sources
Memory blocks	H	Available	Provided by the foundry
PLL	H	Available	Provided by the foundry

ATMEL DIOPSIS 940 migration conclusion

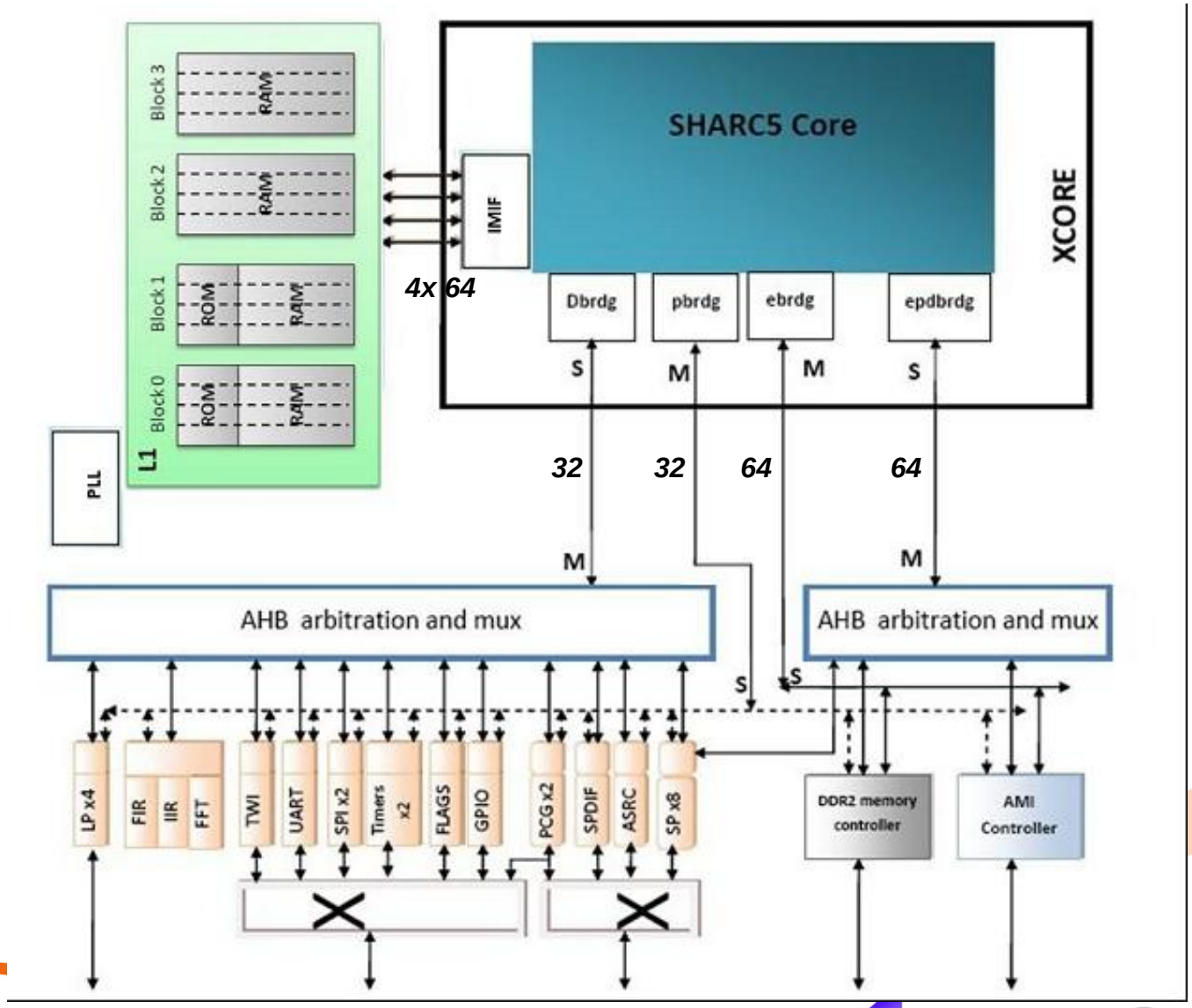
- The HW Migration of the Diopsis is quite “easy” since it is a well-known structure for companies developing SOC based on LEON.
- Most of its functions are well known and should be compliant with selected foundy. The DDR controller and the SpaceFibre IP are still missing.
- The space DSP is more adapted to the 65 nm STM process that provides better performances (X2) compared to ATMEL ATC18RHA.
- But the performances of the mAgic Core are not sufficient to justify the migration.
- Improving the mAgic core would lead to modify deeply the HW and make a new SDE. This is a long and risky task since the HW is no more supported and since the SW has been developed a long time ago with obslete tool.

ANALOG DEVICES – ADSP21469

Analog Devices ADSP-21469 – block diagram



ADSP-21469 - block diagram under NDA



Analog Devices ADSP-21469

- based on a DSP core called XCORE + L1 memory + IO block
- Techno 65 nm CMOS
- Speed 400 MHz max for the XCORE
- Half speed internal AHB bus 64 bits (2) or 32 bits (2)
- XCORE contains two processing elements that operate as a single-instruction, multiple-data (SIMD) engine. Each contains an ALU, multiplier, shifter, and register file.
- 2,4 GFlops / 800 MMACs
- 5 Mbits in 4 banks – 4 X 64 bits access in parallel
- IO no HSSL two 8-bit wide link ports, running at 166 MHz
- DDR2 & SRAM/E2PROM/SDRAM Interfaces

NGDSP MIGRATION STUDY OF ADSP 21469

ADSP 21469 XCore Migration (1/2)

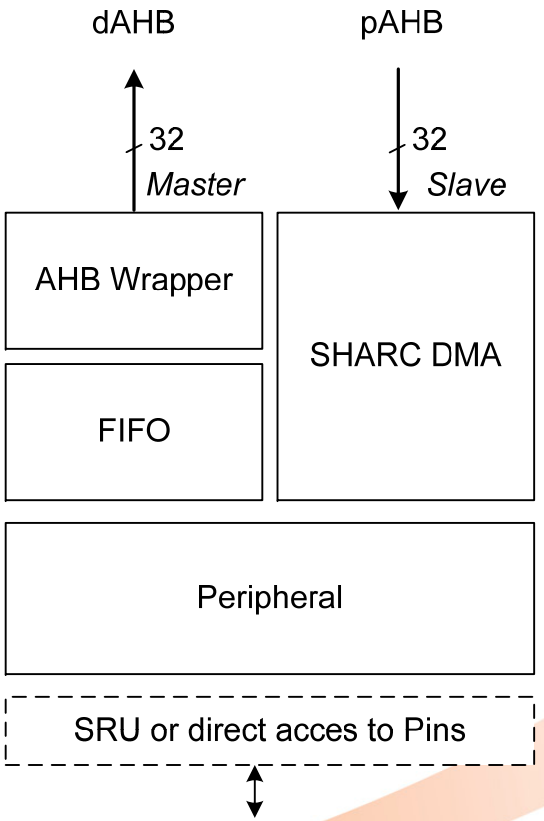
- **The DSP core "SHARC" must not be functionally changed, otherwise the compiler would have to be modified**
- **the DSP Core would be delivered by ADI as an IP core.**
- **The DSP Core contains features used to improve the timing performances → a fully synchronous XCORE model would be used for migration**
- **As memory, the DSP Core contains :**
  - L1 memory
  - An instruction cache
- **The instruction cache can be hardened with parity bits, in case of error a cache miss is activated.**

ADSP 21469 Core Migration (2/2)

- the L1 memory has to be hardened by using an EDAC to protect each 16-bit wide block (16->22 bits)
- A scrubbing of the L1 memory has also to be implemented : detect and correct single error – raise an interrupt in case of double error.
- Scrubbing can be made by a DMA peripheral connected on the AHB bus
- At first error detection has to be made.
- Then error correction has to be launched by an Interrupt Service Routine, since only the processor and not the DMA can perform Read-Modify-Write commands.

ADSP 21469 IO Migration (1/2)

- The IO block contains many functions that are not useful for space applications (audio processing, TWI..)
- The slow peripherals are connected to APB
- The other peripherals are connected by using a standard I/F to AHB developed by ADI
- best approach is to use this standard I/F and to connect space peripherals



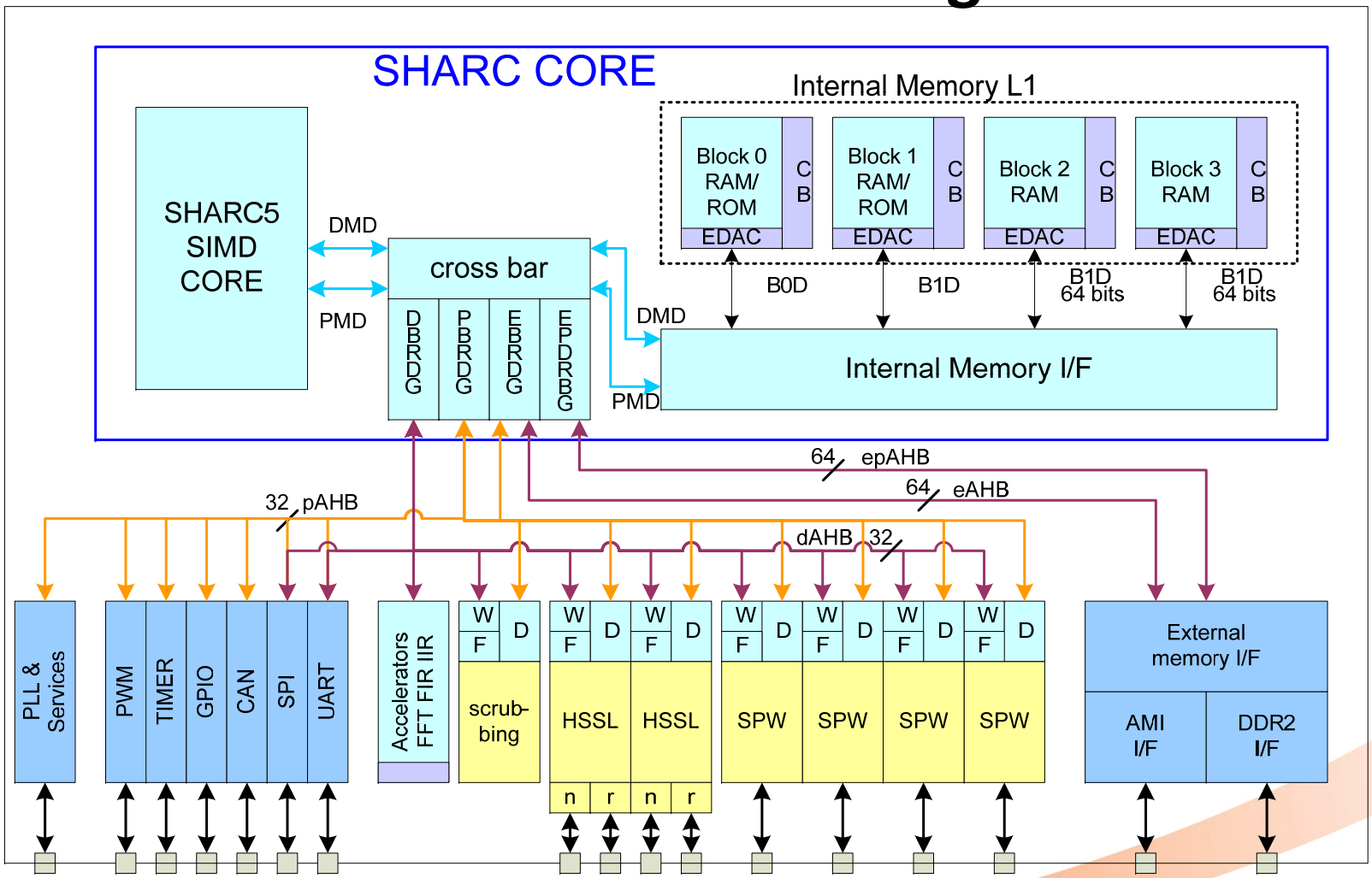
ADSP 21469 IO Migration (2/2)

- The HSSL can also be connected to the 32 bit AHB bus that runs at half the speed of the DSP core.
- But the throughput of the AHB bus is limited to 32*100 MHz ~ 3,2 Gbits/s
- A bottleneck would be created if 2 links are connected.
- Another solution would be to connect the HSSL to the 64 bit AHB bus used for memory I/F but it would conflict with memory accesses.

ADSP 21469 memory controller Migration

- 2 solutions :
- harden the ADI memory controller
  - difficult since RS codes have to be added for SDRAM/DDRAM, Hamming for SRAM and possibly triplication for E2PROM
  - Actual ADSP memory controller supports only DDR2
  - Due to NGDSP development duration, DDR3 (or even DDR4) should be the baseline.
- Adapt an existing “space” IP memory controller to the DSP, to DDR space RAMs and to the ST 65 nm process.
- This is still an issue.

ADSP structure after migration



unchanged elements

new elements

hardening structures for memories

modified elements

Summary of the IP cores required

Function	Hard/Soft	IP core	Provider/Comments	Hardening
IP core allowing to connect the peripherals on the AHB bus	S	Available	Analog Devices	to be done
SDRAM/E2PROM controller	S	Available	From AE/GR and some space companies	done
DDR controller	S	Not available	Problematic (1)	to be done
High Speed Link	H	Available for STM	Only available from STM	Done by STM
SpaceFibre I/F	S	Not yet available	From UoD or ESA	done
Spacewire-RMAP	S	Available	Many sources at least UoD/ESA – AE/GR	done
Slow peripherals	S	Available	Many sources at least AE/GR	done
Memory blocks	H	Available	Provided by the foundry	to add check bits, EDAC and possibly scrubbing
PLL	H	Available	Provided by the foundry	should be done by the foundry

AREA Estimation

- **ADSP21469 IP has ~ 1 Mio Gates**
- **Factors leading to increase of area req.:**
  - Use of TMR FFs (STM65) or Rad-hard FFs (ATC18)
  - EDAC check-bits for memory

Main Components	Number of Gates ATC18RHA	Number of Gates STM65
IOP	About 1,2 Mgates	About 1,4 Mgates
4 SPW interfaces with RMAP	~200 000	~200 000
XCORE	About 0,5 Mgates	About 0,5 Mgates
HSSL	N/A	~20 000
CRC FIFO for 2 HSSL channels	N/A	~60 000
Ext Memory Controller	N/A	~100 000
Total DSP (excl. on-chip memory)	~1 900 000	~2 300 000
Total chip area (incl. 5 Mbit RAM and 1.875 Mbit EDAC)	132 mm^2	38 mm^2
Die size (incl. pad & supply ring)	13 mm * 13 mm	7 mm * 7 mm

Package Assessment

- **Based on experimental verification within KIPSAT, the HSSL require:**
  - Flip-chip technology with properly positioned bumps in order to minimize parasitics,
  - The routing of the various signals at the PCB of the package should be perfectly matched.
- **After evaluation of existing packages, it has been concluded that a <u>dedicated package</u> solution is required.**
  - E2V is a candidate for package development.

Migration Summary: STM vs. Atmel

Feature	STM	Atmel
Process availability	**> 2014 (TBC)** **Currently under Development**	**Now**
Operating frequency	**200 MHz (expected)**	**70 MHz**
Expected performance*	**1.2 GFlops peak,** **0.4 GFlops practical**	**0.42 GFlops peak,** **0.14 GFlops practical**
DDR Memory support	**Problematic**	**No**
High Speed IOs	**HSSL 6.25 Gbit/s** **Package needs to be developed**	**No IP macro available**
No. of ASIC gates (excluding on-chip memory)	**~2 300 000**	**~1 900 000**
Power consumption	**~0.9 W**	**~2.7 W**
Radiation mitigation technique	**TMR FFs**	**Hardened FF**
Radiation figure (first estimations)	**2,2E-6** **(hypothesis from KIPSAT 1)**	**3,52 E-6**

→ STM65 technology is recommended for the migration of AD21469.

→ Pre-requisites are:

→ **Technology needs to be qualified for space.**

→ **Package needs to be developed and qualified for space.**

ADSP SDE Adaptation

Item	Status	Development
Part Activation of a new DSP in Andromeda tool for the space DSP	Specific to space DSP	Made by ADI
Management of the version of the space DSP in Andromeda	Specific to space DSP	Maintenance either ADI or ESA TBD
Header files and .xml files to define Memory Mapping Register MMR's for peripherals, and registers for visibility in the debugger	Specific to space DSP	Initial development made by ADI form SpaceDSP specification – Maintenance either ADI or ESA TBD
Control of silicon anomaly workarounds through the code generation tools	Specific to space DSP	Initial development made by ADI – Maintenance either ADI or ESA TBD
C/C++ compiler	Same as ADSP-21469	N.A. provided by ADI
Assembler	Same as ADSP-21469	N.A. provided by ADI
Linker	Same as ADSP-21469	N.A provided by ADI
Runtime libraries for the Space DSP part that support the C compiler	Same as ADSP-21469	N.A provided by ADI
Drivers and system services for the Space DSP peripherals	Specific to space DSP	Not provided by ADI – to be developed by ESA
Cycle-accurate simulator including a functional modelling of the peripherals (no cycle-accurate modelling of peripherals).	Specific to space DSP	The peripheral modelling has to be developed by ADI, the simulator does not have an open interface.

- **The level of qualification of the SDE and the Software libraries is not defined now. It may have a significant impact of the effort required for SW activities.**

ADSP21469 Migration conclusion (1/2)

- The HW Migration of the ADSP21469 is more complex since it concerns an advanced component using a structure not familiar to space developers.
- The SHARC core must not be changed except for memory hardening otherwise it may impact the compiler.
- The migration of the IO function is in fact a redesign based on existing space IP cores connected to the standard AHB I/F provided by ADI.
- The memory controller is still an issue since it has to embed ECC specific to space memories, be compliant with STM 65 nm process and also to space DDRx not yet selected.
- The validation of the space DSP is a significant task. It would be based for the DSP core on a testbench provided by ADI, for the new space IOs validation procedures will have to be developed.

ADSP21469 Migration conclusion (2/2)

- **The Migration of the ADSP21469 is difficult to envisage using a 0,18 um process, the STM 65 nm process is mandatory.**
- **The SDE has also to be migrated, but if the DSP core is unchanged the modifications would be limited to the IO management and drivers development.**

MIGRATION FLOW

Migration Flow (1/2)

- **Flow similar for ATMEL DIOPSIS and ADSP 21469.**
- **“Big ASIC development Flow” with an embedded processor.**

The Migration Flow Steps are :

- **Requirement Consolidation for Space DSP**
- **DSP Core IP modifications (hardening)**
- **Development of missing IPs (memory Controller)**
- **Assembly of the IO block**
- **Integration of DSP IP, space specific IPs and support logic**
- **HW/SW Verification of the DSP - Critical Issue**
- **Prototyping on a FPGA based platform with HW/SW verification**

Migration Flow (2/2)

- **Migration of the SW Development Environment (SDE)**
  - Modification of current SDE (to include new peripherals)
  - Verification of compatibility with commercial DSP SDE
  - Development of associated SW for new peripherals
  - Toolbox compatibility verification
- **DSP Foundry First Run**
- **Validation (functional, performance, radiation)**
- **Design Improvement**
- **DSP Foundry Second Run**
- **Validation (functional, performance, radiation)**
- **Hirel Qualification**
- **Commercialisation**

Development Schedule

- **Migration project start: Jan 2013 assumed.**
- **Availability of Space DSP: Beginning of 2018.**
- **2 runs are assumed**

RESSOURCE ASSESSMENT

RISK ASSESSMENT

Migration Contributors (1)

Abbrev	Description	Main Tasks
ESA	European Space Agency	- Responsible of the whole development - Negotiate Licensing agreement - IP acquisition
DSP_vendor	Owner of the commercial DSP (as ATMEL or Analog Device)	- Licence the DSP IP cores to ESA - Provide the DSP database - Support the Migration
Contractor or Prime	Responsible of the DSP migration in front of ESA	- Technical management of the Migration Activity - Responsible of the DSP specification - Responsible of the DSP validation - Can also carry out specific tasks according to their competence

Migration Contributors (2)

Abbrev	Description	Main Tasks
HW_Subco	**Design House in charge of the RTL development**	**- Acquisition of the commercial DSP database and other required IP** **- Migration of the DSP database** **- Development of the missing function** **- Integration of the RTL database of the DSP** **- Verification by simulation** **- Verification by HW prototyping (FPGA based prototyping)** **- Support for Gate Level Design and Chip validation** **- Synthesis on the target technology** **- Bist and Scan Insertion** **- Pre-Layout Static Timing Analysis** **- Equivalence check (RTL to Gate)** **- Post Layout back annotated simulation** **- Functional test vector generation** **- Development and manufacturing of radiation and evaluation test board** **- ASIC (prototype and flight model) device tests and validation**

Migration Contributors (3)

Abbrev	Description	Main Tasks
SW_Subco	Company in charge of the Software development	- Migration of the SDE - Qualification of the Space DSP SW tools - Performance Tests - Maintenance of the SDE - Support to Customers - Development of radiation test software - Support for ASIC (prototype and flight model) device tests and validation
Backend_Subco	Design House in charge of the Layout	- Place and Route for the space DSP - Post-layout extraction and checks - Post-layout Static Timing Analysis check - Equivalence check (pre-layout Gate to post-layout Gate) - Foundry Test program development - GDSII generation - ATPG Vector generation (tester specific format) and simulation (for both stuck-at and TDF)

Migration Contributors (4)

Abbrev	Description	Main Tasks
Foundry	**Foundry**	**- Wafer manufacturing of the prototypes and flight models.**
ATH	**Assembly and Test House (can be the Foundry)**	**- Wafer Probing & Sawing** **- Prototype Packaging and Test** **- Flight Model Packaging, Test and Qualification**
RTH	**Radiation Test House**	**- perform TID tests** **- perform SEE tests**

CONCLUSION

Final Conclusion (1/2)

- **Atmel DIOPSIS is too unstable & slow to use with a very user-unfriendly development & debug environment. The migration of the ATMEL DIOPSIS 940 is not recommended due to the low performance obtained by the existing mAgic DSP core. Moreover, the improvement of this core is a risky project.**

- **Both TI C6727 and ADSP-21469 are seen as good user-friendly development and debug environments, with roughly similar performances.**
- **But TI C6727 is not available as an IP core.**

Final Conclusion (2/2)

- The ADSP21469 migration would require a significant effort, but it can be a very attractive solution, if commercial terms are agreed. The STM 65 nm process is required. However a fast DSP requires fast memories, and the interfacing to DDR2/3 memories needs to be assured. The qualification of the SDE and the Software libraries may have a significant cost impact.
- Xentium core appears to be an efficient solution, but Astrium has only considered SW aspects and has not investigated the HW migration of the Recore Solution to a rad hard technology.
- From a technical point of view, it is recommended to implement the next generation DSP based on ADI DSP IP.