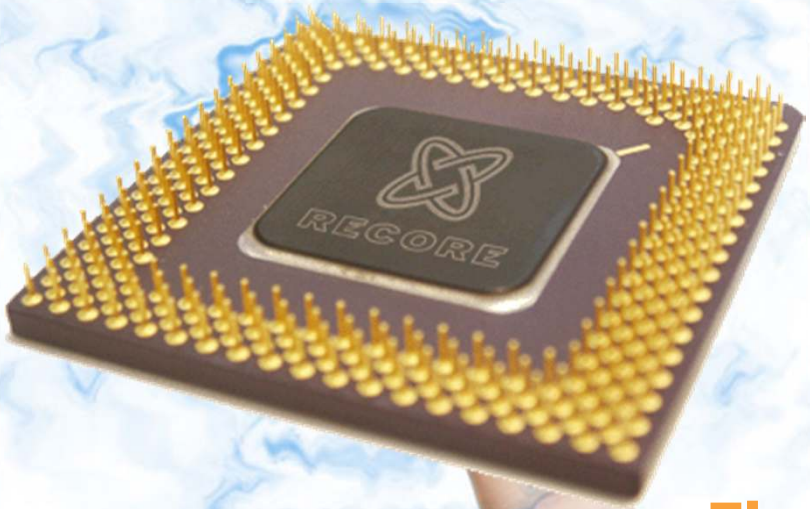
28 August 2012

Massively Parallel Processor Breadboarding (MPPB)



Final Presentation

TRP study 21986

Gerard Rauwerda
CTO, Recore Systems
Gerard.Rauwerda@RecoreSystems.com

RECORE

Recore Systems BV
P.O. Box 77, 7500 AB,
Enschede, The Netherlands
☎ +31 53 4753 000
+31 53 4753 009
info@recoresystems.com
www.recoresystems.com

Massively Parallel Processor Breadboarding

- ESA contract: 21986
- Technical Officer: Dr. Roland Trautner (TEC-EDP, ESA-ESTEC)
- Objectives
  - Develop and demonstrate reconfigurable multi-core DSP
  - Benchmarking of next-generation space DSP applications
  - Identify reconfiguration mechanisms for reliable and dependable SoCs
- Project execution
  - Original contract: 2009 – 2012
  - CCN extension: 2011 – 2012
- Contractors:
  - Recore Systems BV, Enschede, The Netherlands
  - University of Twente, Enschede, The Netherlands

© 2012 Recore Systems BV

Massively Parallel Processor Breadboarding

Multi-core SoC benchmarking of Recore's reconfigurable DSP technology in FPGA prototype for space applications

- Activities in original contract (2009-2012):
  - Define MPPB architecture
  - NoC / SoC design and implementation
  - Verification & Validation of MPPB
  - Benchmark application implementation

© 2012 Recore Systems BV

Massively Parallel Processor Breadboarding

Multi-core SoC benchmarking of Recore's reconfigurable DSP technology in FPGA prototype for space applications

- Activities in CCN (2011-2012):
  - Extend software with floating-point support
    - Emulation of floating-point in software
  - Analysis of ASIC migration and rad.-hardening effects
  - Feasibility of FDIR (Fault Detection, Isolation & Recovery)

© 2012 Recore Systems BV

Recore Systems

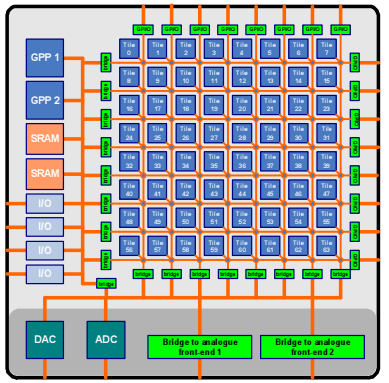
- Fabless semiconductor company
  - Based in The Netherlands
  - Established in September 2005
- Business model
  - Semiconductor devices business
  - Intellectual Property (IP) licensing
- Technology keywords
  - Reconfigurable multi-core Systems-on-Chip
  - Digital Signal Processing
- Focus markets
  - Digital radio/TV broadcasting (e.g. media players)
  - Wireless communication (e.g. cell phones)
  - Beamforming (e.g. advanced radar systems)

© 2012 Recore Systems BV

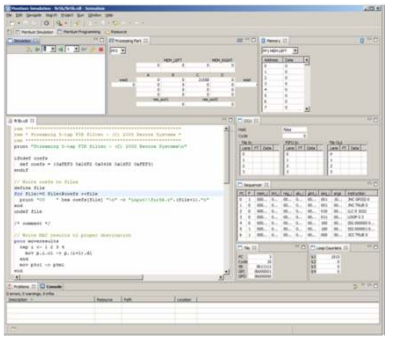
Products and services providing complete solutions

- Intellectual Property
  - Hardware
    - Reconfigurable multi-core processors
    - Montium®, Xentium® and Memtium™
  - Software development tools
    - Industry standard development tools for programming our processors
  - Configware™
    - Digital Signal Processing application software for our processors
- Semiconductor devices
  - Moon™ → digital radio/TV
  - Reflex™ → embedded DSP

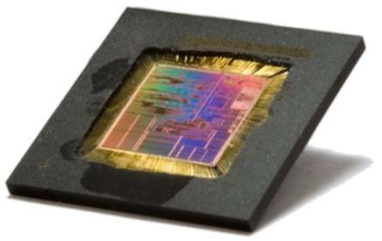
Many-core IP *for stream processing*



Design tools *Eclipse based IDE*



Silicon Proven *Montium 4-core*



© 2012 Recore Systems BV

University of Twente (UT)

- University from Enschede, The Netherlands
  - Degree programmes range from **business administration**, **psychology** to **applied physics**, **engineering** and **biomedical technology**
  - Applied sciences research: **nanotechnology**, **process technology**, **engineering**, **information & communication technology** and **biomedical sciences**

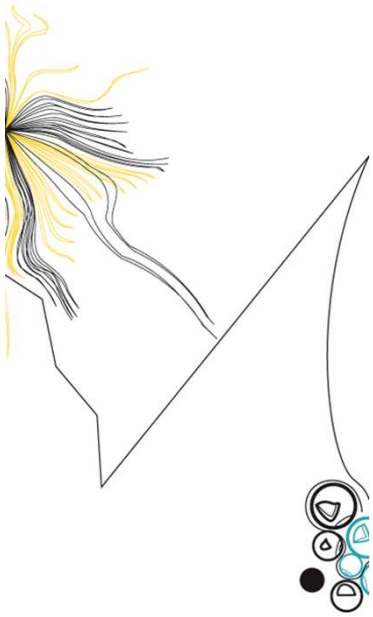
- Computer Architecture for Embedded Systems:
  - Karel Walters – PhD-student
  - Gerard Smit – full professor Computer Architectures for Embedded Systems
  - Sabih Gerez – assistant professor CAD systems

© 2012 Recore Systems BV

CAES group Research focus

Energy-efficient Embedded Systems

- Research themes
  - Efficiency in ICT systems
    - Energy efficient Streaming Architectures (Smit, Kokkeler, Kuper, Bekooij)
      - +/- 15 PhD students
    - Efficient and dependable mixed signal ICs (Kerkhoff)
      - 6 PhD students
  - Using ICT for efficiency
    - Energy management in Smart Grids (Smit)
      - 5 PhD students + 1 PD



Highlights of CAES

- Start-up companies
  - Recore Systems
  - Bibix systems
  - Smart Signs solutions
  - HOMA software
- Strong cooperation with industry
- Mix of fundamental (NWO) and applied research (STW/EU FP7/BSIK/ direct funded)
- Research eco system in the group
- Focus on energy resulted in many funded projects
- Excellent cooperation with other EWI chairs (EE + CS + MATH)

Outline

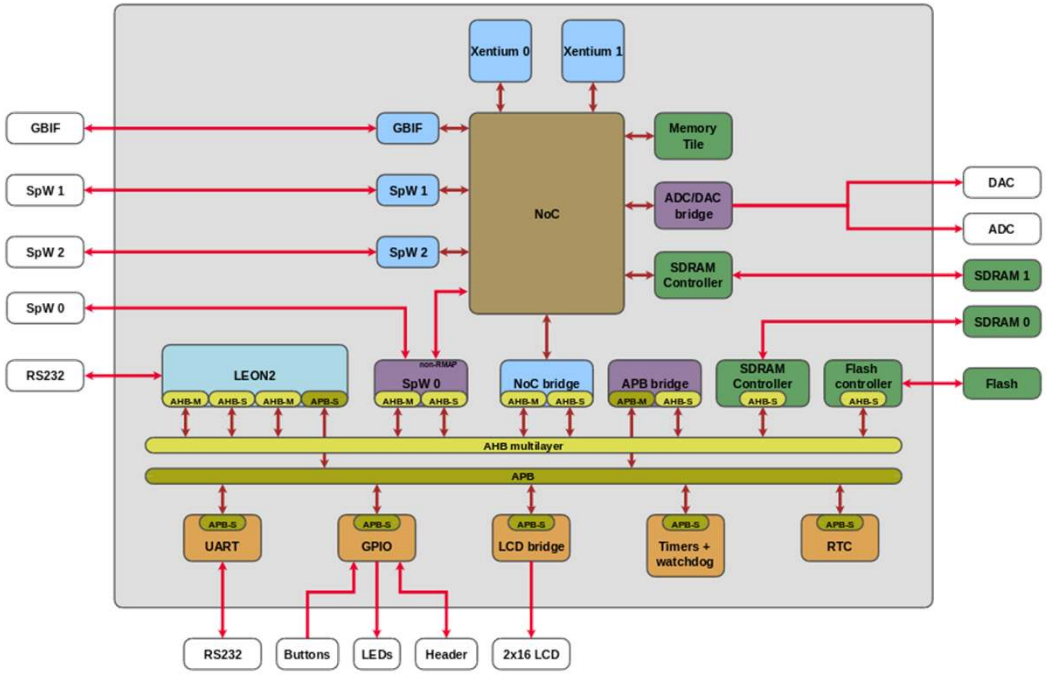
- MPPB platform hardware
- MPPB / Xentium® software development

- MPPB validation & benchmarking
- MPPB FDIR
- ASIC migration & radiation hardening
- MPPB lessons learned / future directions
- MPPB demonstration
- Q&A

© 2012 Recore Systems BV

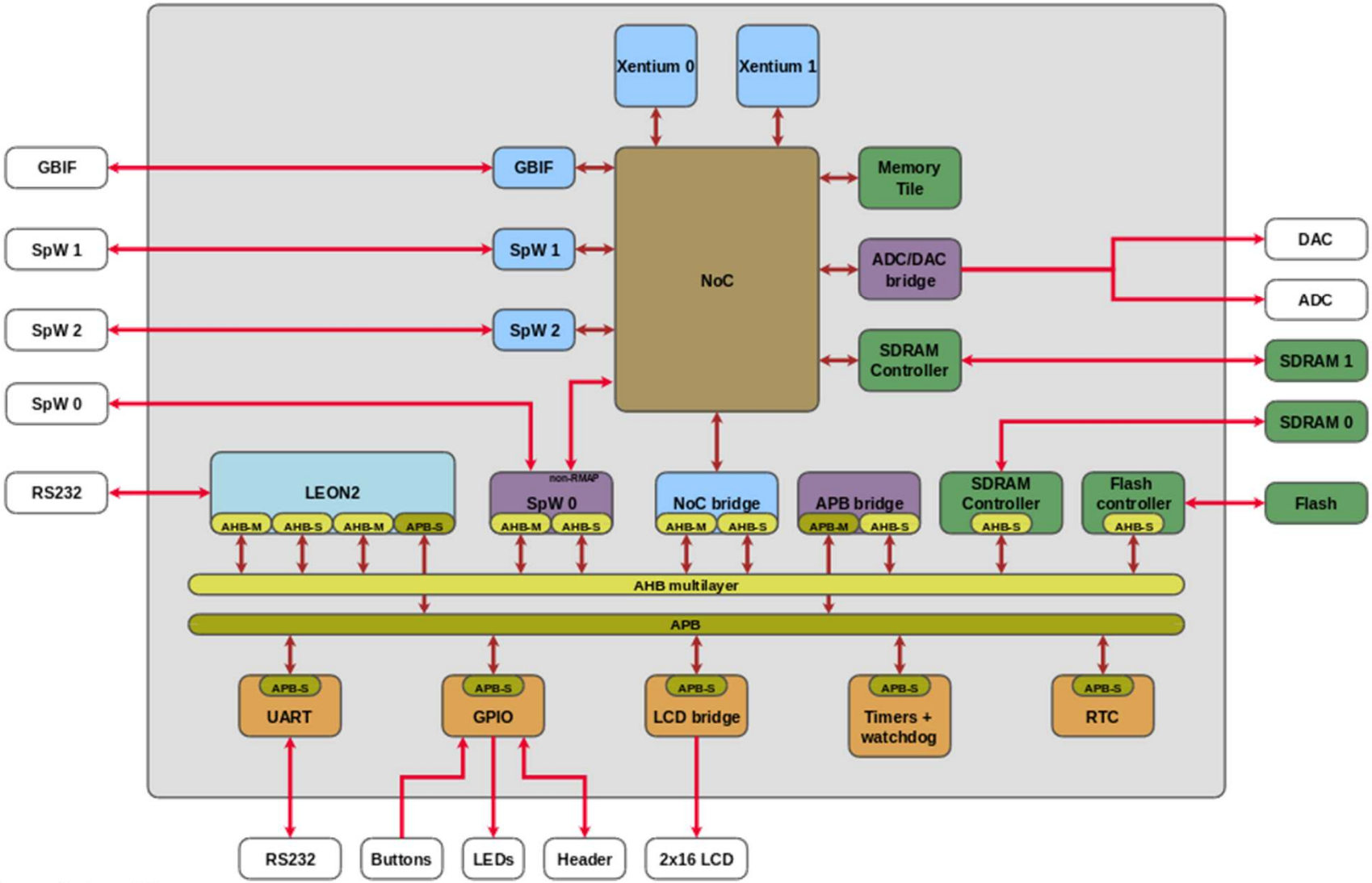
MPPB features
on a Xilinx Virtex-5 FPGA

- 50 MHz system clock
- 2 Xentium DSP tiles
- 1 Leon2 processor
- Network-on-Chip
- Heterogeneous memories
- High speed interfaces



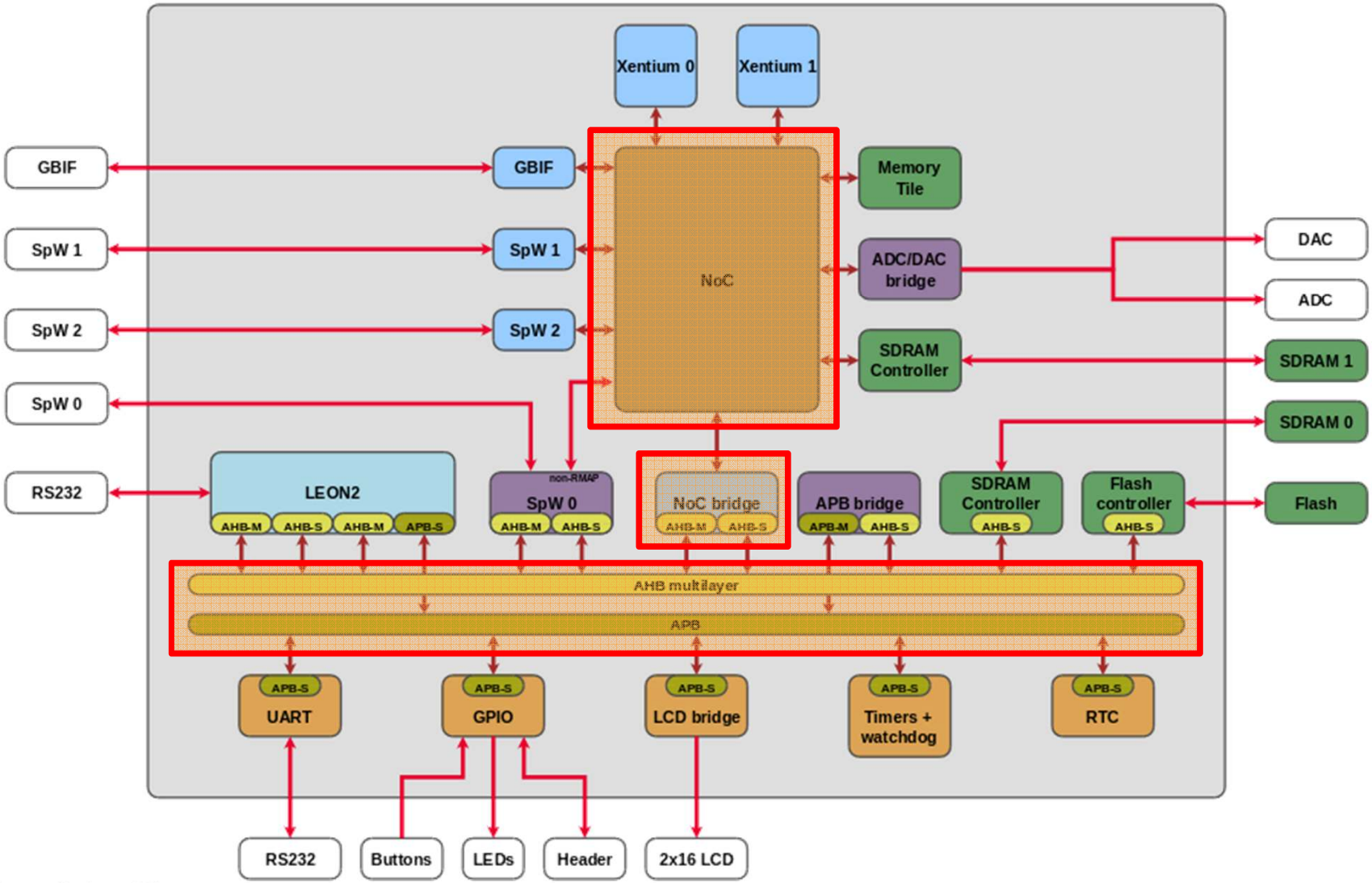
© 2012 Recore Systems BV

MPPB architecture



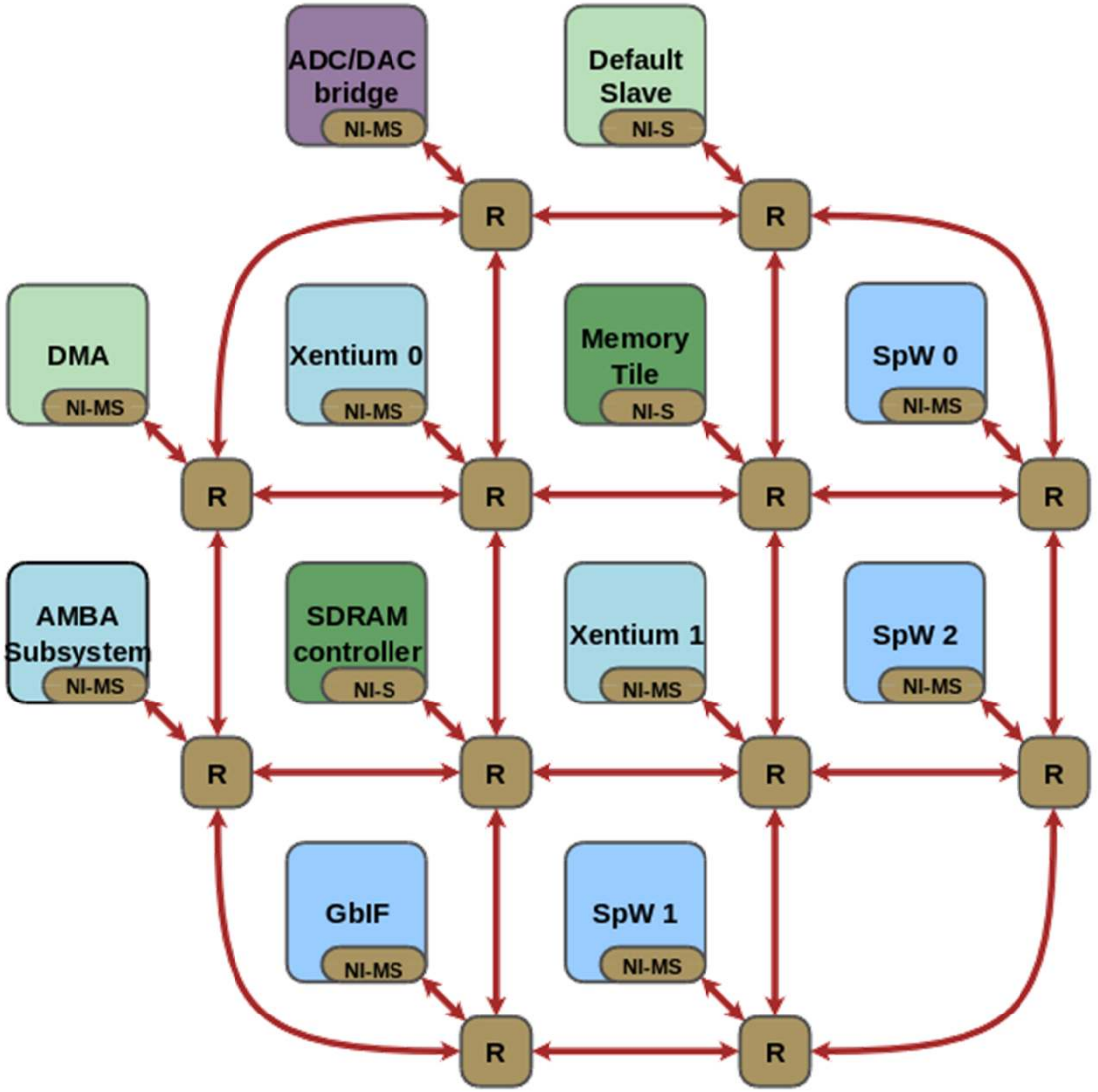
© 2012 Recore Systems BV

MPPB architecture
On-chip interconnect



© 2012 Recore Systems BV

NoC subsystem



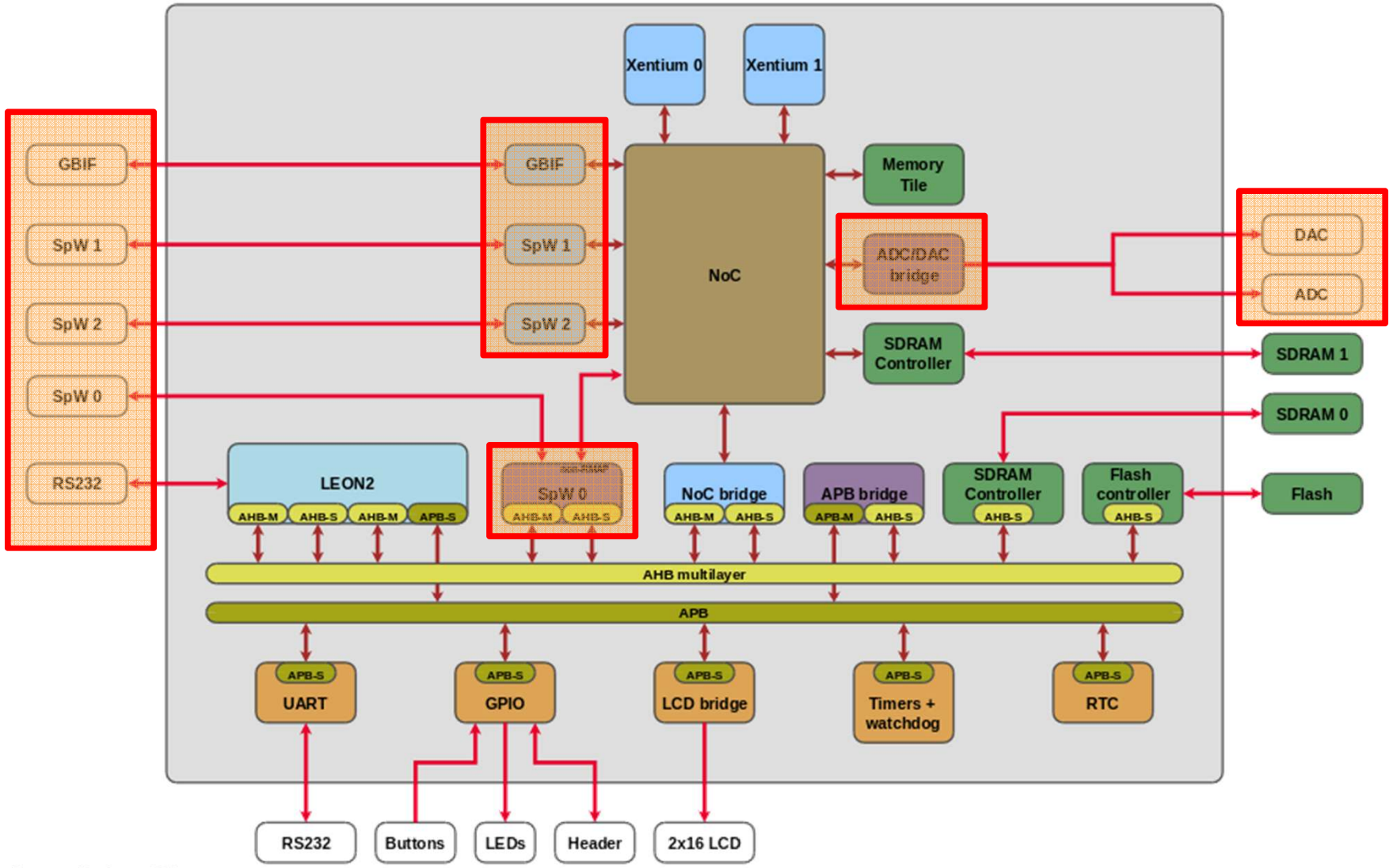
© 2012 Recore Systems BV

Interconnect
NoC

- Purpose
  - Interconnects NoC components
  - Scalable (#cores, #interfaces, #memories)
- Features
  - Packet-switched routing
  - 5 port routers
  - 4 services, priority based
    - for throughput and latency guarantees
  - Memory mapped communication protocol layer
  - X-Y routing
    - Deadlock free
    - Design-time layout of tiles based on estimated traffic load

© 2012 Recore Systems BV

MPPB architecture
High-speed interfaces



© 2012 Recore Systems BV

MPPB interfaces
Bridges

- NoC interface bridges to connect external peripherals
  - Memory-mapped network interface
  - Packing/unpacking of data
  - Configuration of external peripherals

- SpaceWire link – NoC bridge
- Gigabit link – NoC bridge
- ADC & DAC – NoC bridge

© 2012 Recore Systems BV

MPPB interfaces
SpW-NoC

- Purpose
  - Provides standard interface for space systems
  - Without RMAP support
- Features
  - Network interface with DMA
  - Using ESA SpW-b IP as back-end
  - Memory mapped transmit and receive buffers
  - Memory mapped status and configuration registers
  - Link speed: 100 Mbps

© 2012 Recore Systems BV

MPPB interfaces
SpW-AHB

- Purpose
  - Provides standard interface for space systems
  - RMAP target
    - Useful for debug purposes
    - Data transfer initiated by host
- Features
  - AHB master/slave
  - Using ESA SpW-RMAP IP as back-end
  - Memory mapped transmit and receive buffers
  - Memory mapped status and configuration registers
  - Link speed: 100 Mbps

© 2012 Recore Systems BV

MPPB Interfaces
ADC/DAC-NoC bridge

- Purpose
  - Provides parallel input interface for ADC board
  - Provides parallel output interface for DAC board

- Features
  - Memory-mapped network interface with DMA
  - Packing/unpacking of samples in/from 32-bit NoC words
  - Configurable sampling rate of ADC
  - Configurable sampling rate of DAC

  - Physical interfaces for ADC and DAC are dedicated for
    - AD6644 – Analog Devices, ADC, 14-bits @40MSPS
    - DAC5662 – Texas Instruments, DAC, 12-bits @40MSPS

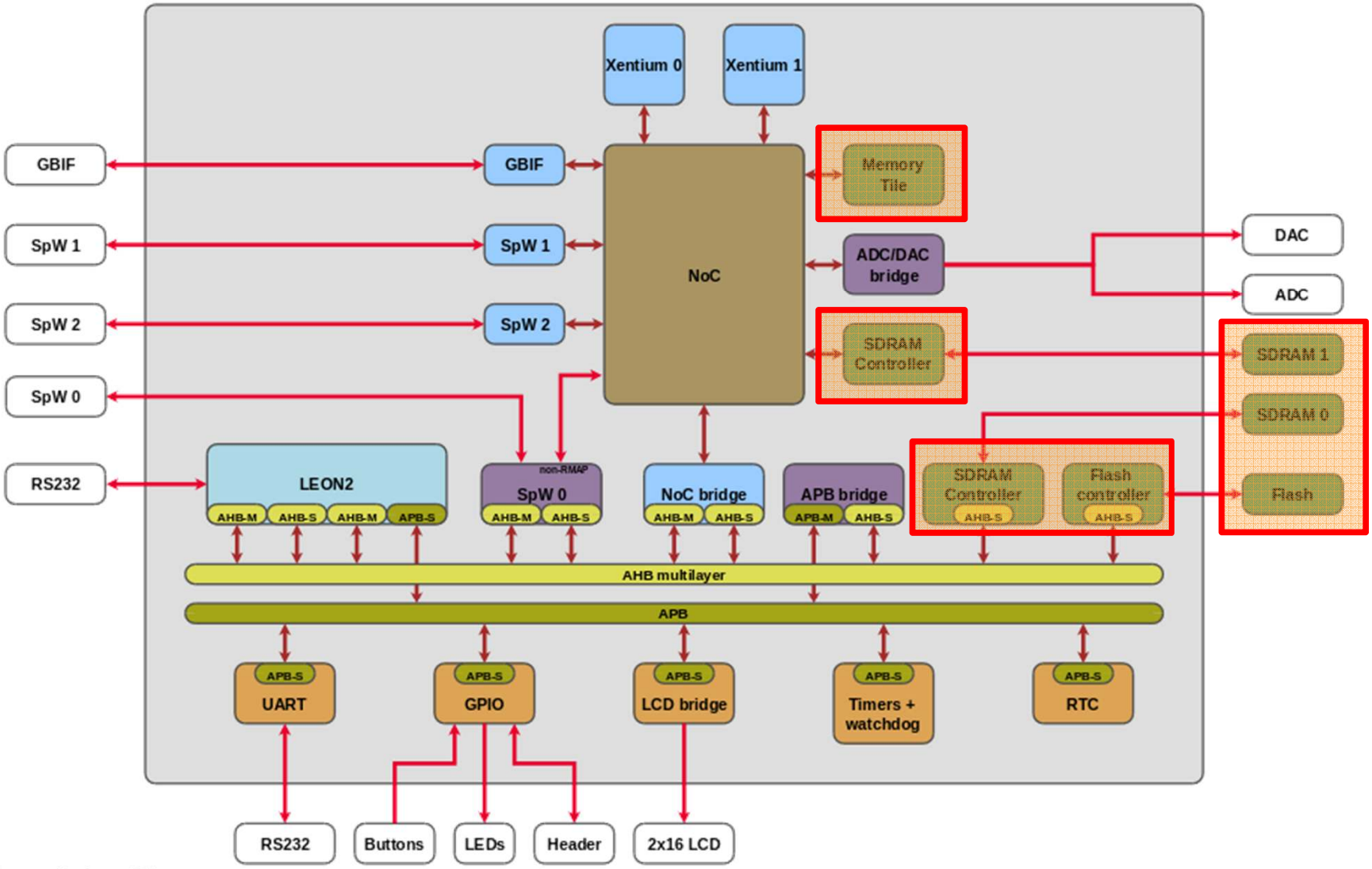
© 2012 Recore Systems BV

MPPB Interfaces
GigaBit link

- Purpose
  - Connecting two chips via the NoC
  - Increase resources (interfaces, processors and memory)
- Features
  - Memory-mapped network interface with DMA
  - Aurora link layer protocol
  - Net throughput measured 1.1 Gbps (board-to-board)

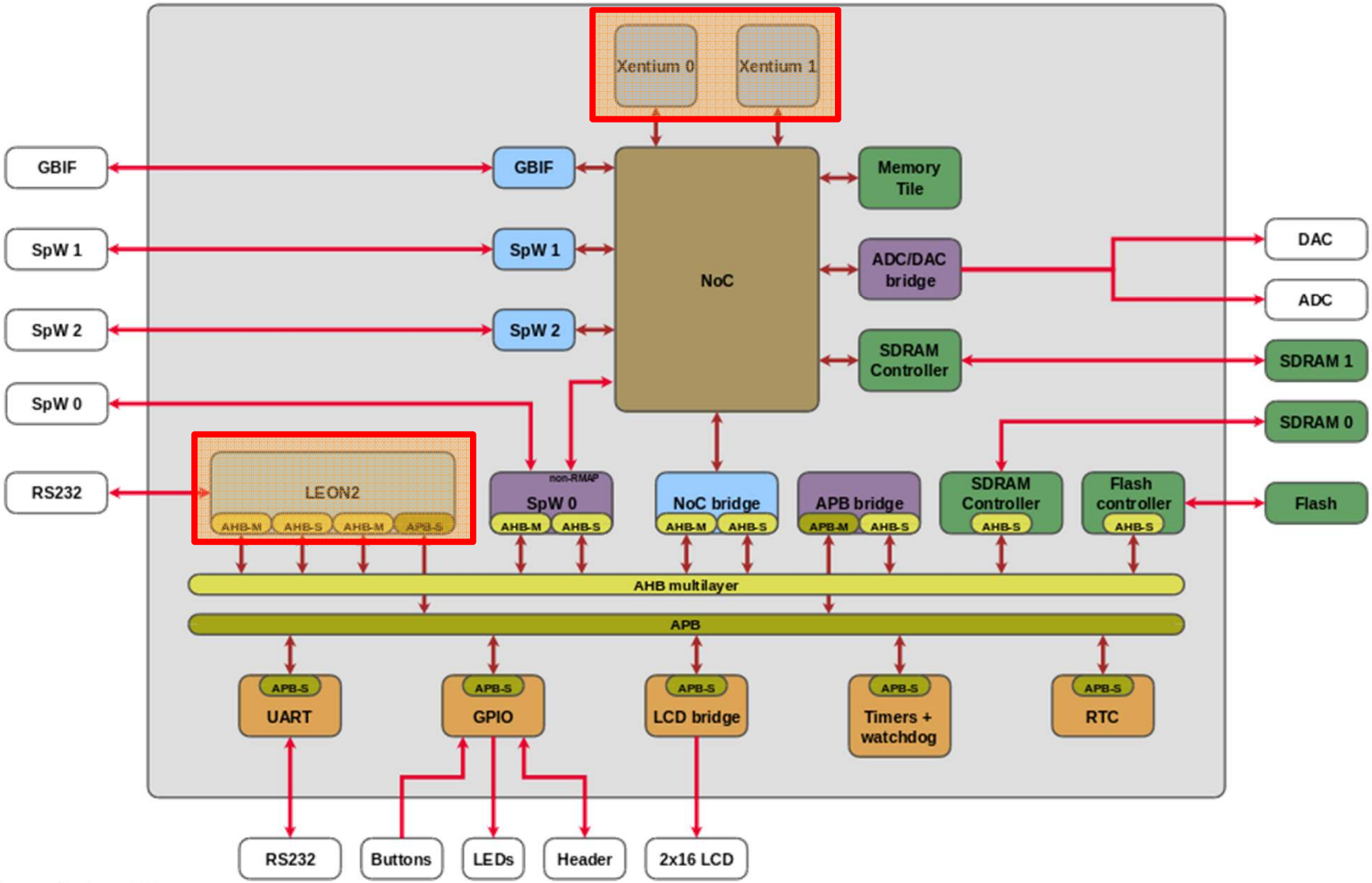
© 2012 Recore Systems BV

MPPB architecture Memories



© 2012 Recore Systems BV

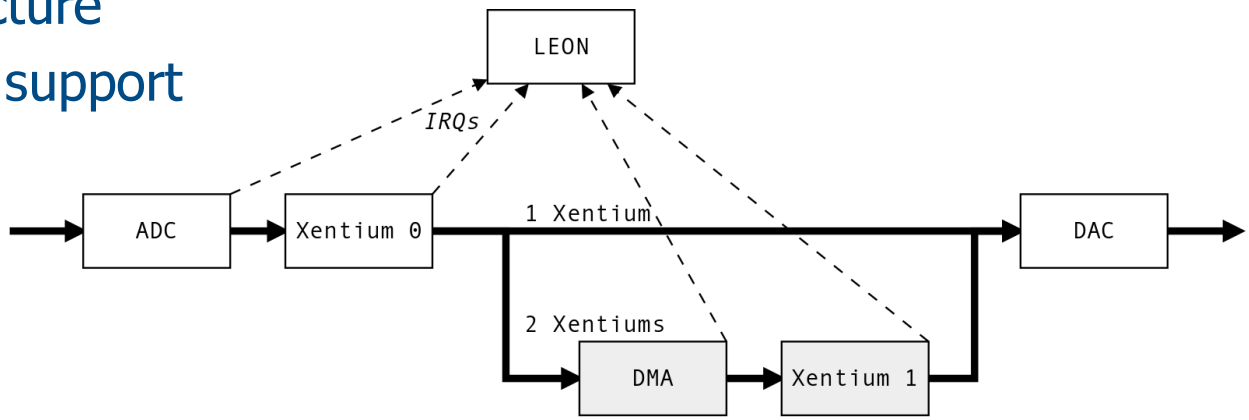
MPPB architecture
Processing cores



© 2012 Recore Systems BV

Leon2 processor

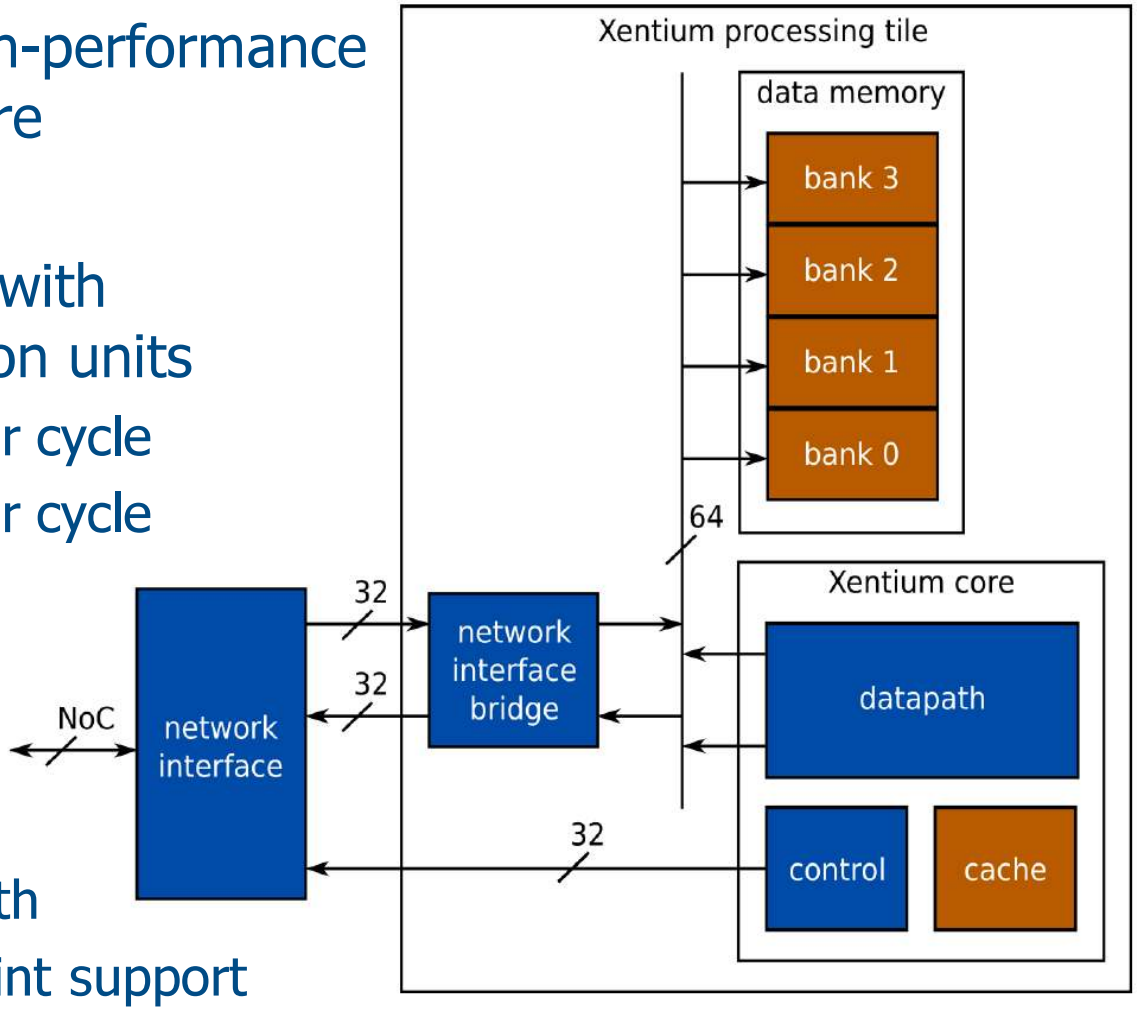
- Purpose
  - Perform control-related tasks
    - Boot system
    - Configure DMA transactions in NoC
    - Control Xentium processors
    - Setup MPPB system (peripherals, interfaces, etc.)
    - Monitor and output status of applications
- Features
  - Sparc V8 architecture
  - Hardware debug support



© 2012 Recore Systems BV

Xentium® processing tile

- Programmable high-performance fixed-point DSP core
- VLIW architecture with 10 parallel execution units
  - 4 16-bit MACs per cycle
  - 2 32-bit MACs per cycle
  - 2 16-bit complex MACs per cycle
- Data precision
  - 32/40-bit datapath
  - Block floating-point support



© 2012 Recore Systems BV

MPPB features
on a Xilinx Virtex-5 FPGA

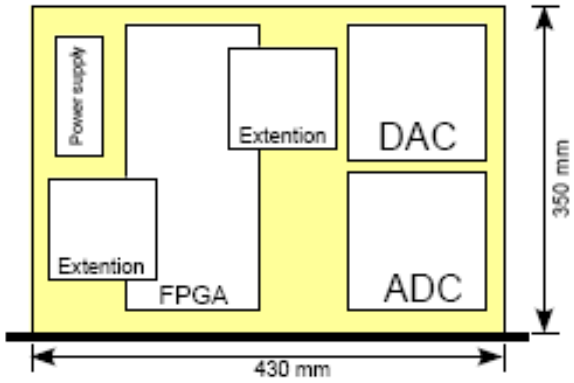
- 50 MHz system clock
- 2 Xentium tiles (@ 50MHz)
  - 2×200 16-bit MMAC/s
  - 2×100 32-bit MMAC/s
  - 2×100 16-bit complex MMAC/s
  - 2×32 KB data memory
  - 2×8 KB instruction cache
  - 1M FLOPS SP (emulated)
- 1 Leon2 processor (@ 50MHz)
  - 32-bit SPARC V8
  - Debug Support Unit / UART
- Network-on-Chip (@ 50MHz)
  - 32-bit packet-switched
  - 1.6 Gbps per link
    - In each direction
- Memories
  - 256 KB memory tile on NoC
  - 256 MB SDRAM on NoC
  - 256 MB SDRAM on AHB
  - 128 MB Flash on AHB
- SpaceWire (100 Mbps link)
  - 3 SpW-NoC interfaces
    - 1 including RMAP-target
- Gigabit interface
  - 1.1 Gbps full-duplex
    - Aurora link layer protocol
- ADC/DAC-NoC interface
  - Configurable sampling rate
  - 14-bit, 40 MS/s, ADC
  - 12-bit, 40 MS/s, DAC

© 2012 Recore Systems BV

MPPB box assembly

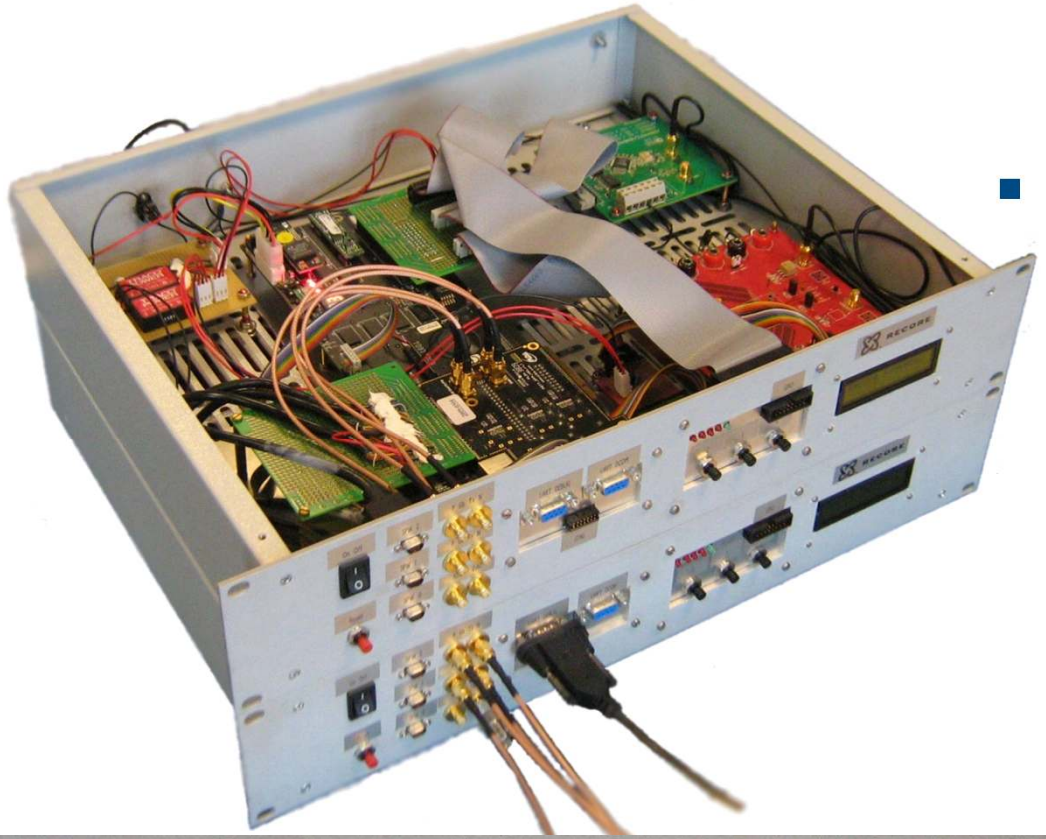
MPPB unit contains:

- FPGA development board
- 2 interface extension boards for
  - ADC, DAC, SpW 0 / 1 / 2, GPIO
- 1 Gigabit interface board
- ADC evaluation board
- DAC evaluation board
- LCD
- Power supply
  - Internal: 12V, 5V
  - External: 230V



© 2012 Recore Systems BV

MPPB Box



- 3 MPPB boxes delivered to ESA/ESTEC
  - Evaluation by EADS/Astrium
  - Networking/Partnering Initiative (NPI) with Polimi

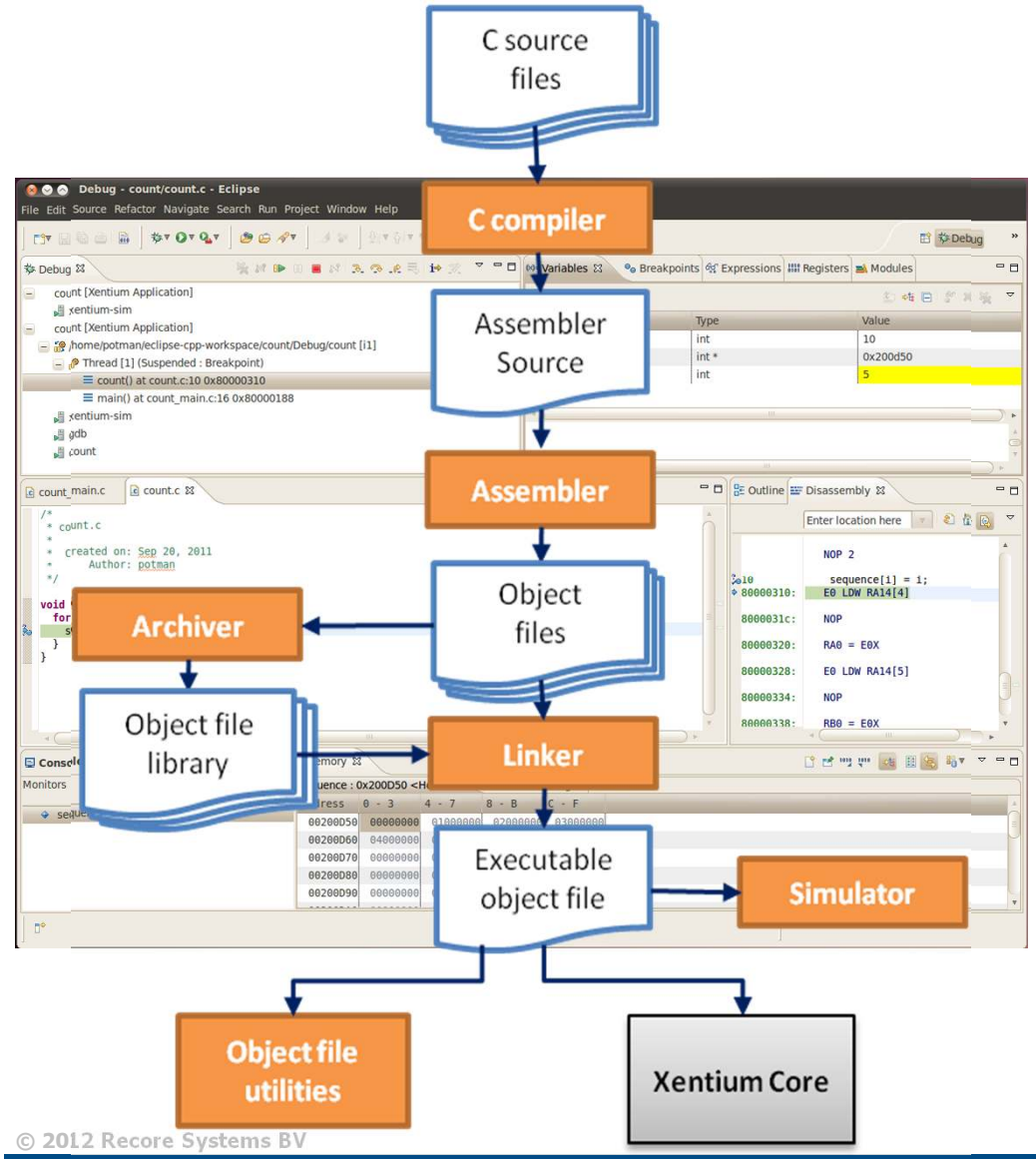
Outline

- MPPB platform hardware
- MPPB / Xentium® software development

- MPPB validation & benchmarking
- MPPB FDIR
- ASIC migration & radiation hardening
- MPPB lessons learned / future directions
- MPPB demonstration
- Q&A

© 2012 Recore Systems BV

Xentium®
software development flow

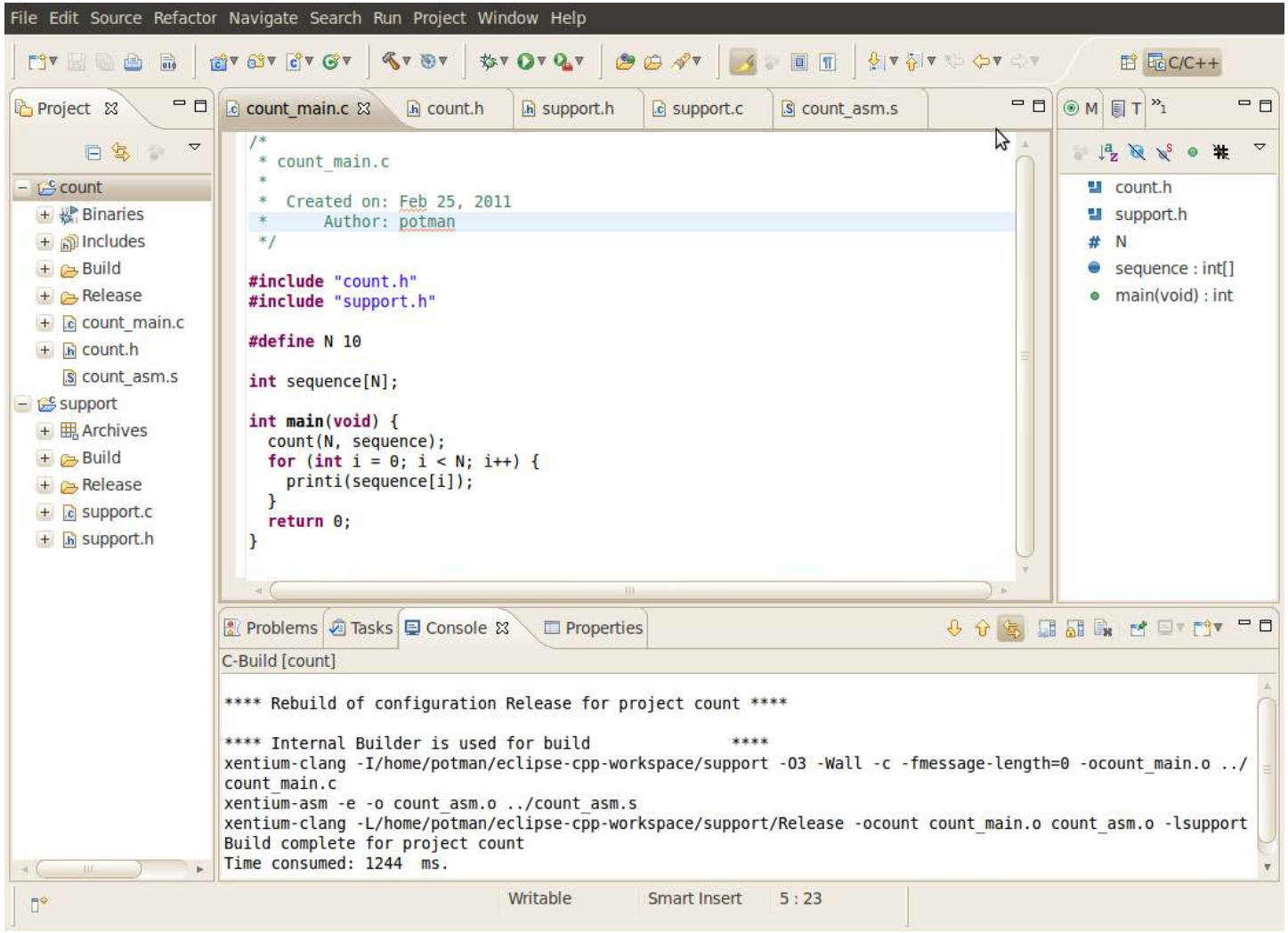


- Xentium C compiler
  - ANSI/ISO-standard C
  - Built-in functions for Xentium specific operations
  - Mix C and assembly functions calls
- Xentium assembler
  - Clean and readable
  - Extensive built-in preprocessor
  - Standard assembler directives
- Compile, assemble & link a program in a single step
- Xentium instruction set simulator
  - Trace program execution
  - Program execution cycle count
- Xentium Eclipse Plug-in
  - Integrates command line Xentium tools into the Eclipse C/C++ IDE

© 2012 Recore Systems BV

Xentium Eclipse Plug-in (1/4)

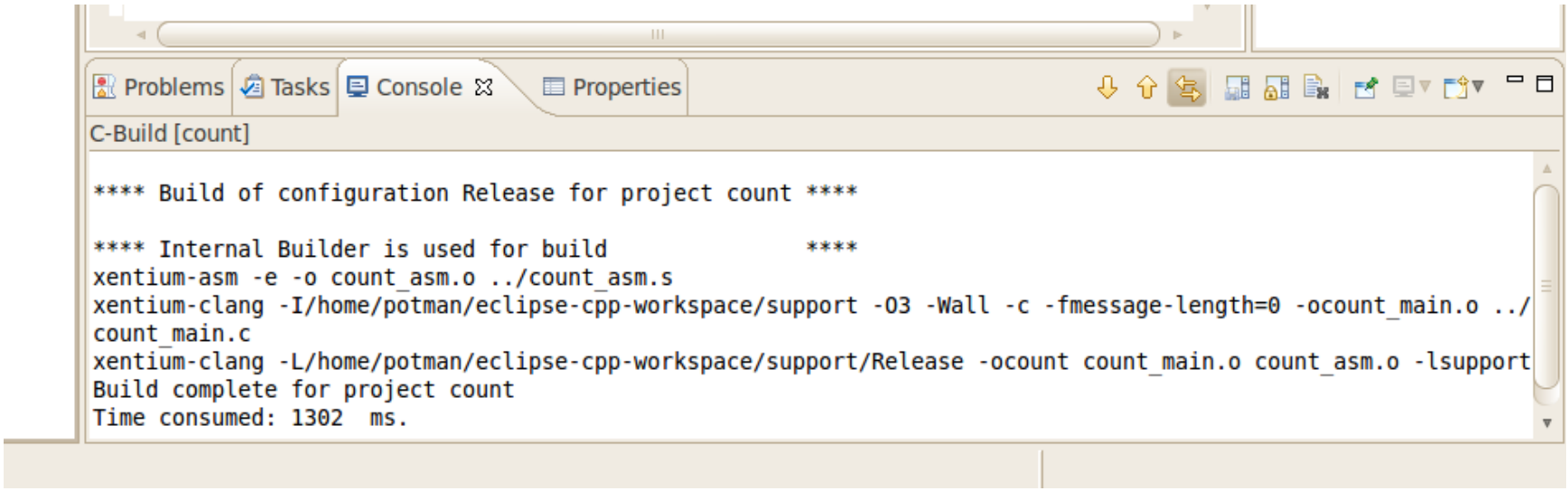
Overview



© 2012 Recore Systems BV

Xentium Eclipse Plug-in (2/4)

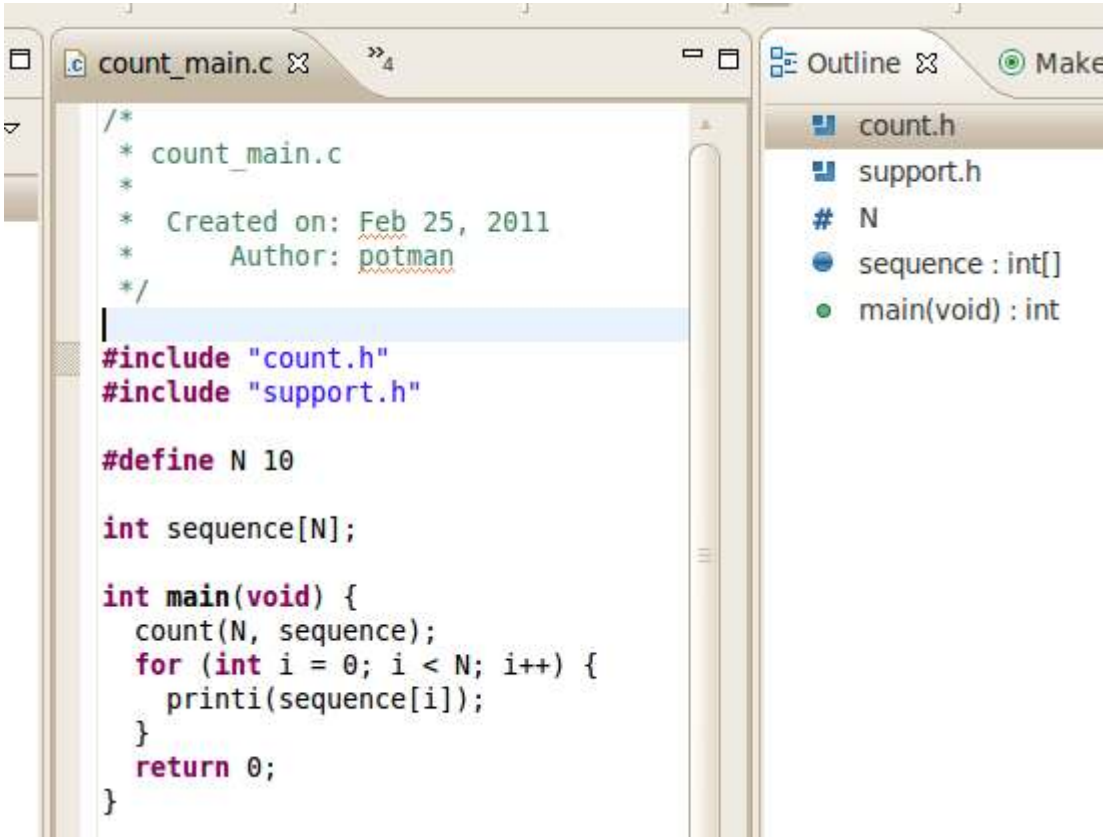
- Integrates the command line Xentium tools



© 2012 Recore Systems BV

Xentium Eclipse Plug-in (3/4)

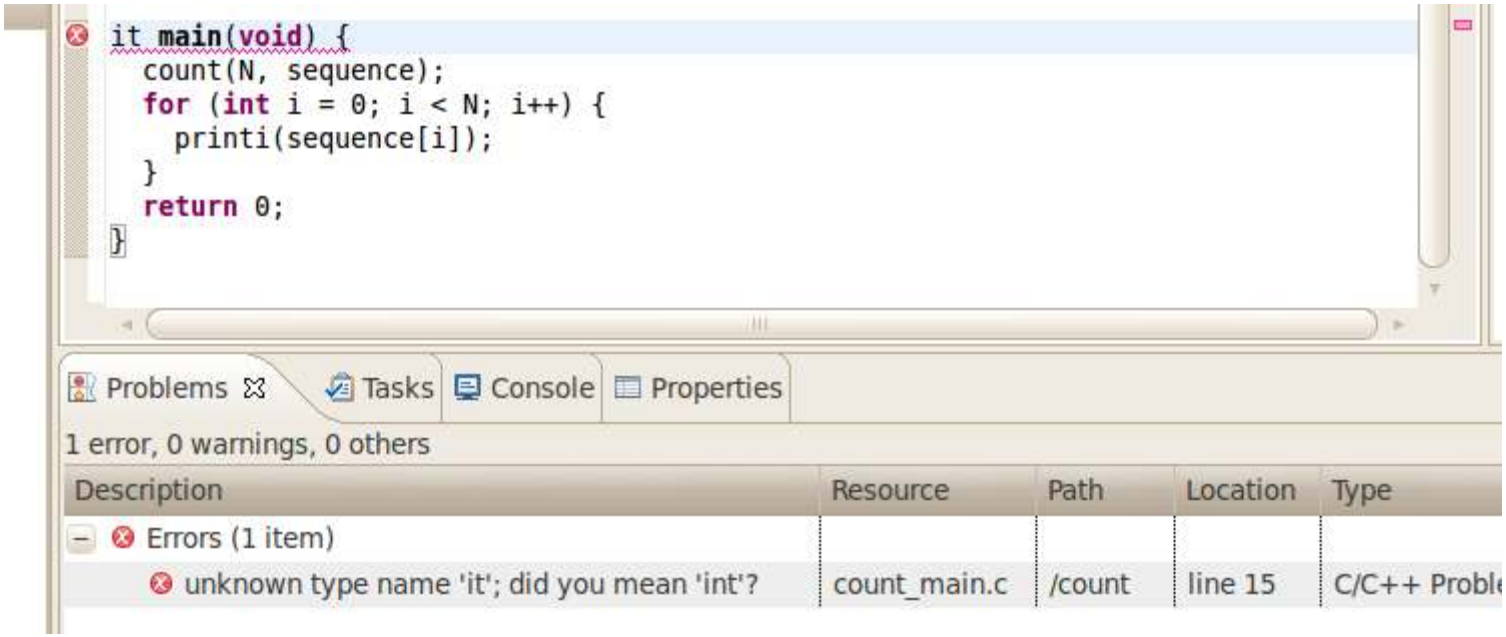
- Use features provided by the Eclipse IDE for C/C++



© 2012 Recore Systems BV

Xentium Eclipse Plug-in (4/4)

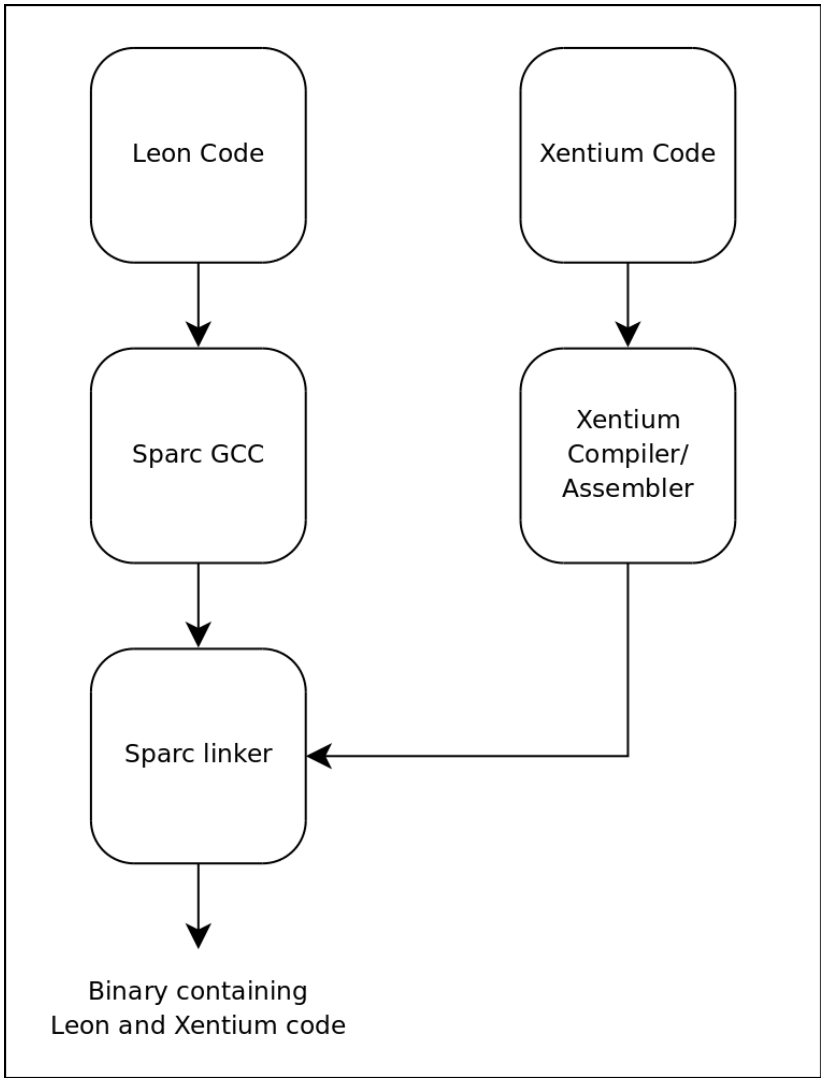
- Diagnostics support for Xentium compiler



© 2012 Recore Systems BV

MPPB software development

- Writing code
  - Leon
    - C or SPARC assembly
  - Xentium
    - C or Xentium assembly
- Compiling code
  - Leon
    - sparc-elf-gcc
  - Xentium
    - Xentium C-Compiler or Xentium assembler
- Linking code
  - Xentium binaries are linked in the Leon binary



© 2012 Recore Systems BV

MPPB Programming Scheme

- Xentium applications
  - DSP Kernel accelerators
  - Seen as tasks, started from the LEON host processor
- Xentium API
  - Implements synchronization with Xentiums
    - Communication (interrupts/mailboxes)
    - Task queuing
  - Uses DMA to copy data to/from the Xentiums

© 2012 Recore Systems BV