DSP Day - ESA Summary

DSP Day - Conclusions & Next Steps

- **NGDSP Tradeoff Study & MPPB Conclusions**
- **NGDSP: next step(s)**
- **MPPB: next step(s)**
- **Other DSP related ongoing developments**
- **Near-term new activities: SSDP**
- **Roadmap view**
- **AOB & Discussion**

NGDSP Tradeoff Study and MPPB Conclusions

NGDSP Tradeoff Study

- DSPs and their SDE's have been evaluated
- Required design modifications have been assessed, development steps identified
- Preferred candidate (ADI 21469) has been selected, discussions with IP owner have started
- Negotiations, IP licensing, and start of development depend on availability of funding

Massively Parallel Processor Breadboarding Study

- MPPB breadboard units* have been designed, tested and delivered
- Benchmark and application software have been developed
- System has been evaluated in CCN to NGDSP tradeoff study (largely positive)
- DSP IP and SDE are available from RECORE for evaluation and licensing

* ESA has 3 MPPB units available which can be provided to industry for limited timeframes to support independent test and evaluation; SDE can be licensed from RECORE b.v.

NGDSP – next step(s)

NGDSP development: how to continue

Current situation: Completion of IP licensing process and start of development depend on availability of funding

From range of potential funding sources investigated, only **ECI (European Component Initiative)** remains. The latest situation wrt ECI is as follows:

- NGDSP is on list of activities for ECI phase 4, with high priority
- Funding request is part of package to be presented at **ESA Ministerial Council (Nov 2012)**

=> National delegations need to be aware of industry's needs wrt DSP & components in general

If funding is approved,

- Discussion and negotiations for DSP IP licensing can commence and be completed
- Development of NGDSP can commence, probably in multiple steps (pre-development / main development / qualification) and with parallel threads (software / boards etc)

MPPB – next step(s)

Massively Parallel Processor Breadboarding Study: how to continue

Current situation: DSP IP and SDE are available for evaluation and licensing

In 2011 an activity called DARE+ (Design for Radiation Effects) has started, aiming at completion & bug fixing of the rad-hard (1 Mrad) 180nm ASIC design library developed by IMEC (Belgium).

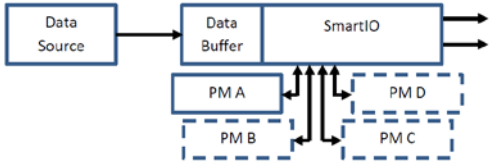
Part of the development is an “application ASIC” for test purposes which contains hardened key parts of the MPPB design (NoC routers, nodes / bridges, DSP core, memory tile etc)

⇒ **Functional prototypes expected to be available Q1 2013, with DSP & NoC elementgs running at ~100 MHz.**

⇒ **After successful test and validation of the chip, hardened DSP / NoC & related IP will be available for licensing / rad-hard ASIC developments**

Other ongoing activities – 1/4

High Performance COTS based Computer (Hi-P)



- using high performance COTS DSP - TI 6727 DSP
- modular design – SCOC3 controller and scalable # of PMs
- radiation effects (SEE) mitigated by hardware and software mechanisms

Requirements:

High-Performance CBC	
Performance	> 500 MIPS/MFLOPS in high performance mode, > 70 MIPS/MFLOPS in low performance mode available to application software. Expected: ≥ 1 GFLOPS
Reliability	> 0.8 over lifetime, recovery from transient errors in < 10 sec
Power	< 25 Watt in high performance mode, < 15 Watt in low performance mode
Lifetime	15 years, with 1000 days of high performance mode operation
Other	>3 high speed I/F, >3 low speed I/F bus interface, > 144 MB memory

Title / Type / Contractor / Timeframe / Output

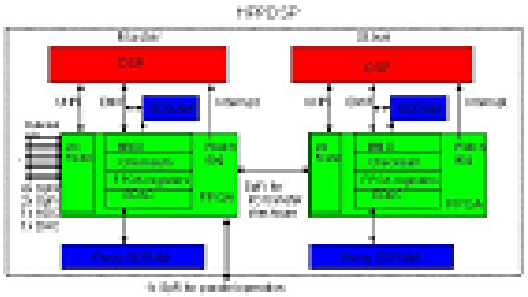
"Hi-Performance CBC", GSTP, AST-F/CGS, 2009 (Phase I) and 2011-2013 (P. II)

TRL ~5 Demonstrator, Hi-Rel SmartIO, configurable #PMs, radiation tested, BM results

Other ongoing activities – 2/4

High Processing Power Digital Signal Processor (HPPDSP)

- dedicated COTS DSP (TI 6727) based computer supporting future SRE missions
- low power, low mass among key requirements
- radiation effects (SEE) mitigated by H/W and S/W techniques
- lower power but less flexible than Hi-P



Requirements:

HPPDSP CBC	
Performance goal	1 GFLOP
Radiation performance	30 krad min.
Power envelope	< 12W total, goal 3W total, at 1 GFLOP
Communication	3 SpW, 1 Gbit I/F
Software	Re-use of commercial SDE, RTOS support
Reliability	1 SEE max per 3 days in L2, outage duration < 10 sec

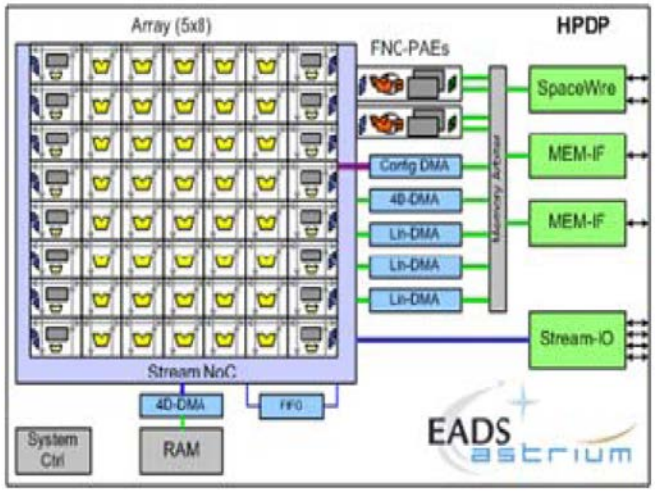
Title / Type / Contractor / Timeframe / Output

"High Processing Power DSP", CTP, AST-UK/CGS, 2010-1012

TRL ~4 breadboard (low power & mass), SEE mitigation software, benchmark results

Other ongoing activities – 3/4

High Performance Data Processor



- uses XPP reconfigurable processing core (PACT)
- 40 ALU PAEs, 16 RAM PAEs, 2 FNC PAEs
- 100 MHz target speed for ALU PAEs
- Several GOPS processing power (fixed point)
- > 1 Gbit streaming ports, SpW, DMAs, memory ports
- SDE from PACT, high level language capable
- Very good ratio of processing power / power consumption expected
- ASIC technology: STM 65nm low power CMOS (C065LP)
- addresses very high bandwidth / data streaming applications (Telecom / EO)

Title / Type / Contractor / Timeframe / Output

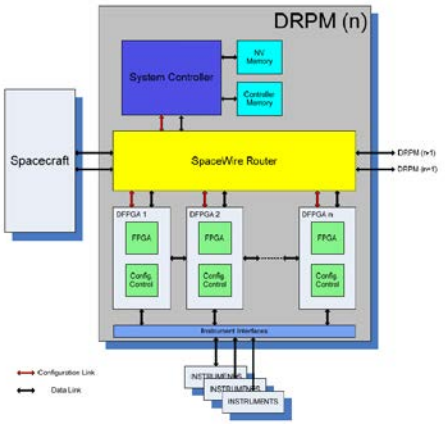
"High Performance Data Processor Prototyping", GTF, ISD / Astrium-G, 2011-2013

~TRL 4 prototype chip, SDE, demonstration software

Other ongoing activities – 4/4

Dynamically Reconfigurable Processor Module(s) - DRPM

- based on reconfigurable (SRAM-based) FPGAs
- aimed at high performance onboard data processing
- supporting partial reconfiguration
- goal is a unit that can reconfigure for any mission requirement
- chips used: Xilinx Virtex 4 and 5
- Two consortia are developing DRPM demonstrator platforms:



Consortium 1: **special attention to hardening against SEU susceptibility**

Consortium 2: **focus is put on the operational SW** for the unit; **hardware solution is envisaged to be migrated to missions Proba 3** (coronagraph DPU) and Solar Orbiter (Coronagraph DPU) -TBC

Contractor / Timeframe / Output

a) Astrium Stevenage UK / IDA, Braunschweig

b) TwT GmbH, University of Paderborn, University of Bielefeld, University of Torino

TRL 3-4 hardware expected to be available Q4 2012

Why different lines of development ?

NGDSP chip: Main goal & preferred solution but not available before 2018 even in best case

- high reliability & high performance, high productivity (SDE) and maturity, rad-hard

Gap filler: COTS based computers (Hi-P, HPPDSP): developed to be ready by ~ 2014

- Has radiation issues, but potential to complement rad-hard solutions in future

Specific solutions for Niches / special applications:

- data streaming apps in communications (HPDP), mixed signal designs, etc
- Good in their niche but too specific to provide global solution

Generic technology utililization (FPGA like in DRPM) and **R&D** (example MPPB)

- FPGA based HW: can cover niches / allow fast development; has drawbacks (power, radiation)
- R&D - technology evaluation to support decision making, keep overview, maintain roadmaps

New activity - SSDP

Scalable Sensor Data Processor (SSDP)

This activity was approved by AC and IPC earlier this year, supported by CTP funding.

Objectives (from IPC-approved AC paper)

"The objective of the proposed activity is the development of a **high performance, scalable, rad-hard** (~1 Mrad TID), highly integrated **mixed-signal** Data Processor for Sensors, Instruments, and Processing Units with excellent re-use potential for future **Science & Exploration missions**"

Deliverables (from IPC-approved AC paper)

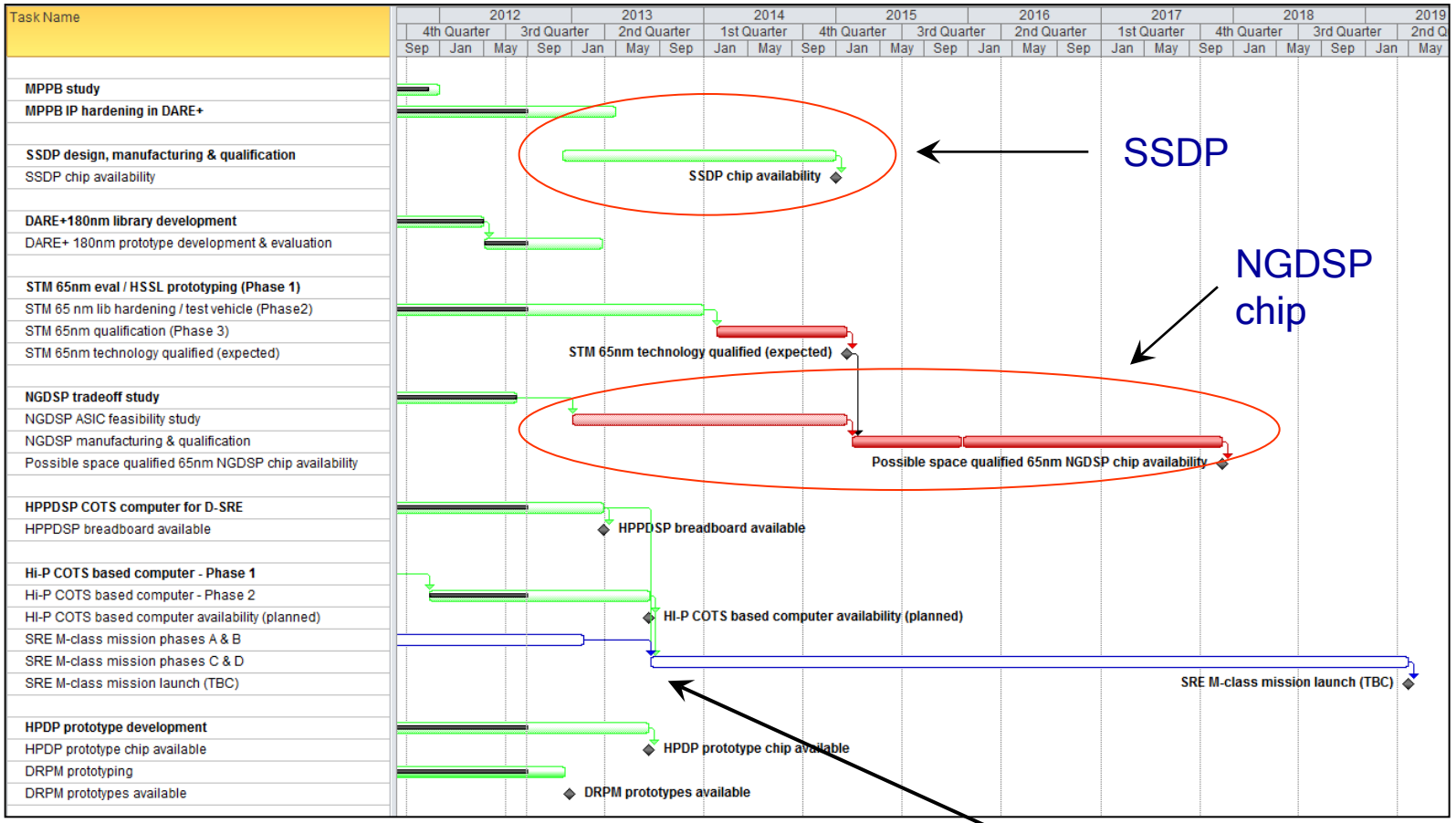
"**Packaged, functionally tested prototype chips** suitable for prototype / EM systems, instruments, and data processing units; **Software Development Environment; software library** including interface/subsystem drivers, basic DSP kernels and data processing / compression algorithms; Functional **test & evaluation boards**; Radiation test boards"

⇒ **ITT release can be expected Q4 2012.**

⇒ **ESA intends to exploit synergies and set up dedicated supportive activities to cover areas like required software development, board development etc.**

⇒ **Goal is to have SSDP Prototypes end 2014 with following qualification and FMs available ~2016 (compatible with JUICE mission timeline).**

Roadmap View & Near-term Project Needs



Today

Funding allocated

No funding allocated

No Funding allocated and expensive

TRL 5-6 need date for SRE missions

Discussion / Q & A

ESA DSP Day – The End

Thank you !

ESA presentations will be posted on TEC-EDP's
"Onboard Payload Data Processing" website:
http://www.esa.int/TEC/OBDP/SEMYHDFKZ6G_0.html

ESA & TEC-EDP wish you a good evening & safe return.