ESA DSP day

August 28th, 2012

ESA/ESTEC

ESA DSP Day – Agenda & Logistics

Time	*Agenda Item*	*Presenter*	*Participants*
9:00 – 09:15	ESA introduction – DSP Day	ESA/RT	public
09:15 – 10:45	Massively Parallel Processor Breadboarding Study (MPPB) Final Presentation – part 1	RECORE	public
10:45 – 11:00	*Coffee break*		
11:00-12:30	Massively Parallel Processor Breadboarding Study (MPPB) Final Presentation – part 2/demo	RECORE	public
12:30-13:30	*Lunch*		
13:30 – 15:30	NGDSP Tradeoff Study Final Presentation	ASTRIUM	public
15:30 – 15:45	*Coffee break*		
15:45-17:00	FP7 DSPACE project summary	DSPACE consortium	public
17:00 - end	ESA summary / public discussion / AOB	ESA & participants	public

* WLAN access: Login/pwd for ESA public network access is available - pick a sheet

Overview

- **Digital Signal Processing for Space Applications**
- **Consolidated Development Routes**
- **Today's Final Presentations**

Digital Signal Processing for Space Applications

The need for on-board processing power has been increasing in the past and will do so for the forseeable future. This is recognized by ESA, industry, and other users of space systems and applications. There is consensus that a powerful next generation DSP chip is needed to address current and future requirements.

ADCSS 2007 => NGDSP round table has been held with strong industrial participation

Report available at ADCSS07 website: "Next Generation Processor for On-board Payload Data Processing Application ESA Round Table- Synthesis, TEC-EDP/2007.35/RT, October 2007"

Key NGDSP requirements have been established:

1 GFLOPS processing power (~factor 20 improvement wrt. today's available technology)
rad-hardened design, EDACs, space specific / high speed IF
ITAR free IP and processor, high quality SDE

NGDSP Development Options

7 development options that could address the DSP processing needs of the space community were identified and presented, discussed and prioritized at ADCSS'07.

=> 4 development options remain after consolidation during the last years.

Development Routes for Payload Data Processors

The following main payload data processor development routes remain today:

Hardening of a COTS DSP against radiation effects on board / software level

- Does not depend on other technologies such as ASIC DSM
- Potentially fast route to performant processor boards
- Problem areas: Reliability, radiation hardness, complexity, mass and power

Hardening of a proven COTS DSP architecture by using a space qualified ASIC platform and transparent modifications

- Re-use of Software Development Environment (SDE), commercial chips saves cost
- High maturity IP, SDE
- IP hardening and -cost are potential issues

Development of a multi-core DSP / massively parallel IP based processor

- High performance feasible,
- IP hardening, SDE maturity, programming are potential issues

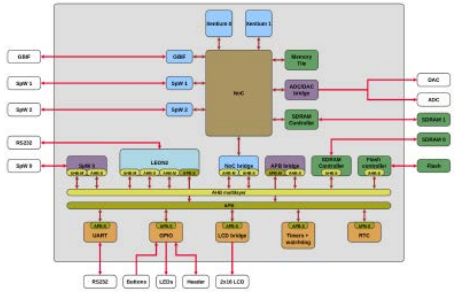
Reconfigurable FPGA based solutions

- Interesting for specific solutions, potentially fast route to flight hardware
- Problem areas: Reliability, radiation hardness, power consumption, ITAR

Today's Final Presentations – 1/2

Massively Parallel Processor Breadboarding (MPPB) Study

- Scalable architecture, GPP + fixed-point DSPs + NoC
- FPGA based prototype, LEON2 GPP + 2 DSP cores
- On-chip error mitigation possible – will be investigated



Requirements:

Platform	FPGA
Performance goal	1 GFLOP or higher on target ASIC platforms
Scalability	Highly scalable (~linear with number of cores)
Power envelope	< 10 Watts on target ASIC technology
Communication and I/F	Space standard communication interfaces, SDE interfaces, ADC and DAC I/F
Software	Commercial SDE, programmability in high level language (C) and assembly code
Target ASIC technology	rad-hard 65 nm (under development with STM), established ATMEL 180nm, or DARE 180nm

Type / Contractor / Timeframe / Output

- TRP, RECORE Systems, NL, 2009 – 2011, CCN till mid 2012
- TRL ~3 Breadboard, FPGA based, DSP SDE, SEE hardening analysis, BM results

Today's Final Presentations – 2/2

European Digital Signal Processor Tradeoff and Definition Study

- Concept: licensing & hardening the design a commercial DSP IP (like 'old' ADI 21020)
- 3 DSPs evaluated: ADI 21469, TI 320C6727, ATMEL Diopsis; + (via CCN) MPPB
- Tradeoff study to identify 1 preferred + 1 backup candidate
- Actual NGDSP development in subsequent step

Key requirements:

Performance goal	1 GFLOP or higher on target ASIC platform
Radiation performance	ca 100 Krad (Si), no SEL, design hardened against SEE
Power envelope	< 10 Watts
Communication	High speed serial links, space standard communication interfaces
Software	Re-use of commercial DSP SDE
Target ASIC technology	rad-hard 65 nm (under development with STM), established ATMEL 180nm

Type / Contractor / Timeframe / Output

- TRP, AST-F, 2009 – 2011, CCN till mid 2012
- Study Report, Tradeoff analysis, IP migration analysis & planning, benchmark results