DSPACE Project Introduction and Core Architecture

ESA DSP DAY
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The research leading to these results has received funding from the European Community's Seventh Framework Programme ([FP7/2007-2013]) under Grant Agreement n°262798

Outline

- **Project Overview**
- Design Approach
- Core Architecture
- Conclusion

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DSPACE Project

- EU FP7 Research Project
  - 2 years duration: July 2011 – July 2013
  - Total budget: 1.6 M€

- DSPACE Consortium:
  - SITAEL (project coordinator)
  - RWTH Aachen University
  - Consorzio Pisa Ricerche
  - INTECS
  - Space Applications Services

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Requirements

- Higher DSP performance required for feasibility of new space missions:
  - Earth Observation missions (e.g. processing of IR sounder and SAR instruments data)
  - Science and Robotic Exploration missions (e.g. optical navigation for descent and landing; camera image compression)
  - Telecom applications
- European strategic non-dependence for critical technologies
- Key requirements for next generation space DSP:
  - Processing power ≥ 1 GFLOPS
  - Radiation hardness (TID > 100 Krad) and protected memories (EDAC)
  - Space standard I/O interfaces
  - High quality SW Development

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Objectives

- DSP synthetisable VHDL core for space applications
  - TMR
  - EDAC
  - Synchronous/Asynchronous reset
  - Optional low power support with clock gating
- Software Development Environment including:
  - Optimized ‘C’ compiler chain
  - Instruction Level Simulator
  - SW debugger
- Benchmark Core validation

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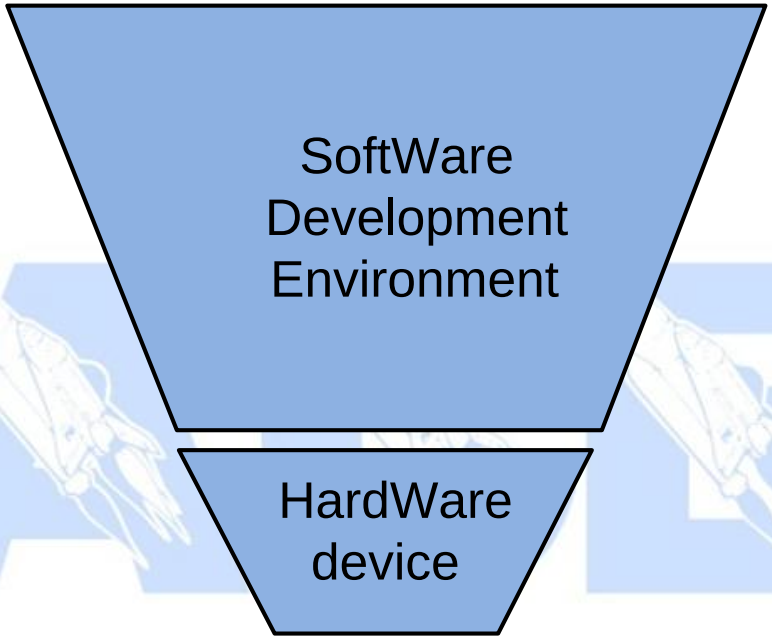
Design approach

The most demanding task of a new (Digital Signal) Processor development is the design and the debugging, of its compilation chain.



Such effort was not compatible with the DSPACE project budged.

Two expedients to manage the SW impact:

1. The exploitation of LISA methodology to automatically generate part of the SDK (assembly, linker, instruction Level Simulator ..).
2. The reuse of existing compilation chain tools combining them with a low level glue SW layer and code optimizer.

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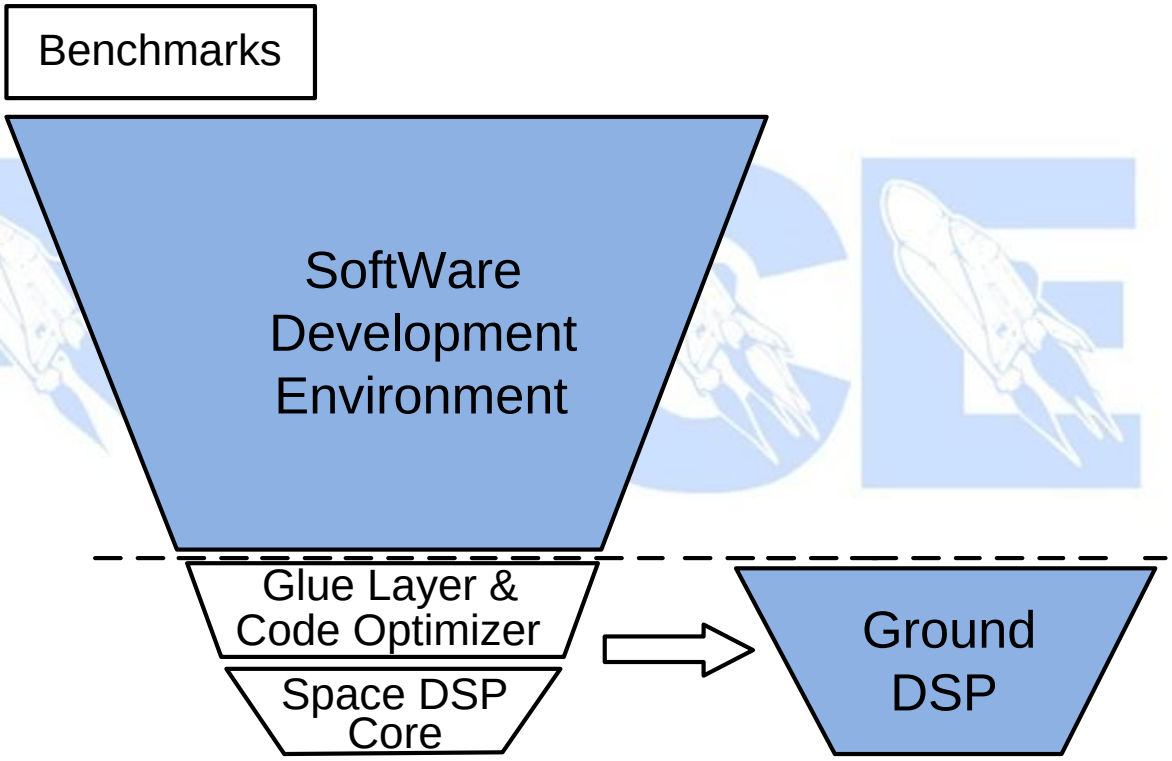
DSPACE activities

- HW design
  - Architecture definition
  - VHDL Core finalization
  - Demo Board
- SW Design
  - Glue Layer
  - Code Optimizer
  - Benchmarks
- Reuse
  - LISA VHDL, ILS, Assembler
  - Open-Source DSP optimized 'C' compiler



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Benchmarks

- Adoption of ESA DSP SW benchmarks specification

"Next Generation Space Digital Signal Processor Software Benchmark, TEC-EDP/2008.18/RT, December 2008"

- Application-oriented benchmarks
- Main kernel algorithms:
  - FIR filters, FFTs
  - Standard CCSDS Lossless Data Compression, Image Data Compression
- Benchmark code development in C and Assembly (for filters and FFTs)
- Execution for performance measurement on:
  - Cycle Accurate Simulator
  - FPGA demonstrator board

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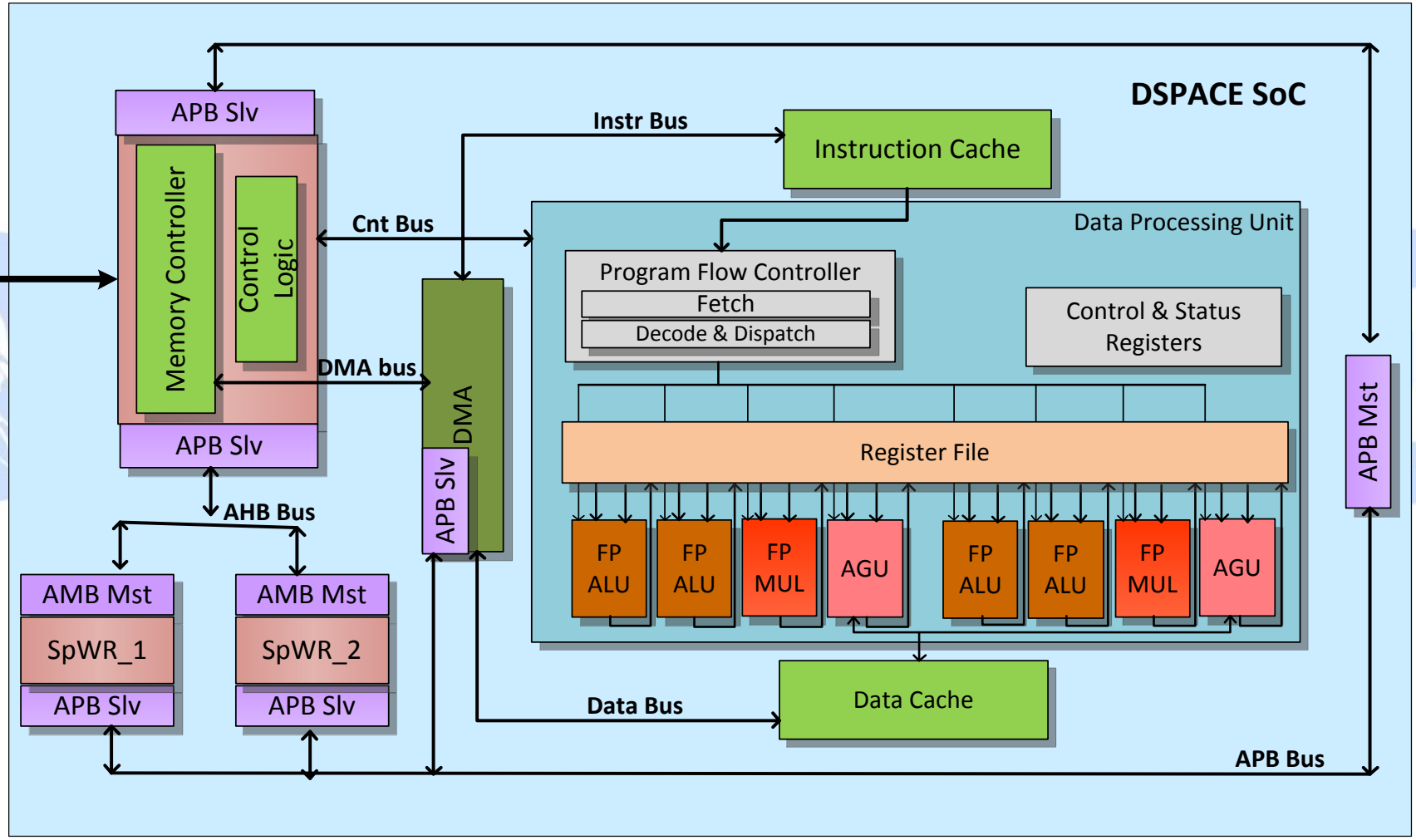
DSPACE Architecture



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Building Blocks

- VLIW 8 slot data processing unit
- Instruction Cache, 32 Kbyte + EDAC
- Data Cache , 64 Kbyte + EDAC
- DMA
- Memory controller for 72 bit ECC DDR2
- SpW-RMAP Communication modules
- AHB/APB bus

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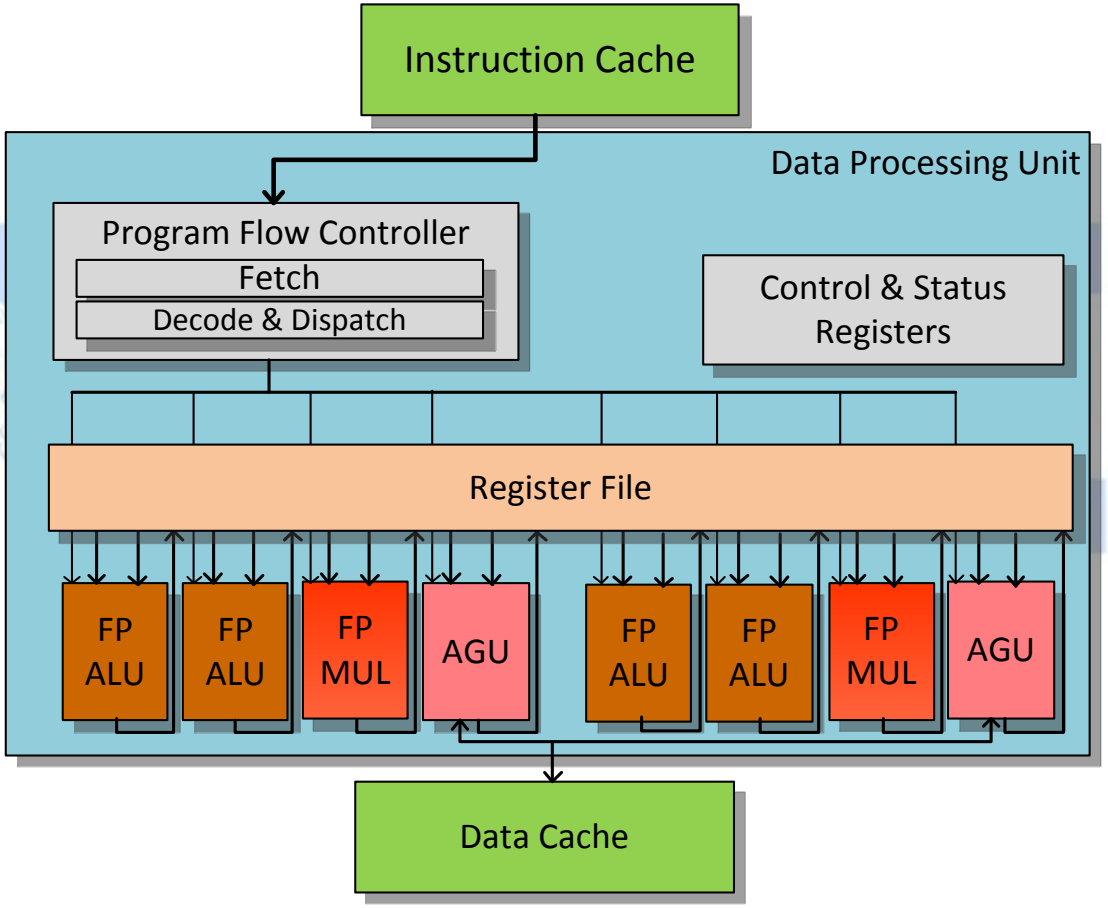
Data Processing Unit

- 8 slot VLIW with predicated execution
- parallel functional units:
  - 4 FP ALUs
  - 2 FP MUL units
  - 2 AGUs
- 64 x 32-bit Register File
- Data formats:
  - 32-bit fixed-point
  - 32-bit (IEEE 754 single precision) floating-point



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Three Different Functional Units

Functional Unit	Instruction Functionality
FPMUL: Integer and single precision FP Multiplier unit	• 32x32-bit multiply • Single-precision floating point multiplication • 16 x 16bit multiply
FPALU: Integer and single precision FP Arithmetic Logic Unit	• 32-bit logical operations • 32-bit arithmetic operations • 32-bit compare operations • 32-bit bit-field operations • 32-bit shift • Min/Max operations • Bit reversal • Trailing bit count • Single-precision floating point compare • Single-precision floating point arithmetic operations • Min/Max floating point operations • Integer / floating point conversion • Branch • Interrupt Handling • Control register transfers to/from register file • Input / Output transfer to/from external peripherals (I/O Space)
AGU: Integer Address Generation Unit	• Load and store bytes, half-words, words and double-words • 32-bit add and sub in linear or circular address calculation • Load and store with 5-bit and 15-bit constant offset using 18 different addressing option (base + register with address post/pre modify)

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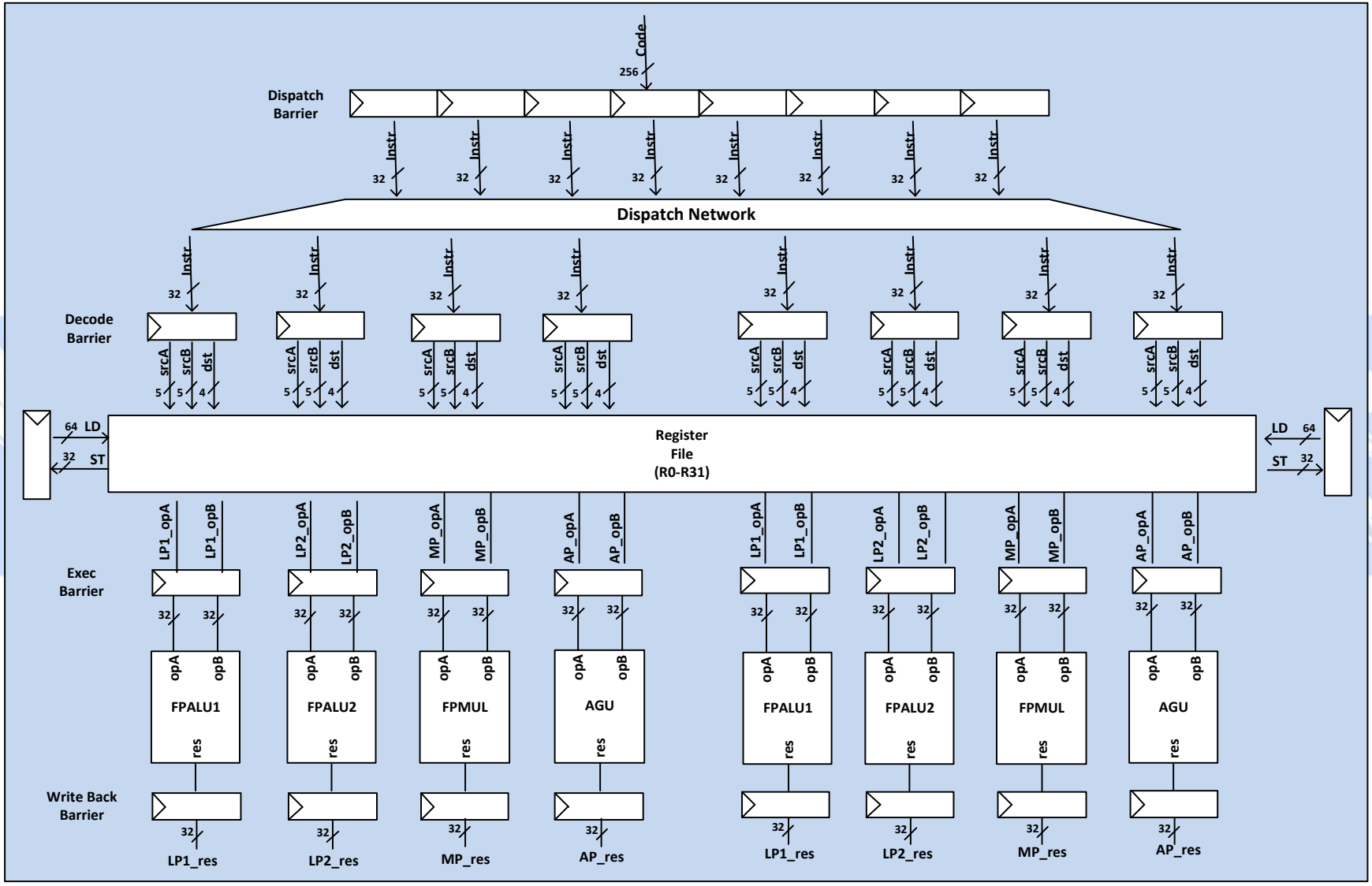

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DPU Pipeline

- Simple and scholastic HW architecture
  - Strictly pipelined VLIW structure
  - No dynamic instruction schedule, no stall management
  - Delayed branch
  - The same latency for all instructions except than LOAD/STORE/JMP
- HW specification early frozen to allow the full SW/HW integration
- HW optimization/enhancements are postponed:
  - Data forwarding (Register File by-pass)
  - Instruction Multi-latency
  - Complex operands support

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Target Technologies and Performances

- DSPACE design will incorporate radiation-hardening-by-design techniques (EDAC protection of on-chip and off-chip memories, TMR on registers)
- Atmel ATC18RHA
  - currently available, space-qualified 180 nm ASIC technology
    - ***→ expected DSP performance: 750 MFLOPS (peak) @ 125 MHz***
- ST Microelectronics DSM65
  - new space-qualified 65 nm ASIC technology (NDA signed)
    - ***→ expected DSP performance ≥ 1 GFLOPS***
- Xilinx Virtex5-QV XQR5VFX130 FPGA
  - It is the only space-qualified FPGA compatible with DSPACE features
  - A Larger Kintex7 XC7K160T/XC7K325T device has been selected for the demonstrator board

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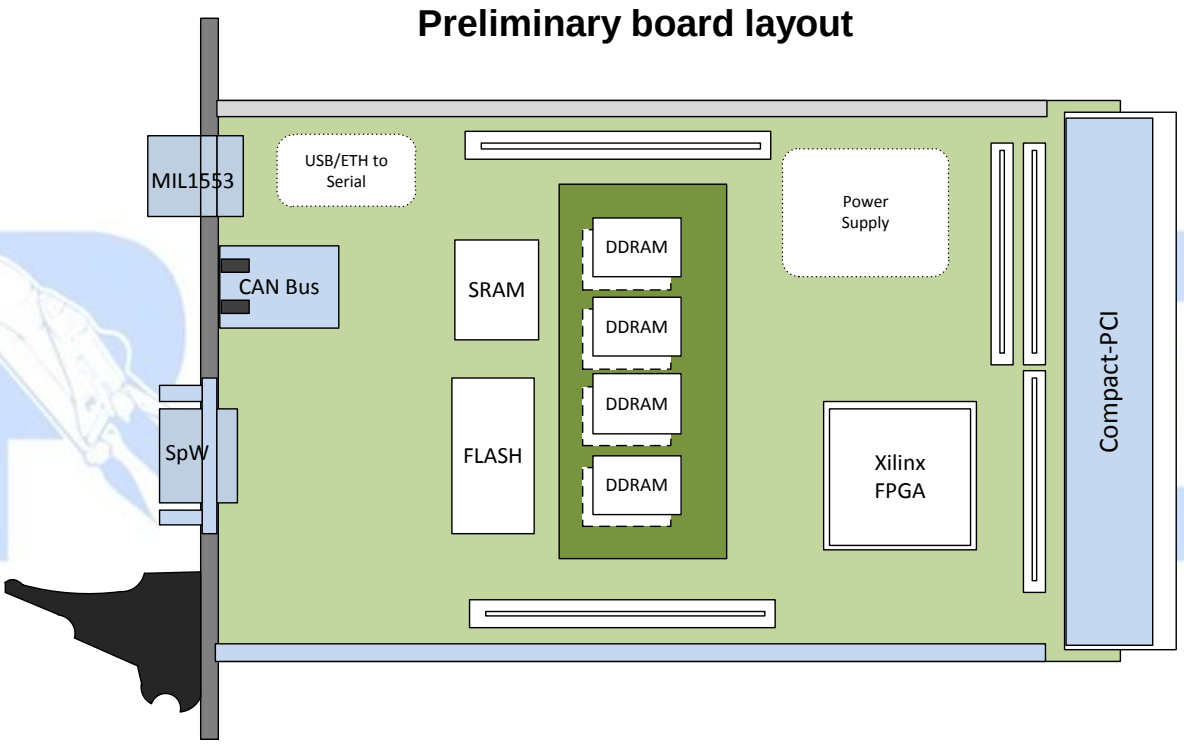
DSPACE Demonstrator Board

- Compact PCI 3U + mezzanine communication board
- Xilinx Kintex7 FPGA
- In C-PCI crates or as a standalone desktop board (with case and power adapter)
- Will be used in test and validation activities



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Conclusions

- DSPACE project aims to realize the core for a Space 1 GFLOPs DSP component providing it with a complete and reliable SDE.

- The VHDL core is complete and under test.
- Simple ‘C’ programs and Assembly test are running on the Instruction Level Simulator.
- Schedule
  - Demo board for FPGA emulation is planned in Q4 2012
  - Complete C compiler chain: Q1 2013
  - HW/SW test and benchmarking Q2 2013

- Evaluation Kit based on ILS can be released to Beta-Tester in Q1 2013

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Thank you for your attention!

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