



# Next Generation Processor for On-board Payload Data Processing Application

## ESA Round Table

October 4-5, 2007

## Synthesis

### *Purpose of the Document*

The purpose of this document is to present a synthesis of all the presentations that have been done during the ESA Round Table on the Next Generation Processor for On-board Payload Data Processing Application.

### CONTENTS

1	Background .....	2
2	Introduction .....	3
3	Overview of Future Mission Requirements .....	4
4	Overview of General NGDSP Requirements .....	5
5	Current Hardware Developments .....	6
6	Industry Opinions and Implementation Options .....	7
7	Data Processing Performance Requirements .....	14
8	Architectural, Functional, and Debug Requirements .....	15
9	Memory Support and Memory Interfaces .....	16
10	Input and Outputs Requirements .....	17
11	Software Requirements .....	17
12	Schedule Requirements .....	18
13	Summary of the Synthesis .....	19
14	Workshop Agenda .....	23
15	Reference Documents .....	25
16	Glossary of Acronyms .....	26



## 1 Background

The ESA Round Table 2007 on the Next Generation Processor for On-board Payload Data Processing Applications was held at ESTEC (Noordwijk, NL) in the frame of the ADCSS 2007 workshop on the 4-5 October 2007. The purpose of the Round Table was twofold as indicated in the Round Table Program:

- i) Review the needs of current and future missions in order to derive the requirements for the next generation of space DSPs
- ii) Review the available technology options for the implementation of the Next Generation Digital Signal Processors for deriving a development roadmap that cumulates in the availability of a new device which can satisfy the identified mission needs

For that purpose the Round Table was organized in 2 days of presentations and discussions, comprising 3 parts that reflected the process of collecting the requirements, discussing possible solutions, and an initial consolidation of the requirements:

- Part 1: Requirements and Mission needs
  - Presentation of demanding upcoming and future missions
  - Presentation of industrial DSP experience, future needs, and related studies
- Part 2: Overview of available technology options
  - Presentation of selected ongoing industrial developments
  - Presentations on use of COTS components: studies and application cases
  - Overview of ASIC processes available in the semiconductor industry
  - Data processing solutions based on IP cores
- Part 3: Discussions and Round Table Conclusions

ESA was very pleased to welcome 85 attendants to that Round Table from which 74 were representing the European space community (industry, space agencies and universities) and 11 participants from ESA side.

15 presentations were made on Day1 and 9 presentations were made on the morning of Day 2. The detailed agenda of the Round Table is attached in chapter 14 for convenience.



## 2 Introduction

The Main purpose of the first session of the Round Table was to review together with the representatives of the European space community the requirements for the next generation of Digital Signal Processors (DSPs) for space applications.

The synthesis of the presentations, intermediate and final discussions is structured according the following categories:

- *Future Mission Requirements*
- *General NGDSP Requirements*
- *Current Hardware Developments*
- *Industry Opinions and Implementation Options*
- *Data Processing Requirements*
- *Architectural, Functional, and Debug Requirements*
- *Memory Support and Memory Interfaces*
- *Input and Output Requirements*
- *Software Requirements*
- *Schedule Requirements*

The synthesis provides a summary of the most important statements presented by the participants. There are some redundancies in the statements that are presented in the following overviews; these redundant statements have been kept on purpose in order to show the importance (as well as the differences) given to some of the requirements by the participants.



### 3 Overview of Future Mission Requirements

Through the various presentations a number of diverse mission requirements were defined. In the following, general requirements and expectations are recorded, as well as quantitative requirements for parameters like throughput, data processing power and radiation hardness.

Earth Observation Mission Requirements with respect to the potential next Earth Explorer Core Missions from ESA

- *The BIOMASS SAR instrument will produce up to 270 Mbit/sec instrument data, supporting 450 Mbit/sec downlinks*
- *Spectrometers and imagers of the TRAQ and FLEX missions produce a mean data rate from 10 Mbit/sec up to 80 Mbit/sec*
- *Onboard compression shall be re-programmable, lossless compression is preferred*
- *Onboard autonomy / data selection for downlink and optional data encryption is desired*
- *Other SAR or high resolution optical instrument e.g. for the Sentinel satellites can produce data rates exceeding 1 Gbit/sec.*
- *The orbit duty cycle is there typically limited by the capability to transmit the data to the ground. An efficient data compression is essential for these systems.*

Future Mission Requirements from CNES (F)

- *Processing power up to 90 GOPS required for some applications*
- *In some applications ASICs are unavoidable, high speed ASIC technology is needed also as DSP front-end*
- *Flexibility and re-programmability in-flight are important*
- *ASICs, hybrid (IP core in FPGA + general purpose DSP) or purely IP core based options will be required*

Future Mission Requirements from ASTRIUM (F)

- *High performance is needed for radars, imagers, flexible telecom applications, navigation, security and onboard autonomy, and due to modern software development techniques (need more memory and proc power)*
- *There is a need for technology re-use / cost reduction (IP) - new technology should enforce re-usable solutions*
- *IR sounders studies for MTG indicate the need for 1-10 Gbit/sec data rate processing*
- *Some microwave payloads (SAR) are expected to generate 10-60 Gbit/sec data*
- *Re-programmability (update of lookup tables, bypassing of processing blocks etc) will be required*

Future Mission Requirements from TAS (F)

- *New earth observation missions have very high data rates at detector output*
- *Data compression is among the most demanding requirements for on-board processing*
- *For a next generation EO mission (IASI instrument) they expect 300 Mbit/sec sensor data rates*
- *Future onboard network switches will have a need for high performance DSP for flexibility*



## Science Department Mission Requirements (ESA)

The expected requirements from future science missions have not been presented during the ADCSS round tables. Instead, they were derived from a technical note [1] summarizing the predicted requirements for the Cosmic Vision 2015-2025 programme.

- *Required processing power up to 1000 MIPS / FLOPS*
- *Variable radiation hardness requirements: 100 krad will be sufficient for most missions, but specific missions will require 300 krad and above (Jupiter, Europa, missions approaching the sun)*
- *Power and mass are critical on many science missions*
- *Downlink rates up to 155 Mbit/sec, and detector bitrates up to 40 Mbit/sec are expected*

The presentation of future mission requirements provided the background for the following series of presentations and discussions, which focused more on the detailed requirements and technologies.

## 4 Overview of General NGDSP Requirements

In addition to the more specific requirements listed in the subsequent chapters, the following general requirements were mentioned during the presentations and discussions:

CNES (F):

- *For small laboratories or institutes the availability of a rad-hard, low power DSP component is very important*
- *The availability of the IP core is also important, but more for big companies*
- *Re-programmability of both hardware and software is desirable*

TAS (I)

- *DSP availability as standard product (component) for space is required*
- *Availability of a standard data processing module (board / box) is desirable*
- *DSP availability as IP core is desirable*

AAS (A)

- *Mature and efficient development tools / environments / libraries are required*
- *The availability of a real time operating system is essential*
- *Predictable software timing is very important for many applications*

In the discussion some participants stated that available processing power was in most applications more essential than low electrical power consumption. Mass was seen as a key factor. The need for a European source for the NGDSP to guarantee independent access to the technology was pointed out several times during the presentations and round table discussions.



## 5 Current Hardware Developments

A number of ongoing development activities were presented by industry. The performance and general properties of these solutions illustrated the technology gap between current and future requirements presented before.

ASTRIUM (DE) is following a number of related development / prototyping activities:

MDPA study funded under the ARTES program

- *70 MIPS class platform processor*
- *SOC with LEON2-FT, FPU, standard interfaces and DVB codec*
- *ASIC CDR 2008*

LEON Co-processor for payload data processing

- *DSP co-processor and LEON IP core implemented in FPGA technology*
- *Memory mapped interface, dedicated co-processor memories*
- *Concept provides flexibility, scalability, and higher performance for based LEON designs*
- *Need for European space qualified FPGAs with multiplier macros was identified for higher performances*
- *Advantages of standardizing a co-processor interface were discussed. PCI was discussed as a simple option.*

GAIA video processing unit

- *Off-the-shelf board from Maxwell based on PowerPC 750FX COTS CPUs, designed for space*
- *Radiation hardness is achieved on computer board level by triplication of the CPU*
- *High performance (1800 MIPS) but power hungry (33W) solution, causing thermal difficulties.*
- *Chosen because there was no alternative (time- and budget-wise)*
- *Uses additional hardware processing front-end*
- *The US export licensing has caused difficulties*

HPDP study for re-programmable data processor

- *Promising concept for a range of applications*
- *Flexible, power efficient, powerful and IP core based*
- *Phase A ongoing, Phase C/D (for transfer to rad-hard technology) shall start in 2008*

ASTRIUM (DE) explained that the hardware processing front-end for the GAIA VPU was needed because the chosen CPU was not able to do everything in SW. The COTS based approach was chosen purely due to the lack of sufficiently performant space qualified systems and components. Multiple processors are used and are re-synchronized in SW for mitigating radiation effects.

The standardization of co-processor interfaces was also addressed. Gaisler Research (SWE) recommended using the PCI bus standard.



AURELIA (I) is another company working on a versatile data processing system (IPPM):

- *LEON2-FT based payload data processor(Integrated Payload data Processing Module)*
- *100 MIPS performance class*
- *AT697 and FPGAs, multiple standardized interfaces*
- *Migration to FM in less than 1 year possible*

From the presentations in the 'current developments' session it was obvious that the ongoing developments, while being useful for specific application cases, cannot fulfil the general needs on current and future high performance data processing applications. The LEON2-FT (AT697) based designs are complementary to high performance data processors, but are not an option to solve all future needs.

The reconfigurable HPDP architecture studied by ASTRIUM (DE) was seen as a candidate for covering some specific high performance data processing needs. It was however not perceived as a generic solution to the range of applications expected on future missions.

## **6 Industry Opinions and Implementation Options**

The following sections provide a summary of the opinions voiced by major industrial players as well as the technology options and building blocks they can offer for establishing a Next Generation DSP.

### User / NGDSP System Designer Viewpoints

#### ASTRIUM (DE)

- *COTS is seen as solution only for cases where no other technology solution is available*
- *Specialized co-processors are an option in some cases, standardized interfaces are desirable*
- *A heterogeneous dual core couple (GPP + DSP) is a powerful solution but has software related issues*
- *COTS IP is preferred to a generic DSP component solution*
- *Re-programmable architectures (HPDP) are being studied and represent an interesting combination of performance, power consumption, cost, and flexibility*

#### TAS (I)

- *The flexibility of DSPs is required to cover the full future application range*
- *Additional essential components (EDAC, memory interface, etc) are important*
- *In some application cases, GPP (like the LEON3) with specialized hardware (FPGA/ASIC) is preferable*
- *Radiation tolerance > 100 krad is required*
- *Fault tolerant design is important*



- *TAS (I) indicated that low power consumption is important*
- *Radiation hardening of COTS DSPs is considered beneficial in terms of processing power, development environment; but problematic in terms of radiation hardening, inclusion of space-standard interfaces etc.*
- *Radiation hardening of a European DSP core (like DIOPSISIS from ATMEL) was considered an interesting option but maturity, growth potential, and effectiveness for target applications remained unclear*
- *The effectiveness and performance of LEON3 based solutions for payload applications was doubted*
- *Reconfigurable architectures were considered promising but their maturity was questioned*

## AAS (A)

- *Adoption of commercial DSP IP was considered advantageous, because industrial developments could start before the radiation hard component was actually available*
- *Internal memory, EDAC are required improvements over the TSC 21020*
- *The availability of commercial development tools is very important*
- *Combination of assembly language with high level language must be possible for the optimization of software performance*
- *Low interrupt overhead is important for many applications*
- *Caching like on LEON2 has an adverse effects on the predictability of execution times*
- *A real DSP is preferred over a GPP; but having one processor for both control and signal processing applications would allow to pool the efforts*

In the round table discussion the need for DSP chips, availability of the IP core and standard modules was discussed. Big companies expressed higher emphasis on IP-core availability, while small and medium companies and institutes insisted on the importance of a standard component solution. The issue of the validation of modified IP cores was discussed, as well as the difficulties of managing IP core based data processing designs for SMEs.

The problem of licensing a DSP IP only for a single manufacturing process technology (like for the TSC 21020) was pointed out and the need to avoid such limitations in future activities was emphasized.

With respect to preference of implementation technologies, TAS (I) indicated that telecom preferred IP core, science preferred a board; for miniaturized solutions the DSP component would be preferred.

On the question whether 100krad or 300krad radiation tolerance was required no preference was indicated by the round table participants, indicating that a tolerance of 100 krad would satisfy their needs.





## COTS DSP Manufacturer and User Statements

### Texas Instruments (US)

- Within its product range, TI (US) offers QML-V DSP products for space applications, most notably the SMV320C6701 devices, providing up to ~1 GFLOP, as standard products
- TI (US) uses a non-invasive radiation hardening technique by introduction of a Boron Backside Blanket Implant which significantly decreases the SEU sensitivity. This allows to reuse mask sets of the commercial devices instead of hardening the space qualified products on register level.
- Standard products are ITAR free (however specific ones may fall under ITAR)
- TI (US) standard tools for software development can be used
- In the future TI (US) will offer addition and even more advanced DSP as radiation hard components for space

The approach proposed by TI (US) was welcomed as a potential fast route to a performant DSP that could cover some of the space application areas. However, some question marks remained on sufficiency of radiation hardness, packaging qualification, and possible future US export regulation related restrictions. TI (US) stated in the following discussion that they would consider licensing an IP core to ESA.

### Analog Devices (US)

- AD (US) announced they would be willing to license the IP of one of their processors, similar to the procedure followed with the ADSP 21020
- Their current SHARC family is code backwards compatible to the TSC 21020 DSP
- SHARC provides up to 2400 MFLOPS, 32/40 bit Floating point, and multiprocessor interfaces
- AD (US) noted it would be easier for them to license the SHARC IP than the TigerSHARC IP

### CNES (F)

- *Tested COTS Blackfin DSP from AD for use on space missions*
- *Stated that performance depends strongly on use of internal memory*
- *Latch-up and SEFI tolerance investigated, further evaluation is ongoing*
- *The tested DSP may be an option for science missions in a dual redundancy architecture*

Overall, a COTS based solution was seen as a reasonable approach to fill gaps and satisfy needs that could not be served by rad-hard qualified standard products. Hardening a COTS processor board for a wider application range was not considered to be a satisfactory option, due to the varying needs and requirements of projects. EADS (DE) disregarded the wider use of the option to compensate the radiation weaknesses of COTS by using triple redundancy and similar mitigation concepts, and emphasized the need for a rad-hard qualified processor component.

Hardening an IP core acquired from a big DSP manufacturer, or the availability of a radiation tolerant version of a commercial DSP (TI) were both seen as interesting options. The approach used for the TSC 21020 was seen as a very successful one, with compatibility to a commercial device,



availability of a good development environment, the possibility to start designs years before the rad-hard product became available, and the potential of software backwards compatibility.

Industry suggested not to restrict efforts to AD (US) designs but also investigate TI (US) products with military heritage (also due to long product life cycle time), and take the best deal. The participants further noted that using an IP from a US manufacturer had to include the transfer to European technology and hardening in a European fab. CNES (F) suggested aiming for high performance processor type in order to support a long product life cycle. Participants voiced their concern that it was essential to maintain on-chip memory, and to harden it, to maintain the high performance, while keeping all hardware modifications transparent for the user and the development environment.

The use of an available (Non-ITAR) non-European rad-hard or tolerant DSP, like the TI (US) C6701, was welcomed as a possible shorter-term option for satisfying some of the user needs. TI (US) suggested to further improve the SEU sensitivity by trimming the some process parameters of existing commercial production facilities. Industry requested that ESA should assess the feasibility of such an approach. CNES (F) pointed out that the availability of such a solution was an important issue, and that a family approach for future processor availability / compatibility should be addressed.

Having a European radiation hard NGDSP product was considered very important by most participants. Despite the possibilities of using COTS components there was a wide agreement that a qualified rad hard standard component was essential.



## European ASIC Manufacturers

A number of ASIC manufacturers presented their manufacturing processes and ongoing process developments:

### ATMEL (F)

- ATMEL now offers ATC18RHA 0.18 $\mu$ m ASIC process with up to 5.5 M gates and components in QML-Q and QML-V
- Latch-up free, 300 krad, SEU hardened library
- 90 nm process under development, first tests in 2008
- Future ASIC platform could include LEON or DSP cores, FPGA blocks, etc
- ATMEL offers a 1 GFLOPS DSP/GPP combination in the DIOPSIS chip as a candidate for future space DSP, replacement of ARM GPP core by LEON3 possible

### ST Microelectronics (F)

- ST is developing 65 nm technology for space, ramp up 2008 for production
- Proposes structured ASICs with embedded processor and serialiser / deserialiser cores and customizable area
- The customisation would be performed with the top metal layers only.
- Thermal issues were discussed, package options are an issue

## Foreign ASIC Manufacturers

### Ramon Chips (I)

- RC is offering normal ASICs that are rad-hard by using rad-hard by design technology at gate level. RC is using a commercial 0.18  $\mu$ m process in combination with this dedicated libraries designed for rad-hardness.
- Products don't require a US export licence, the commercial foundries used by RC have a high availability
- Screening can be performed up to QML-V (expensive) or custom and non-destructive (electrical testing / low cost)
- Low cost screening allows factor 10 lower cost per die compared to QML-V.

In the general discussion on specific solutions for data processing based on ASIC/FPGA technology industry expressed the need for a very large European reprogrammable FPGA. Radiation hard ASICs were considered very important including a structured ASIC approach. The continued availability of a radiation hard ASIC process in Europe was considered important.

CNES (F) expressed the European need for an affordable multi project wafer service, and the need for a fast reprogrammable FPGA from a European source.



## Reconfigurable Architectures / Multi-core-processor System Designers

### PACT XPP (DE)

- *Presented XPP-III concept, using an array of Processing Array Elements (PAEs) and on-chip network with fast reconfiguration. Currently the PAE design is limited to 32 bit fixed-point, a floating point option was discussed*
- *The IP can be synthesized with rad-hard libraries, 3 MGates are expected to be required for a space version. PACT stated that for an upgrade to floating point PAEs an increase of the gate count of about 30% is expected.*

### Recore Systems (NL)

- *Presented the Montium® based reconfigurable processor which accommodates multiple heterogeneous processing cores and a network on chip (NOC)*
- *Currently fixed point only, the possibility to add space-specific I/O interfaces was confirmed*

### Clearspeed (UK)

- *Presented CSX600 array processor, with 96 processing elements, and a network on chip*
- *Is a European design licensed for space applications by BAE systems for manufacturing on a 90 nm process*
- *10 Watts, 25 GFLOPS, utilization of processors transparent to user through adapted C compiler libraries.*
- *BAE is expected to sell the chip as a catalogue product*

### Gaisler Research (SWE)

- *Presented the LEON3 SMP FT concept incorporating 4 LEON3 cores*
- *The design includes 2 AHB buses, SpW links, PCI, CAN*
- *Provides ca 500 MFLOPS, possibly up to 2 GFLOPS on 90/65 nm process and further improvements*

In the discussions following the ASIC / Processor IP sessions the possibilities for parallelizing processing tasks, and the overall need for parallel processing was discussed. Industry representatives noted that parallelization is important for efficient use of power and for increasing processing power with limited clock frequencies. The combination of memory and data processing in individual cores would allow very high processing speed at very low power.

For Leon3 SMP, but also in general, industry sees the need to invest more in development tools for designers to support software parallelization. Multi-processors were seen as helpful but the possibilities to efficiently use them were not clear.

AD (US) noted that also for their signal processors they were designing multi-core architectures. Clearspeed indicated that in many applications, like image processing, a huge amount of parallelism does exist. The suitability of the reconfigurable architectures for control processing was questioned.



It was noted that most of the proposed reconfigurable architectures did not intrinsically support floating point data and this was perceived as a significant shortfall.

In a discussion on multi-DSP IP based / reconfigurable processors, TAS (I) indicated that the efficiency, availability, and maturity of the development tools was considered essential for overall cost-effective solutions, and that the tools available for the reconfigurable processor candidates should be compared. Others noted that license costs, productivity etc. also needed to be included. Industry stated further that these architectures should be investigated for their potential in telecom applications and also for their potential in power savings. EADS (DE) stated that from their point of view these solutions were not in the same league as DSPs and a new 'traditional' DSP component was required.

A combination of GPP and DSP similar to ATMEL's DIOPSIS design was considered interesting but questions were voiced on the actual performance such a design could deliver. The lack of a set of benchmarks for comparing all these novel designs was criticised. Establishing a suitable set of software benchmarks was accepted as a general recommendation to ESA.



## 7 Data Processing Performance Requirements

Some information on the required computing performances on future missions was captured during presentations and follow-up discussions.

### 7.1 *Data format and Operations per second*

- *The use of a floating point core with double precision capability was suggested by CNES (F)*
- *CNES (F) presented applications requiring from 6 GOPS (image compression 60 Mpixels/sec with ca 100 ops/pixel required) up to 90 GOPS (1000 x TSC 21020 processing power)*
- *In discussions, TAS (I) indicated that the NGDSP should have > 1 GFLOPS to cover needs; TAS (I) is expecting the NGDSP to perform better than competitive US parts*
- *Floating point support with 64 bit was expected by TAS (I)*

### 7.2 *Data Throughput for Future Missions*

The estimations on data throughput were specified for detectors or overall instruments. The design choice to meet these requirements may therefore incorporate single or multiple processing elements. The following throughput information was presented:

- *EO SAR radars are expected to generate from 270 Mbit/sec instrument data up to extremely high rates of 10-60 Gbit/sec. ; The IASI mission (new generation EO mission, an infrared interferometer) will generate 300 Mbit/sec*
- *EO IR sounders studies for MTG indicate a need for processing data streams of 1-10 Gbit/sec; for spectrometers and imagers, mean data rates of 10 Mbit/sec/ up to 80 Mbit/sec are expected*
- *Science missions - detector bitrates up to 40 Mbit/sec, downlink rates up to 155 Mbit/sec*

During the round table discussion after the 'Requirements and mission needs' session the proposal to settle for a requirement to support floating point format was accepted. Some workshop participants recommended adopting a 64bit format despite the possible implications for memory requirements and pin-out. A minimum processing power of 1 GFLOP for a NGDSP chip appeared to be acceptable for all participants.



## 8 Architectural, Functional, and Debug Requirements

In the discussions after the presentations and during the round table sessions a number of specific architectural, functional, or other detailed technical requirements were addressed. These are summarized in the following subchapters.

### 8.1 *Basic architectural choice*

In general the discussions were focused more on the required NGDSP capabilities than on particular architectural choices. However, the following related issues were discussed and can be pointed out:

- *A general preference for a 'traditional' DSP architecture was perceived; however, it was also stated that Harvard architecture was meeting its limits in some applications*
- *Backward compatibility to TSC 21020 was considered helpful but not mandatory*
- *Reconfigurable architectures were seen with interest, but also with scepticism, and considered a niche product at this time*
- *The architecture choice should support long product lifetime*
- *Floating point support / architecture was stated as a requirement*

### 8.2 *Mono-core versus Multi-core*

The need to move to higher parallelization in order to better utilize the silicon, reduce power consumption, and increase processing speed was generally accepted. However, the participants highlighted a number of related problem areas:

- *Difficult parallelization of software and the lack of corresponding support from SW development environments*
- *Transparency of parallelization process for the user was desired*
- *The efficient integration of inhomogeneous hardware elements / cores without assembly language was considered difficult and not well supported (DIOPSIS)*
- *The lack of floating point capabilities in most presented highly parallel architectures was considered problematic and perceived as a lack of progress on these designs*

### 8.3 *Caches and On-chip Memory*

On-chip memory and Caches were also addressed. The main points were:

- *AAS (A) stated that On-chip memory was considered essential for achieving high performance*
- *Caching was suspected to cause uncertainties in execution time and was seen as a potential problem source for application timing*
- *The importance to protect the on-chip memory against upsets was highlighted by AAS (A) and others*



#### 8.4 *Memory Management Unit*

The wish for a MMU for the NGDSP was mentioned by AAS (A), but was not addressed extensively by other industrial representatives. Apparently this functionality had lower priority for a majority of the workshop participants. A MMU is of higher importance for a GPP than for a dedicated DSP.

#### 8.5 *Co-processor*

The utilization of co-processors was discussed. The implementation of dedicated interfaces found little support and a standard (PCI bus or other fast) interface of a co-processor chip was considered sufficient in terms of bandwidth and performance.

#### 8.6 *Reconfigurable/FPGA block*

No specific need was expressed for a dedicated reconfigurable / FPGA block as part of a NGDSP. However, the availability of prefabricated processing elements (such as multipliers, etc) in space qualified FPGAs was perceived as a desirable feature.

#### 8.7 *Debug support*

The need for hardware support for debugging was mentioned in multiple discussions. It was perceived as an important element for increasing productivity and for supporting efficient application development. AAS (A) pointed out that debugging support by the development tools was essential for the overall cost of a DSP problem solution.

### **9 Memory Support and Memory Interfaces**

#### 9.1 *Memory protection*

The need for EDAC memory protection was stated multiple times by various industrial attendees. Among others, CNES (F) indicated the need to incorporate an on-chip EDAC in the external memory interface in a NGDSP. ASTRIUM (DE) supported the same point of view, indicating that on-chip EDAC was essential for high memory access speed. Such a addition to the memory interface of the DSP would be a significant modification compared to the commercial DSP.





## 9.2 *Memory interface*

No specific requirements were stated on the memory interface. The requirement to connect to SDRAM / SRAM, PROM, EPROM / EEPROM memory types can be assumed. The data throughput specified for future applications certainly implies the requirements for a high speed SDRAM memory interface; Obsolescence of certain types is SDRAM memory will have to be considered. Other factors are available pin numbers and associated package size and power consumption as well as DSP architecture / instruction word size etc.

## 10 **Input and Outputs Requirements**

During the round table discussion after session 1 the support of standardized high bandwidth interfaces was pointed out, with an emphasis on the importance of standards like SpW, CAN, and possibly SpFi in future. AAS (A) indicated that high speed serial links with DMA would be welcomed. TAS (I) also indicated the desire to have integrated high speed serial links

For I/O and for interfacing to dedicated co-processors, a PCI bus I/F was recommended by several participants including Gaisler Research (SWE).

## 11 **Software Requirements**

### 11.1 *Software compatibility issues*

The issue of software compatibility was not given a high priority during the discussions. Although the possibility of NGDSP backward compatibility to the TSC 21020 was welcomed, the overall requirement of software development efficiency and affordability, which also includes multiple factors like development environment quality, debugging support, long product lifetime, availability of qualified libraries, software licenses etc, was considered most important.

Nevertheless, the investment necessary to introduce a new space DSP product in industry was recognized by AAS (A).

### 11.2 *Operating Systems choices*

While there were no specific preferences for a specific OS mentioned, the need for a real time operating system to support the NGDSP was recognized. This requirement was specifically expressed by CNES (F) and supported by AAS (A).



### 11.3 Multi-core software issues

The issue of efficient utilization of multi-core processors was acknowledged by many participants. ASTRIUM (DE) stated that good support for software development for multi-core systems was required. See also chapter 8.2.

### 11.4 Development environments

The availability of a high quality software development environment was considered essential for cost-effective product development. CNES (F) stated a preference for commercially available DSP software development tools. See also chapter 8.7

### 11.5 Software development efficiency

In addition to the availability of a high quality development environment the following points for software development efficiency were addressed by the workshop participants:

- AAS (A) stated that the need for assembly language programming must be minimized due to the related productivity problems and cost impact
- The support of efficient multi-core programming, preferably by a development environment that supports transparent optimization for multiple processing cores, was considered very important
- The need for qualified software libraries to support program development was emphasized by AAS (A)

## 12 Schedule Requirements

Due to lack of a NGDSP today TAS (I) uses either ASIC + available European processors or high performance US processors for demanding applications. For these developments the NGDSP would already be required today. TAS (I) was hoping for the availability of a NGDSP in 3 years or less, with support for more than 10 years.

AAS (A) indicated that an early availability of a solution, for example based on LEON3, might be preferred to optimum DSP solution from their point of view.

ASTRIUM (DE) confirmed the urgent need for more powerful processors and indicated their possibility to start a rad-hard implementation of their HPDP design by 2008 (with a possible availability of the chip by 2010). However, even if this development would proceed to a flight qualified component it could only cover a small fraction of the future needs.



For earth observation missions, the Phase A studies of the 3<sup>rd</sup> cycle of earth explorers will be performed in 2009-2010. Phase B will follow starting 2011. For these missions, the next generation DSP technology should be available by then.

In the round table discussions schedule needs were discussed and it was pointed out by ESA that all different options for establishing a NGDSP were also connected to different schedules, and that a combination / phasing of multiple approaches might be best to meet the needs of the users.

### 13 Summary of the Synthesis

The presentations on future missions clearly indicated the need for a next generation digital signal processor capable of handling data streams of multiple Gigabits per second.

There was an agreement that a NGDSP design needs to support **processing speeds of at least 1000 MIPS/FLOPS**, and that the **support of floating point format was mandatory**.

The **need for a European source for the product to guarantee independent access** was clearly identified and supported by a strong majority of the round table participants.

A **strong need for the provision of a space DSP application benchmark** was identified and responsibility was taken by ESA to work on a suitable set of benchmarks that would allow comparing the performances of diverse data processor designs.

In terms of radiation hardness, a **total dose tolerance of 100 krad** was considered sufficient by the participants, despite the rare need of higher hardness levels on specific science missions.

The need to have a **space qualified NGDSP chip** was confirmed by the majority of industry representatives. However, there was also an additional wish for the **availability of the NGDSP as a validated IP core**.

The availability of a **high quality development environment** was considered essential for achieving high productivity in development processes. In this respect, the obvious advantages of space-qualifying the IP core of a commercial DSP product (like it has been pioneered for the TSC 21020 in a highly successful way) were acknowledged.

Both major DSP manufacturers, **Analog Devices (US) and Texas Instruments (US)**, indicated **that they are willing to discuss licensing of one of their processors as IP cores to ESA**.



The compatibility of the NGDSP with a commercial processor, or with the previous generation of space DSPs, was seen as helpful but not mandatory.

**Multi-core architectures were seen as the general way forward** for general processor development. However, in this respect the **lack of support for multicore software development and software parallelization** was acknowledged.

The **need on on-chip memory and on-chip EDAC support for the external memory interface** of the NGDSP for achieving high processing speeds and reliability in view of external memory devices was acknowledged.

For data I/O, the **compatibility with established interface standards**, in particular with SpW, SpFi, PCI etc was emphasized.

The requirements for interfacing to space qualified external memory types and devices are considered identical to those for GPP processors (see [2]).

**The need for processing power in the NGDSP performance class exists already today.** A number of specific identified routes to a NGDSP, each one with its own associated implementation timeframe, difficulties, costs, and limitations, were discussed in the final round of discussions. These development options and their potential are summarized below.

**Option A: Hardening of COTS processors against radiation effects on computer board / software level**

This option was considered suitable for short term solutions and, more generally, for cases where no feasible rad-hard design solution exists. It was further noted that no such European processor source exists and that the difficulties associated to commercial components (short life cycle, changes in manufacturing techniques etc) do not permit a general solution based on this option. It was however **recommended for ESA to support the development of COTS based computer based for high performance applications on a case by case basis**, and by **supporting the characterization of semiconductor devices**.

**Option B: Hardening of COTS processors against radiation effects by using a space qualified ASIC process and transparent design modification**

The investigation of this option found strong support among participants as a result of the announcements of Analog Devices and Texas Instruments to consider licensing one of their DSP IP cores to ESA. In addition to the availability of efficient development environments and large software libraries, the potential for software backward compatibility (in the case of TSC 21020) is an additional incentive. Questions were raised on the feasibility of porting the design to a radiation hard



version (hardening on on-chip registers and memories; adding required interfaces, etc), on feasible performance, potential US export restrictions to an IP core, and on the commercial conditions. The participant's **recommendation to ESA was to investigate this option with AD and TI, targeting high performance, compatibility with the commercial device and the development tools, and analyzing the technical implications of hardening the commercial design.** Other related requirements from round table discussions are to avoid contractual limitations of the implementation to only one target process, and the provision of the validated IP core to European users.

### **Option C: Use of an available non-European rad-hard / rad-tolerant DSP**

Texas Instruments has proposed their SMV320C61XX DSPs, which are (today) ITAR free standard products, as a possibility to cover some of the needs of the space DSP users. TI uses a non-invasive radiation hardening by introduction of a Boron Backside Blanket Implant which significantly decreases the SEU sensitivity. This allows reusing mask sets of the commercial devices. It was **recommended that ESA follows the proposed design improvements and tests, and performs an assessment of these devices** in terms of radiation characteristics and availability.

### **Option D: Use of a multi-core DSP IP based processor**

A number of highly parallel European data processing architectures with interesting performance characteristics have been presented. For their use in DSP type applications in space it is essential for these designs to incorporate the capability to support floating point format. Furthermore, their performance needs to be assessed with a standardized space DSP applications benchmark (as recommended to ESA) to allow comparisons with conventional DSPs. Other required improvements include user-friendly development environments which make mapping of the software tasks to the parallel processing cores transparent to the user. **The overall conclusion was that the opportunities offered by these novel designs should be investigated further.**

### **Option E: Use of a multi-core LEON3 IP based processor**

A multi-core LEON3 based data processor offers advantages wrt. broad user base, established fault tolerance, and commonalities with space GPP processors. However, it was found that, (although the design could serve certain niche applications) neither the performance nor the architecture was particularly suited to serve the NGDSP user needs.



### **Option F: Use of a combination of LEON and multi-core DSP**

This option was focused mainly on the DIOPSIS GPP/DSP combination designed by ATMEL. The design, which could incorporate a LEON3 GPP in combination with a powerful DSP, would meet the NGDSP performance requirements. Questions were raised on the efficiency / transparency of software development tools, and the maturity of the development environment.

**It was recommended that ESA shall investigate this option together with ATMEL**, including an assessment of the development environment maturity.

### **Option G: Specific solutions based on ASIC / FPGA technology**

This last option aims at the implementation of DSP functionality by means of ASICs and (re)programmable devices. **ASICs and FPGAs** are essential devices for specialized high performance data processing steps, and flexible design techniques. **The availability of these devices, and of future reprogrammable / structured versions, is considered essential for an independent European space sector. It was recommended to ensure the availability of competitive ASIC processes and Multi-wafer project capabilities in Europe, and support work on a European very large reprogrammable space FPGA.**

The discussion of these NGDSP roadmap options and the associated recommendations concluded the NGDSP workshop.

The meeting was considered very productive and allowed a consolidation of the requirements for the next generation DSP. Based on presentations and discussions with industry and agency representatives, the available development options based of different candidate technologies were identified. ESA will further evaluate and down select these options in order to define the roadmap leading to the development of Europe's Next Generation Digital Signal Processors for space applications.

## 14 Workshop Agenda

**Thursday, 4 October 2007**

### Next Generation Processor for On-board Payload Data Processing Applications

08:30 Registration

#### Introduction NGDSP Round Table

09:00 Introduction  
*M. Suess, ESA*

#### Session 1: Requirements and Mission Needs

09:20 Overview of Future Earth Observation Missions  
*Aguirre, M.; Bensi, P.*  
*ESA Earth Observation (Netherlands)*

09:45 On-Board Payload Data Processing Requirements for Future CNES Missions  
*Remetean, E.; Moury, G.; Manni, F.*  
*CNES (France)*

10:10 Evaluations of Next Generation DSP Solutions  
*Notebaert, O.; Boleat, C.; Honvault, C.*  
*Astrium Satellites (France)*

#### 10:35 Coffee Break

10:50 Overview by Thales Alenia Space of High Power Processing Needs for Future Programs  
*Leconte, P.; Dantes, D.*  
*Thales Alenia Space (France)*

11:15 TSC21020 Application Experience Aiding Next Generation Spaceborne DSP Selection  
*Sust, M.*  
*Austrian Aerospace (Austria)*

11:40 Review of Possible Implementation Solution  
*Esposti, M.L.<sup>1</sup>; Estaves, G.<sup>2</sup>*  
*<sup>1</sup>Thales Alenia Space (Italy); <sup>2</sup>Thales Alenia Space (France)*

12:05 Round Table Discussion  
*M. Suess, ESA*

#### 12:35 Lunch Break

#### Session 2: Current Developments

13:35 HPDP - High Performance Data Processor  
*Syed, M.*  
*EADS Astrium GmbH (Germany)*

14:00 The AT697E LEON2-FT Device Integration in IPPM (Integrated Payload Data Processing Module)  
*Errico, W.<sup>1</sup>; Istad, J.<sup>2</sup>; Colonna, A.<sup>1</sup>; Bigongiari, F.<sup>1</sup>*  
*<sup>1</sup>Aurelia Microelettronica Srl (Italy); <sup>2</sup>ESA-ESTEC (Netherlands)*

14:25 MDPA - Multi-DSP/micro Processor Architecture  
*Helfers, T.<sup>1</sup>; Emam, O.<sup>2</sup>; Guyon, F.<sup>2</sup>; Rastetter, P.<sup>1</sup>; Lembke, E.<sup>1</sup>; Ried, O.<sup>1</sup>*  
*<sup>1</sup>Astrium GmbH (Germany); <sup>2</sup>Astrium Ltd (United Kingdom)*

14:50 LEON Co-processor for Payload Data Processing  
Honvault, C.<sup>1</sup>; Notebaert, O.<sup>1</sup>; Vaucher, N.<sup>2</sup>  
<sup>1</sup>Astrium Satellites (France); <sup>2</sup>Advanced Electronic Design (France)

15:15 Round Table Discussion  
*M. Suess (ESA)*

### **15:45 Coffee Break**

#### **Session 3: COTS Based Systems and Processors**

16:00 An Example of High Processing Power Payload Computer: the Gaia Video Processing Unit  
Soucaille, J.F.<sup>1</sup>; Paulet, P.<sup>1</sup>; Lloyd, C.<sup>2</sup>; Bennie, P.<sup>2</sup>; Paulsen, T.<sup>3</sup>  
<sup>1</sup>Astrium Satellites (France); <sup>2</sup>Astrium Satellites (United Kingdom); <sup>3</sup>ESA/ESTEC (Netherlands)

16:25 TI Roadmap for Space DSP  
Williger, I.; Sadeghzadeh, M.  
*Texas Instruments (Germany)*

16:50 Use of Texas Instruments' DSP in Space Programs  
Magistrati, G.  
*Carlo Gavazzi Space SpA (Italy)*

17:15 The ANALOG DEVICES General Purpose DSP processor portfolio  
Butler, P.  
*ANALOG DEVICES (France)*

17:40 Using Low Power COTS DSP: Assessment of Analog Devices Blackfin  
Remetean, E.; UMoury, G.; Manni, F.  
*CNES (France)*

18:05 Round Table Discussion  
*M. Suess (ESA)*

18:35 End

## **Friday, 5 October 2007**

### **Next Generation Processor for On-board Payload Data Processing Applications**

08:30 Registration

#### **Session 5: ASIC Processes**

09:00 RadSafe™ ASSP  
Ginosar, R.  
*Ramon Chips Ltd. (Israel)*

09:25 Space Fibre  
Parkes, S.  
*University of Dundee (United Kingdom)*

09:50 Deep Submicron AIC Platform for Space – Perspectives for use in High Performance Digital Processing Systems  
Renaud, N.  
*Atmel (France)*



- 10:15 High Perf. ASIC Platform Approach for Next Satellite Telecom Processors - Possible Application to other Processors  
*Dugoujon, L.; Aladjidi, A.*  
*ST Microelectronics (France)*

### **10:40 Coffee Break**

#### **Session 6: Processor IPs**

- 10:55 Dynamically Reconfigurable Processor for Space Applications  
*Schüler, E.*  
*PACT XPP Technologies (Germany)*
- 11:20 A Montium® Based Dynamically Reconfigurable Multi-Core for High Performance DSP Applications  
*Hevsters, P.M.; Rauwerda, G.K.*  
*Recore Systems (Netherlands)*
- 11:45 A Dynamically Reconfigurable Processor Architecture for Future Space Missions' Payload Data Processing  
*Arslan, T.; El-Rayis, A.*  
*The University of Edinburgh (United Kingdom)*
- 12:10 A high-performance, low-power, flexible platform for next-generation on-board payload data processing application  
*McIntosh-Smith, S.; Beese, T., Clear Speed (United Kingdom)*
- 12:35 Payload Processing Based on LEON3FT SMP Architecture  
*Gaisler, J., Gaisler Research (Sweden)*
- 13:00 Round Table Discussion  
*M. Suess (ESA)*

### **13:20 Lunch**

#### **Session 7: Roadmap and Conclusion**

- 14:20 Road Map for NG Processor for Payload Applications – Discussion and Conclusion  
*M. Suess, P. Armbruster(ESA)*
- 15:30/16:00 End

## **15 Reference Documents**

- [1] Requirements for [future Science Missions] data processing, Technical Note DHS-TN1-SCI-PAI, U. Telljohann, ESA-PAI, October 2007
- [2] Next Generation of Microprocessors for Space Applications - Synthesis, ESA Round Table September 11-13, A.-L. Pouponnot, September 2006

## 16 Glossary of Acronyms

Acronym	Explanation
AAS	Austrian Aerospace, Vienna, Austria
AD	Analogue Devices, US
AHB	Interface protocol for AMBA bus
AMBA	An open standard on-chip bus specification
ARTES	Advanced Research in Telecommunications Systems, an ESA activity
ASIC	Application specific Integrated Circuit
ASTRIUM	European Aerospace company (EADS subsidiary), France
ATMEL	European Semiconductor Manufacturer, France
BAE	British Aerospace (BAE) Systems, UK
CAN	Controller Area Network (bus)
CNES	French National Space Agency
COTS	Commercial Off The Shelf
CPU	Central Processing Unit
DIOPSIS	An ST Microelectronics dual GPP/DSP IP core activity
DMA	Direct Memory Access
DSP	Digital Signal Processor
EDAC	Error Detection and Correction
EEPROM	Electrically Erasable Programmable Read Only Memory
EO	Earth Observation
EPROM	Electrically Programmable Read Only Memory
ESA	European Space Agency
ESTEC	European Space Technology Centre, NL
FLOPS	Floating Point Operations Per Second
FPGA	Field Programmable Array
FT	Failure Tolerant
GAIA	An upcoming astrophysics mission, successor of Hipparcos
GFLOPS	Giga ( $10^9$ ) Floating Point Operations Per Second
GOPS	Giga ( $10^9$ ) Operations Per Second
GPP	General Purpose Processor
GR	Gaisler Research, Sweden
HPDP	High Performance Data Processor, an ASTRIUM project
I/F	Interface
I/O	Input/Output
IP	Intellectual Property
IR	Infrared
ITAR	International Traffic in Arms Regulation (US)
LEON	A SPARC compatible processor IP core
MDPA	MultiDSP microProcessor Architecture, an ASTRIUM project
MFLOPS	Mega ( $10^6$ ) Floating Point Operations Per Second
MIPS	Million ( $10^6$ ) Instruction Per Second
MMU	Memory Management Unit
MTG	Meteosat Third Generation
NGDSP	Next Generation DSP
PCI	Peripheral Component Interconnect (bus)
QML-V	Highest product quality class for chip manufacturing
RAM	Random Access Memory
RC	Ramon Chips, Israel
ROM	Read Only Memory
SAR	Synthetic Aperture Radar
SMP	Symmetric Multi Processing
SpFi	SpaceFibre
SpW	SpaceWire
SRAM	Static RAM
ST	ST Microelectronics, France
TAS	Thales Alenia Space, France / Italy
TI	Texas Instruments, US
VPU	Video Processing Unit
XPP	Extreme Parallel Processor, a design from PACT G.m.b.H, Germany