European SpaceWire Router Development – an update

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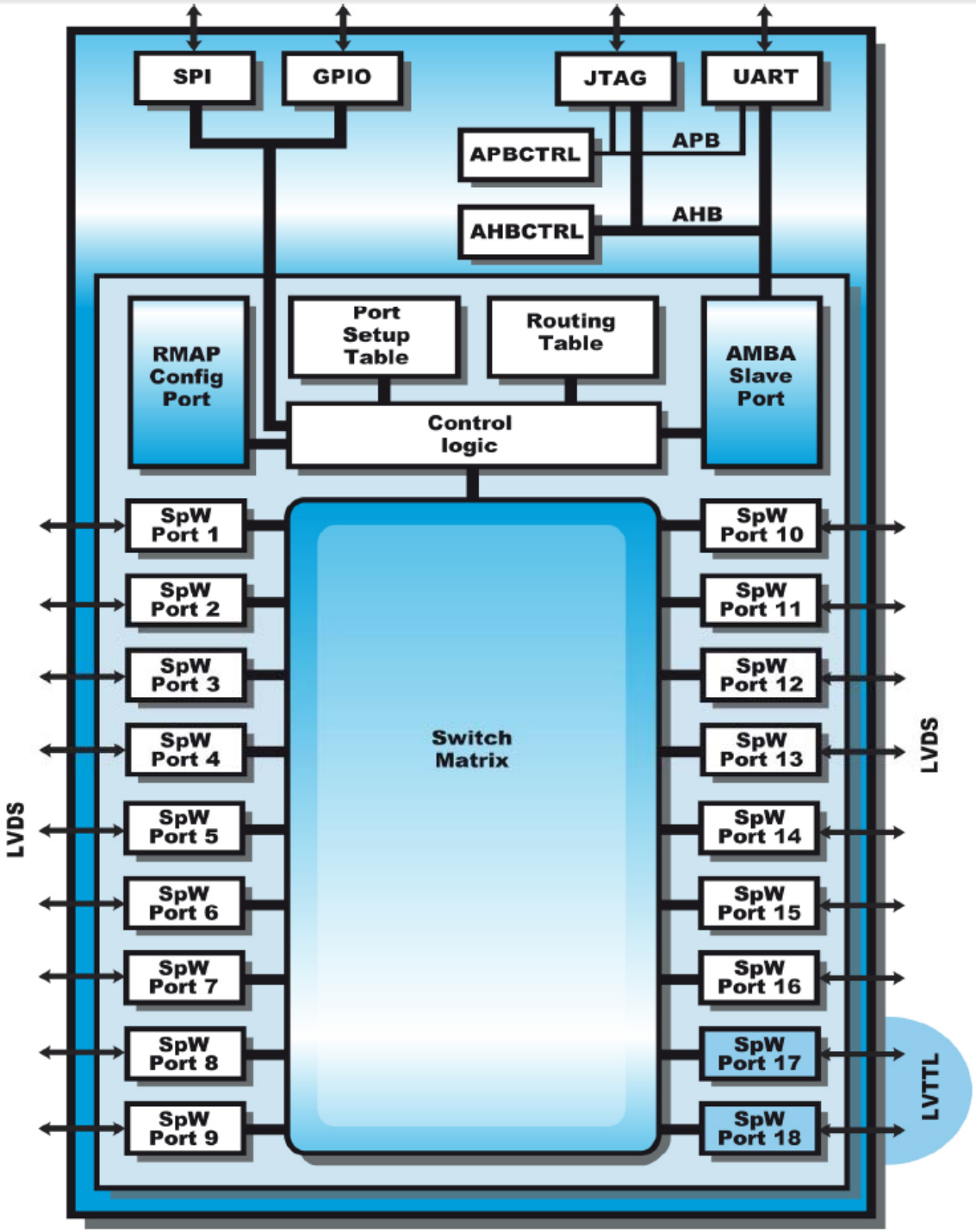
Demand for SpaceWire Router

- Both European and international customers have shown interest in SpaceWire router with greater than 12 external SpaceWire ports
- 18-port SpW router solution is useful in inter-box as well as intra-box networking allowing for topology
  - flexibility built on the ECSS-E-ST-50-12C protocol
- To meet the customer demand Aeroflex Gaisler is furthering development on a 18-port SpaceWire router ASIC
- The ASIC development is done under ESA funding

18-port Router Solution

- The 18x router is based on 180nm UMC using DARE180+ library from IMEC (BE)
- Router implements 18 external SpaceWire ports
  - 16 have on-chip LVDS
  - 2 have LVTTL interfaces to off-chip LVDS transceivers
- The full SpaceWire router architecture includes the following modules: SpaceWire Router, SPI controller, Debug UART, Debug JTAG, and GPIO
- All of these modules have been verified along the development path of the 18x router


SPI
GPIO
JTAG
UART
APBCTRL
APB
AHBCTRL
AHB
RMAP Config Port
Port Setup Table
Routing Table
AMBA Slave Port
Control logic
Switch Matrix
SpW Port 1
SpW Port 2
SpW Port 3
SpW Port 4
SpW Port 5
SpW Port 6
SpW Port 7
SpW Port 8
SpW Port 9
SpW Port 10
SpW Port 11
SpW Port 12
SpW Port 13
SpW Port 14
SpW Port 15
SpW Port 16
SpW Port 17
SpW Port 18
LVDS
LVDS
LVTTL

Development path

- Aeroflex Gaisler has established a clear path for the SpaceWire router IP core
- IP was first implemented in FPGAs for prototyping (Xilinx) [GR-RASTA-SPW16]
- Then migrated to FPGAs for flight (RTAX/RT ProASIC3) [RT-SPW-ROUTER]
- And again implemented in ASIC prototype for ESA's Next Generation Processor

- Currently an implementation of the IP core as a standalone ASIC product (18xSpW) is underway
- Each step in the development process the functionality has been enhanced

Core	Function	Vendor	Device
AHBCTRL	AHB Arbiter & Decoder	0x01	-
APBCTRL	AHB/APB Bridge	0x01	0x006
GRSPWROUTER	SpaceWire Router	0x01	0x08B
GRGPIO	General purpose I/O-port	0x01	0x01A
AHBUART	Serial/AHB debug interface	0x01	0x007
AHBJTAG	JTAG/AHB debug interface	0x01	0x01C
SPICTRL	AHB failing address register	0x01	0x02D

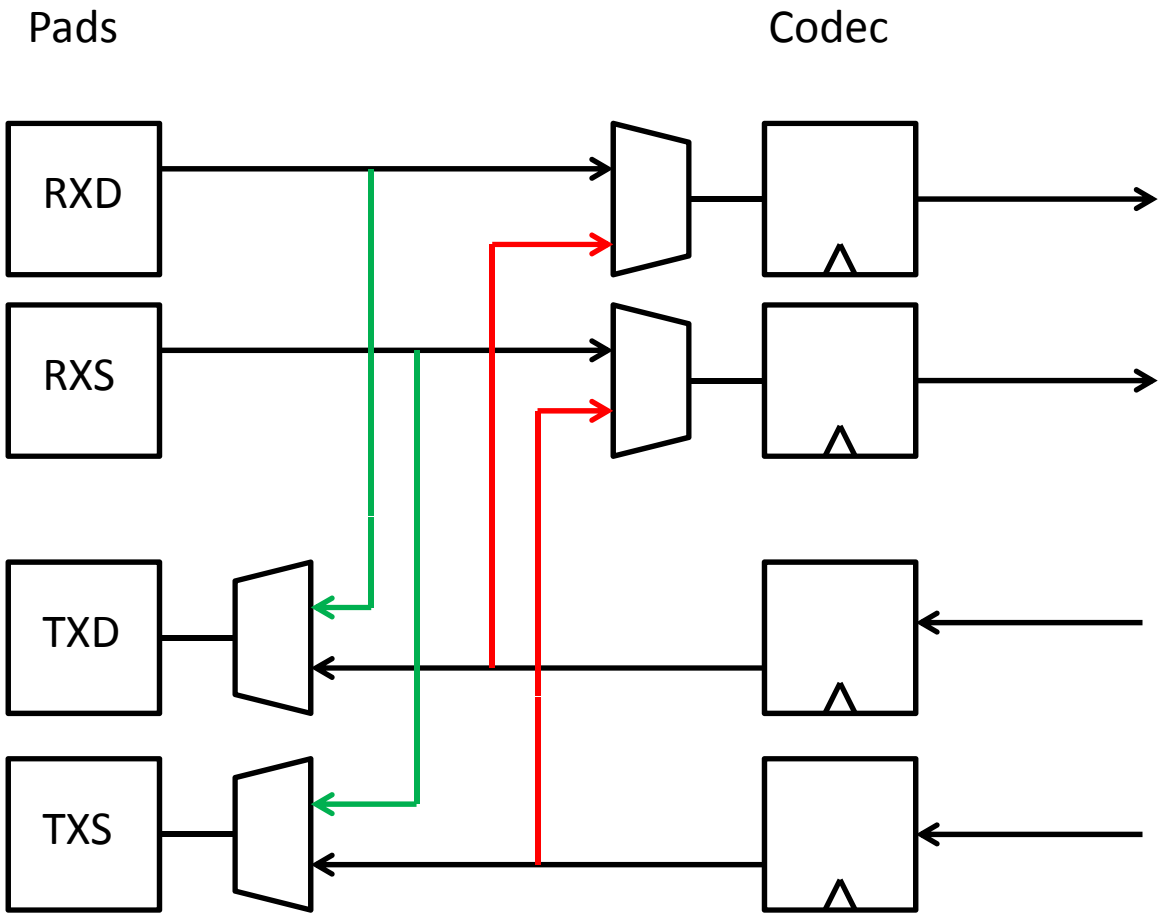
Features

- The router implements all features of a routers as specified in ECSS-E-ST-50-12C
- The router implements part of the draft ECSS Plug and Play standard
- Output port arbitration
  - Each output port is arbitrated using two priority levels with round-robin at each level
  - Each path or logical address can be configured to have high or low priority
- Group adaptive routing
- Packet distribution
  - Packet distribution can be used to implement multicast and broadcast addresses. Packets with logical address 50 can for example be configured to be transmitted on ports 1, 2 and 3 (multicast), while address 51 can be configured to be transmitted on all ports (broadcast).
- Fixed routing: address-less programmable fixed destination routing
- Timers
  - When timers are enabled during packet transmission on a port the timer is reset each time a character is transmitted. The timers use a global prescaler and an individual timer per port. Both the prescaler and the individual timer rate can be configured through the configuration port.

Features continued

- Router supports Distributed Interrupts that are being drafted for Rev. 1 of the ECSS-E-ST-50-12C standard revision (i.e. new Time-Code definition)
- Router supports future SpaceWire-D (deterministic) by providing truncation of packets due to length over-run or time-slot over-run (Time-Codes)
- Auxiliary time-/interrupt-code interface
- GPIO can be used for router configuration and external control
- SPI master interface supports external e.g. ADC for housekeeping information
- Power saving features
  - When a SpaceWire port is inactive the output LVDS driver is placed in power-down mode (outputs are tri-stated with pull-up resistors)
    - Link Disable bit is set to one (see ECSS-E-ST-50-12C for definition).
    - Link Disable bit is zero but the transmitter has not been enabled since the last time the link was disabled.
    - After reset power-down is initially activated until the transmitter becomes enabled the first time. Note that the transmitter is enabled in the started, connecting and run states.
    - Power-down is also enabled if the link is disabled due to the automatic disconnect feature.
    - Clock gating
- In-system test features
  - External and internal loop-back
  - SIST – SpaceWire In-System Test - packet generator and checker

Loop-back



Internal loop-back

External loop-back

SpaceWire In-System Test (SIST)

- Packets compatible with ECSS-E-ST-50-12C and ECSS-E-ST-50-51C
- Packet structure similar to ECSS-E-ST-50-52C, same CRC
- Packet structure:
  - SpW address (0 to 31 bytes)
  - Logical Address (default 0xFE, 254)
  - Protocol Identifier (default 0xF0, 240)
  - Transaction Identifier (2 bytes)(i.e. seed)
  - Data Length (3 bytes)
  - Header CRC
  - Data (0 to 2^{24}-1) bytes (pseudorandom)
  - Data CRC
- Programmable polynomial for pseudorandom sequence
- Can autonomously generate and check packets based on header
- Detects bit errors, packet errors, etc.
- Uses a dedicated internal port on in the routing matrix

Specifications

- Link speed: 200 Mbps
- SpaceWire clock 200 MHz
  - Drives both the receiver and transmitter in all port's codecs in the router
  - Drives a PLL from which a 1x, 2x, 4x and 8x output can be chosen for the internal SpaceWire clock network
- System clock 50 MHz
- Power consumption less than 2 W
- Package CQFP256 (previously used in GR704)
- Total Ionizing Dose > 300 krad (Si)
- Single-Event Latch-Up Immunity (SEL) LET_{TH} > 100 MeV-cm^2/mg
- Single-Event Upsets (SEU) LET_{TH} > 46 MeV-cm^2/mg
- Supply voltage 1.8 V and 3.3 V
- Screening level as per ECSS (better than MIL-STD-883 Class S)

Router configuration

- The router implements eighteen external SpaceWire ports
- Router fully supports ECSS-E-ST-50-51C SpaceWire protocol identification standard
- Mandatory configuration port provides access to configuration and status registers, and the routing table
- Configuration port 0 supports ECSS-E-ST-50-52C Remote Memory Access Protocol (RMAP) standard
- Configuration port also supports Plug and Play identification and network discovery as per draft tentative ECSS standard
- Router can also be configured through UART and JTAG debug interfaces, allowing easy connection to existing processor devices.
- Additional SIST port, configurable via UART or JTAG interfaces

Summary on 18-port SpW Router

- The latest schedule includes Preliminary Design Review held in March 2013
- Completed netlist delivery to layout on 10th of April
- Critical Design Review in end of May 2013
- Prototype manufacturing at the foundry starts in end of June 2013
- Completed prototype validation will occur in February 2014
- An evaluation board available will also be made available in February 2014 (if not earlier)

- For further information contact info@gaisler.com