ESA IP-Cores Offer

SpaceWire IPs

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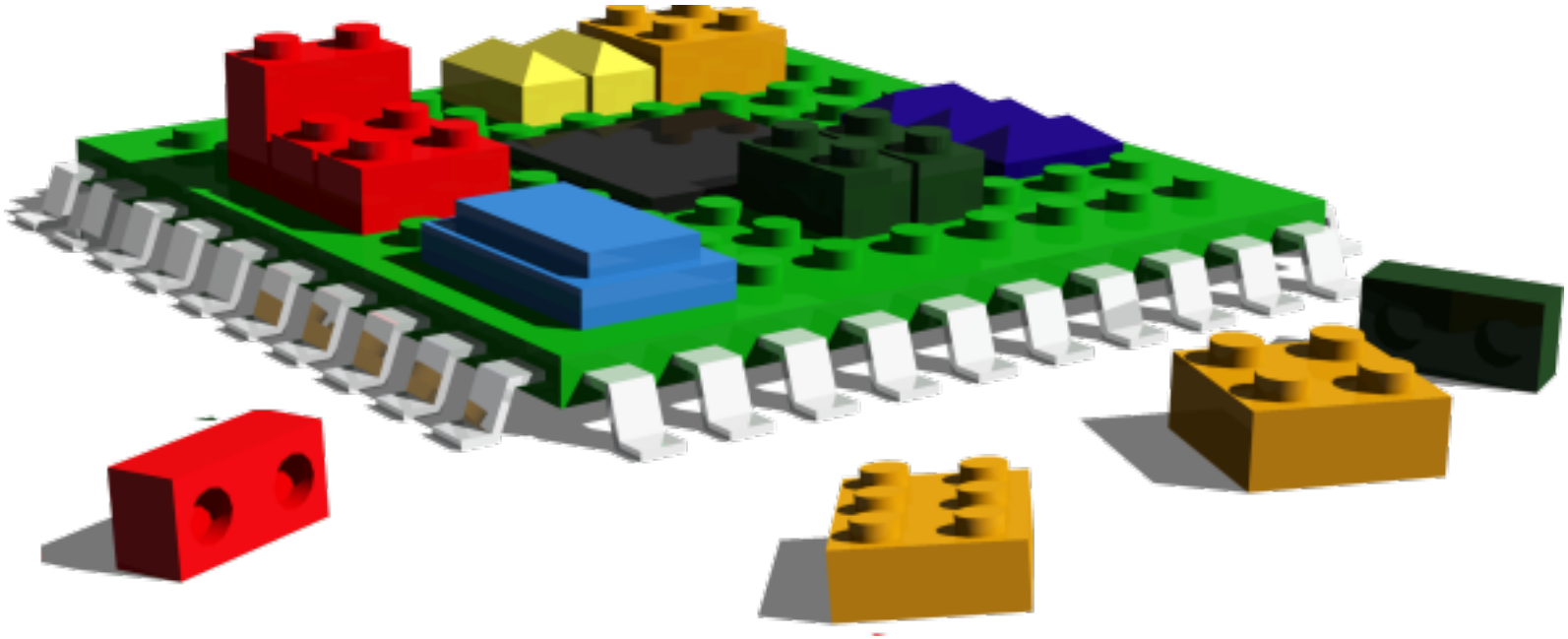
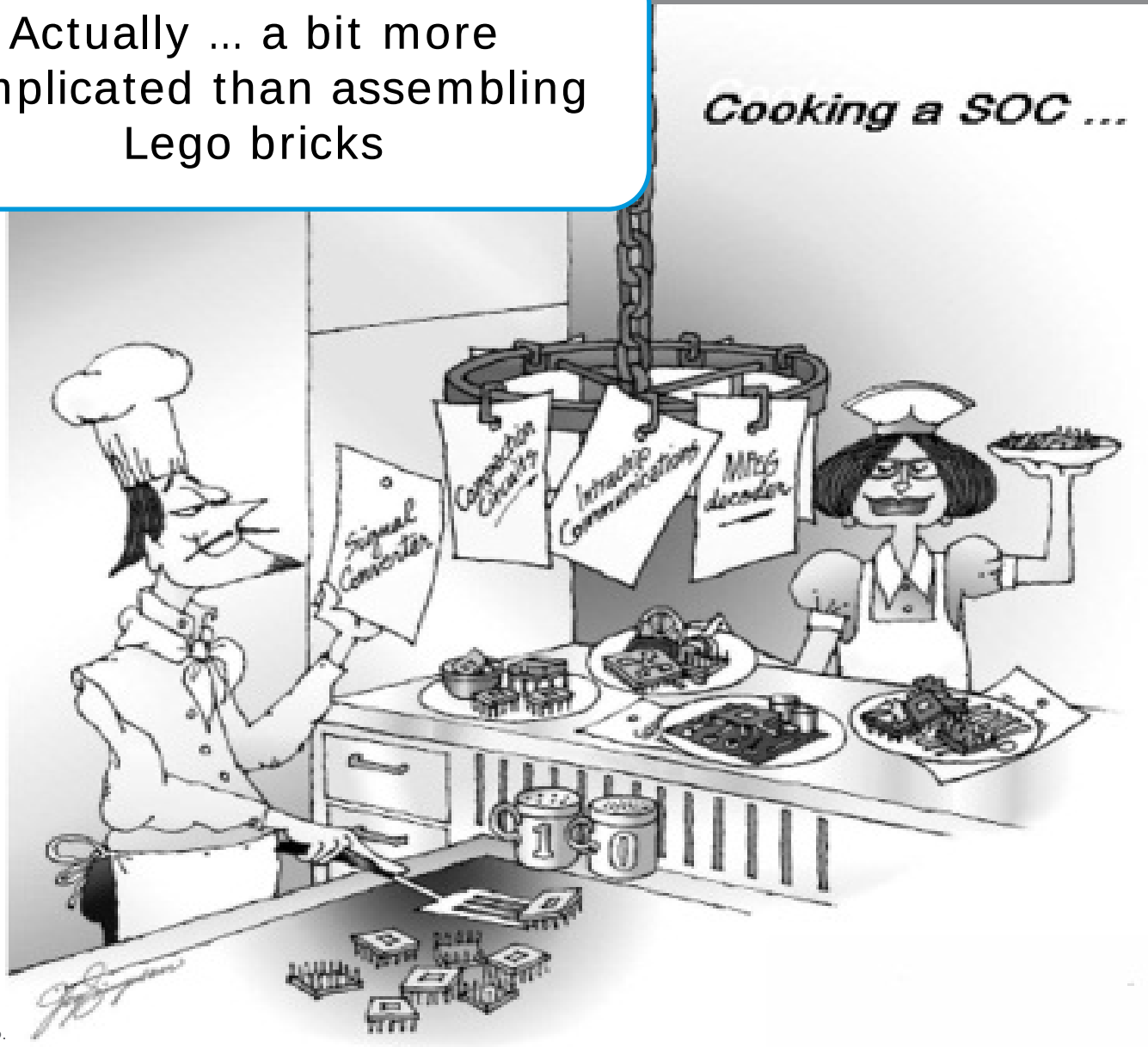
Definitions

Intellectual Property Core – *definition* *from Wikipedia*:

In electronic design a semiconductor intellectual property core, IP core, or IP block is a **reusable unit of logic**, cell, or chip layout design that is the **intellectual property of one party**.



Actually … a bit more complicated than assembling Lego bricks



Reusing Designs

- Reuse in traditional engineering is part of the standard engineering process to save time and money
  - IP-Cores are the *Building Blocks of Large Scale Electronic Designs*

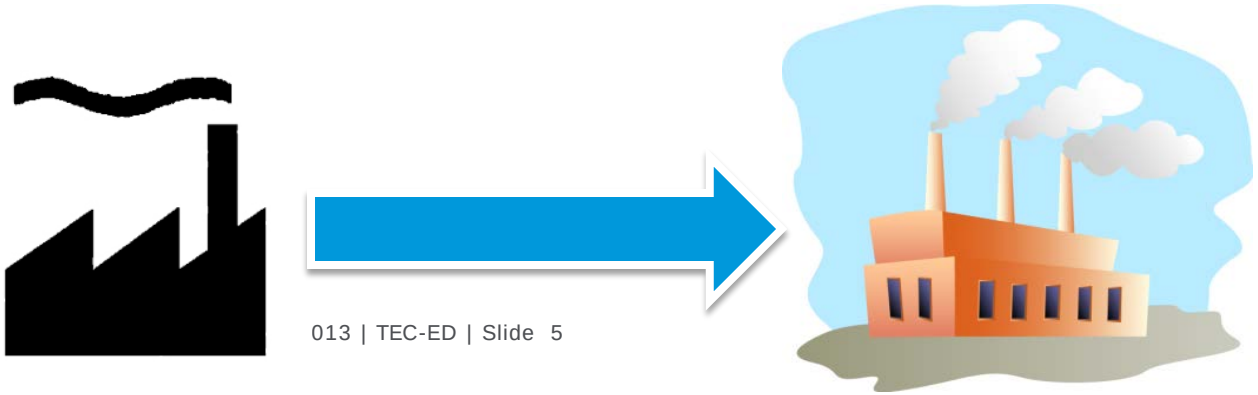
- Designing for reuse more expensive in first instance, but huge savings when reused
  - High Return on Investment for the whole space European Industry
  - Especially true for FPGA designs

- IP-Cores and Standards
  - Favor use of Standards by providing *reference designs*
  - IP-Cores as *de-facto standards*

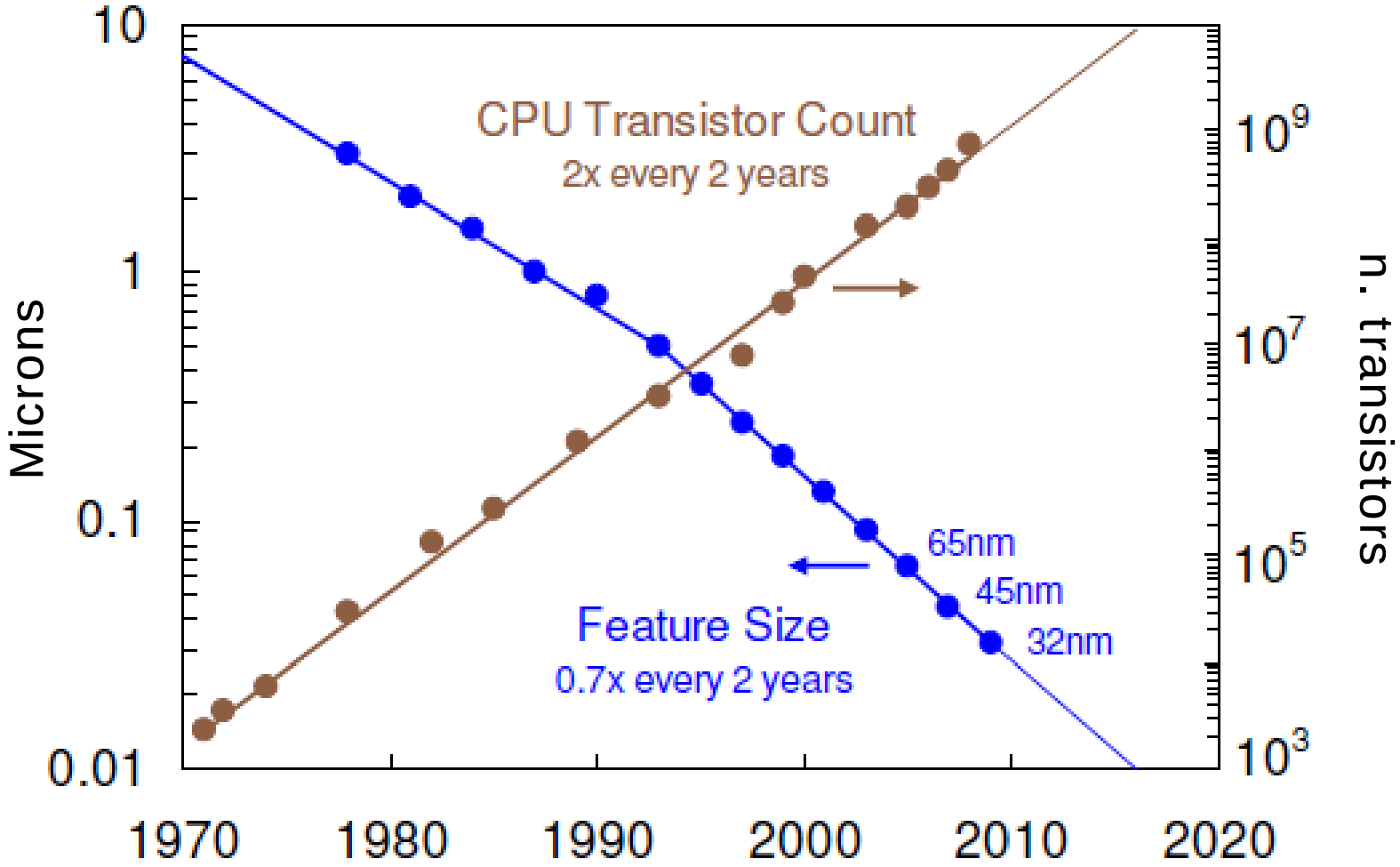
EUROPEAN COOPERATION ECSS FOR SPACE STANDARDIZATION

Securing Designs

- Counteract component obsolescence and discontinuity
  - guarantees the availability of some key functions
  - Virtually *unlimited stock*
- Facilitates Porting the design *in alternative technologies*
  - *E.g. more advanced tech*
  - Providing increased performance without the need for a redesign
- Promotes multiple sources
  - Similar, compatible components from different providers



Enabling Higher Complexity Designs



ESA IP-Cores Service
started in 2002

Role of **ESA in the IP-Core handling**:

- ✓ **Promote / Manage** their development
  - On-Going Developments (TRP/GSTP/ECI …): CCSDS File Delivery Protocol, SpaceFibre, Mass-Memory Controller & File-System, CanOpen …
- ✓ **Licensing** to European (space) Industry
  - Processing requests, producing licenses, solving legal issues …
- ✓ Providing (limited) Support
  - Answering Technical Issues, Investigations in the Lab …
- ✓ Centralize IP users' feedback
- ✓ Maintenance and Updates
  - Following the Collected feedback
  - Through contracts with Industry and internally (lab. activities)

ESA IP-Cores Service
Licensing Conditions and Procedure

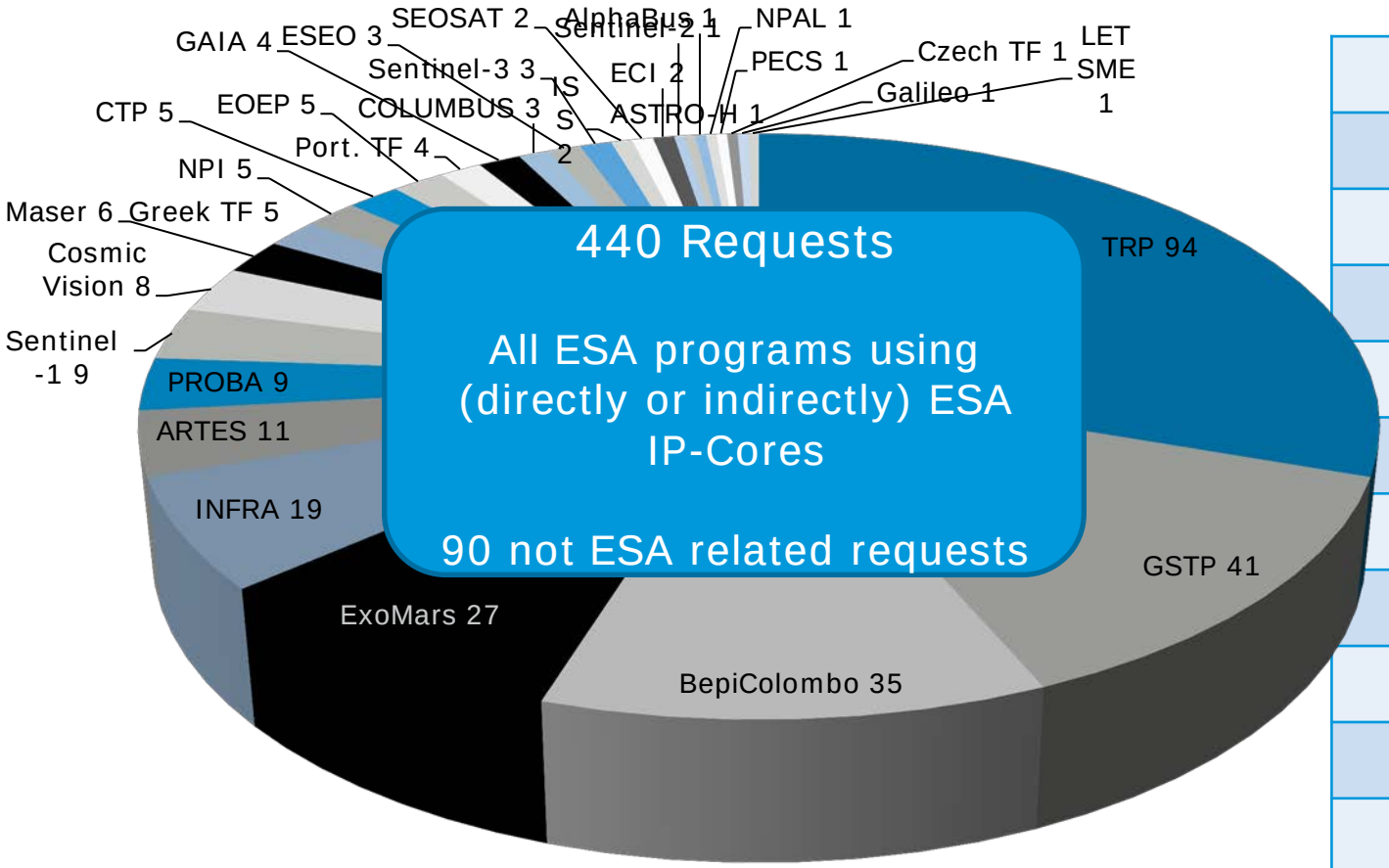
1) Complete Request Form at page: **http://tinyurl.com/ESAIPCores**
2) A License will be produced for signature by ESA and licensee
   - A CPQ is attached to the license to formalize the 5000€ handling fee
3) The requested IP-Core is delivered
   - Limited technical support is provided

✓ Each IP-Core has associated its licensing conditions
   - e.g. some can only be licensed in the frame of ESA activities

✓ A handling fee of 5000€ is associated to each IP-Core License
   - i.e. to each requested IP-Core and for each usage of it
   - See **http://tinyurl.com/ESAIPCores** for more details

✓ In some situations it is possible to obtain licenses for the use in non-ESA projects and, even, by companies not in ESA member states

Statistics - 1



TRP	94
GSTP	41
BepiColombo	35
ExoMars	27
INFRA	19
ARTES	11
PROBA	9
Sentinel-1	9
Cosmic Vision	8
Maser	6
Greek TF	5
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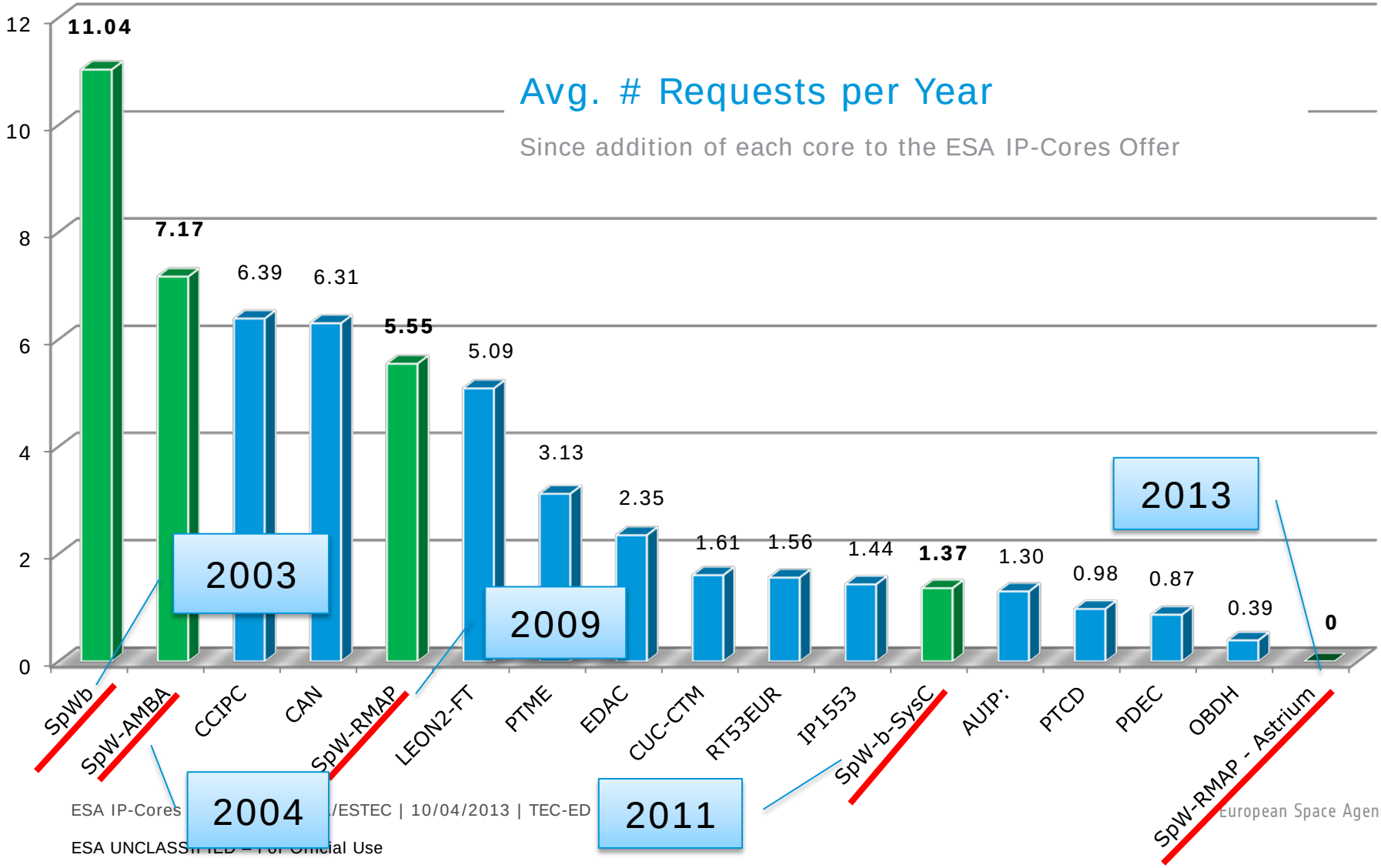
IP-core licensing to programs since 2002

Statistics - 2



SpaceWire IP-Cores

Currently Available

- 4 Synthesizable VHDL IP-Cores
  - SpaceWire-b CODEC, SpaceWire RMAP – Dundee (UK)
  - SpaceWire-b CODEC + AMBA, SpaceWire RMAP – Astrium (F)
- 1 SystemC Model
  - SpaceWire-b CODEC – Qualtek (B)

Under Development

- SpaceFibre Synthesizable VHDL IP-Core
  - Star-Dundee (UK), ESA contract – Available in 2014
- SystemC model of SpaceWire RMAP
  - Model of GRSPW2, ESA contract – Terma (D) – Available middle 2014

SpaceWire-b CODEC, Dundee

- Synthesisable VHDL implementing the SpaceWire-b CODEC
  - Produced in 2003 by the University of Dundee
  - Latest version, 2.3 from 2009
- Property of the University of Dundee/Star Dundee
  - Licensing through the ESA IP-Cores only for the use in ESA projects

    Other use-cases are served directly by StarDundee
- Extensive configuration options:
  - Tx, Rx clocks generation, DDR outputs, pipelining, etc.
- Extensively verified and used in ESA missions/programs:
  - *108 total requests* made to the ESA IP-Core service
  - Missions: BepiColombo, Gaia, JWST, Herschel, Sentinel(s), etc.
  - Present in various standard components: AT7911E, AT7912F, AGGA4, SCOC3, SpaceWire RTC (AT7913E), SpaceWire Router (AT7910E)

SpaceWire-b CODEC, Astrium

- Synthesisable VHDL implementing the SpaceWire-b CODEC with AMBA APB/AHB interface
  - Produced in 2003 by Astrium France, originally part of the SCOC activity
  - Latest version, 1.2 from 2004
- Property of the ESA
  - Licensing through the ESA IP-Cores for the benefit of the member states (and, in selected cases, worldwide)
- Limited configuration options:
  - Rx and Tx FIFO sizes
- Used in various ESA activities:
  - 63 total requests for it made to the ESA IP-Core service
  - Used in various Mass Memory, StarTracker, and EGSE designs
  - Missions ExoMars, BepiColombo, Proba, MASER

SpaceWire RMAP, Dundee

- Synthesisable VHDL implementing the SpaceWire RMAP layer
  - Produced in 2009 by the University of Dundee
  - Latest version, 1.0 from 2010
  - Includes the SpaceWire-b CODEC from Dundee
- Property of the University of Dundee/Star Dundee
  - Licensing through the ESA IP-Cores only for the use in ESA projects
- Extensive configuration options:
  - FIFOs size, watchdog, initiator and/or target, burst transfer and DMA sizes, etc.
- Used in various ESA activities:
  - 21 total requests for it made to the ESA IP-Core service
  - Missions: ExoMars, , etc.

SpaceWire RMAP, Astrium

- Synthesisable VHDL implementing the SpaceWire RMAP layer
  - Produced in 2008 by Astrium
  - Latest version from 2008, added to the ESA IP-Cores offer in 2013
  - Includes the SpaceWire-b CODEC from Astrium
- Property of the ESA
  - Licensing through the ESA IP-Cores for the benefit of the member states (and, in selected cases, worldwide)
- Limited configuration options:
  - Rx, Tx, AHB FIFO sizes
- So far used in the SCOC3 System-on-Chip and CWICOM ASIC
- No requests yet to the ESA IP-Cores service, added to the offer at the beginning of 2013

SpW-b CODEC Performance

Results taken using Synopsys Synplify Premier Auto-constrained timing optimization

XC4VLX200	LUTs	BRAMs	Max Clk Speed
Dundee	463 (0%)	0	217 MHz System Clock 362.9 MHz Rx Clock
Astrium	1806 (1%)	4 (1%)	152.0 MHz System Clock 267.2 MHz Rx Clock

A3PE3000L	Core Cells	BRAMs	Max Clk Speed
Dundee	1089 (1%)	0	77.8 MHz System Clock 111.6 MHz Rx Clock
Astrium	4792 (6%)	0	62.4 MHz System Clock 106 MHz Rx Clock

RTAX2000S	Combinatorial	BRAMs	Sequential	Max Clk Speed
Dundee	475 (2%)	0	377 (4%)	94.3 MHz System Clock 184.3 MHz Rx Clock
Astrium	2031 (9%)	0	1216 (11%)	89.7 MHz System Clock 148.9 MHz Rx Clock

SpW-RMAP Performance

Results taken using Synopsys Synplify Premier Auto-constrained timing optimization

XC4VLX200	LUTs	BRAMs	Max Clk Speed
Dundee	6246 (3%)	7 (2%)	105.2 MHz System Clock 174.6 MHz Rx Clock
Astrium	5407 (3%)	0	115.3 MHz System Clock 259.2 MHz Rx Clock

A3PE3000L	Core Cells	BRAMs	Max Clk Speed
Dundee	13967 (19%)	15 (13%)	33.3 MHz System Clock 96.9 MHz Rx Clock
Astrium	15404 (19%)	4 (3%)	40.7 MHz System Clock 106.8 MHz Rx Clock

RTAX2000S	Combinatorial	BRAMs	Sequential	Max Clk Speed
Dundee	6708 (31%)	10 (15%)	3210 (30%)	59.1 MHz System Clock 142.5 MHz Rx Clock
Astrium	6727 (31%)	3 (4%)	2567 (24%)	58.6 MHz System Clock 150.9 MHx Rx Clock

ASSPs: Link Speed

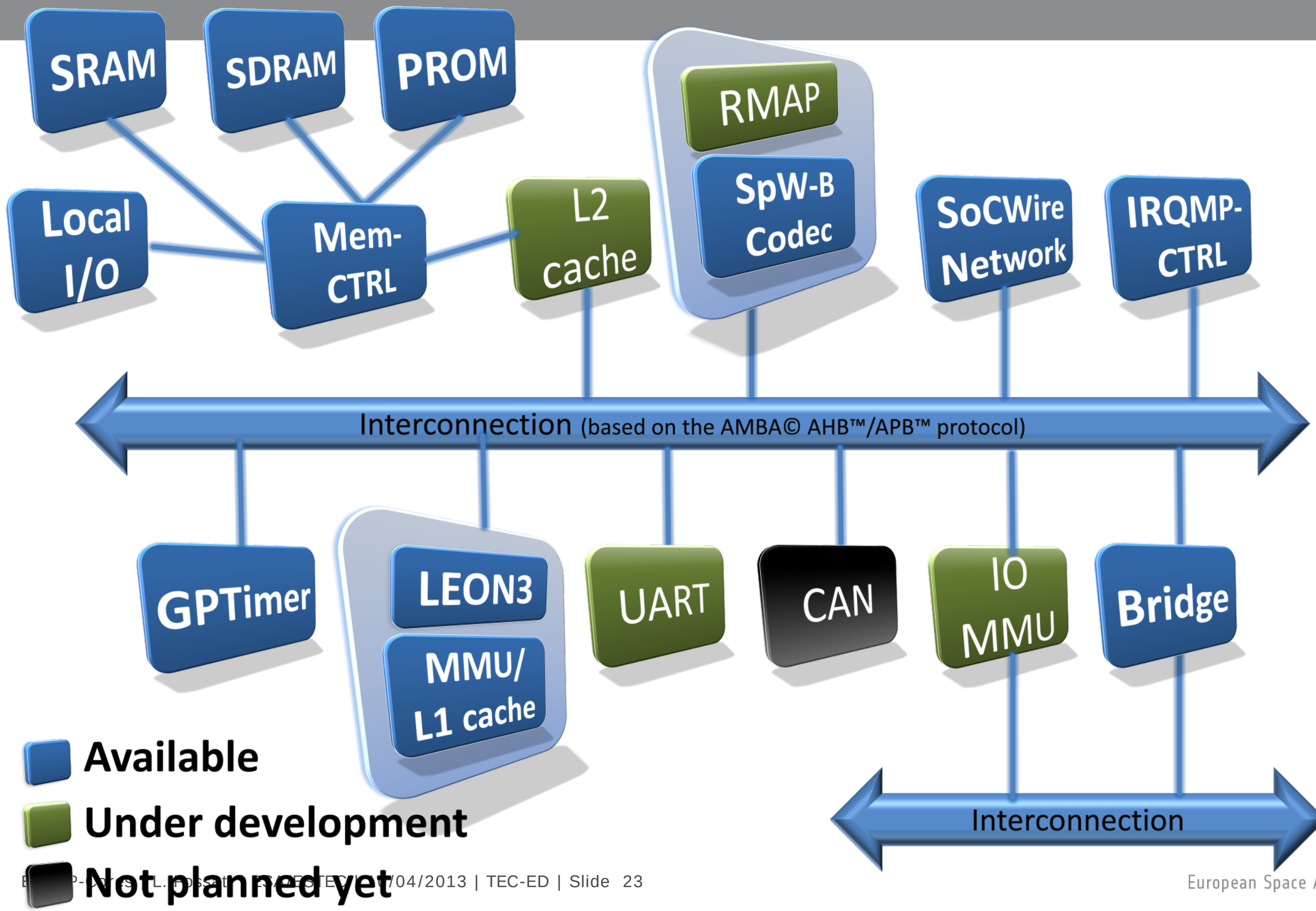
AT7911E	SpaceWire-b CODEC	Atmel MG2RT 0.5µm	200 Mbit/s
AT7912F	SpaceWire-b CODEC	Atmel MG2RT 0.5µm	200 Mbit/s
SCOC3	SpaceWire-b CODEC	Atmel ATC18RHA 0.18µm	160 Mbit/s
SCOC3	SpaceWire-RMAP, Astrium	Atmel ATC18RHA 0.18µm	160 Mbit/s
AT7913E	SpaceWire-b CODEC	Atmel ATC18RHA 0.18µm	200 Mbit/s
AT7910E	SpaceWire-b CODEC	Atmel MH1RT 0.35µm	200 Mbit/s

ASSPs: Link Speed

AT7911E	Triple SpaceWire links High Speed Controller	200 Mbit/s
AT7912F	Single SpaceWire link High Speed Controller	200 Mbit/s
SCOC3	Space Computer on a chip	160 Mbit/s
SCOC3	Space Computer on a chip	160 Mbit/s
AT7913E	SpaceWire Remote Terminal Controller (RTC)	200 Mbit/s
AT7910E	SpW-10X SpaceWire Router	200 Mbit/s

Harware Modeling: *Activities*

European Space Agency



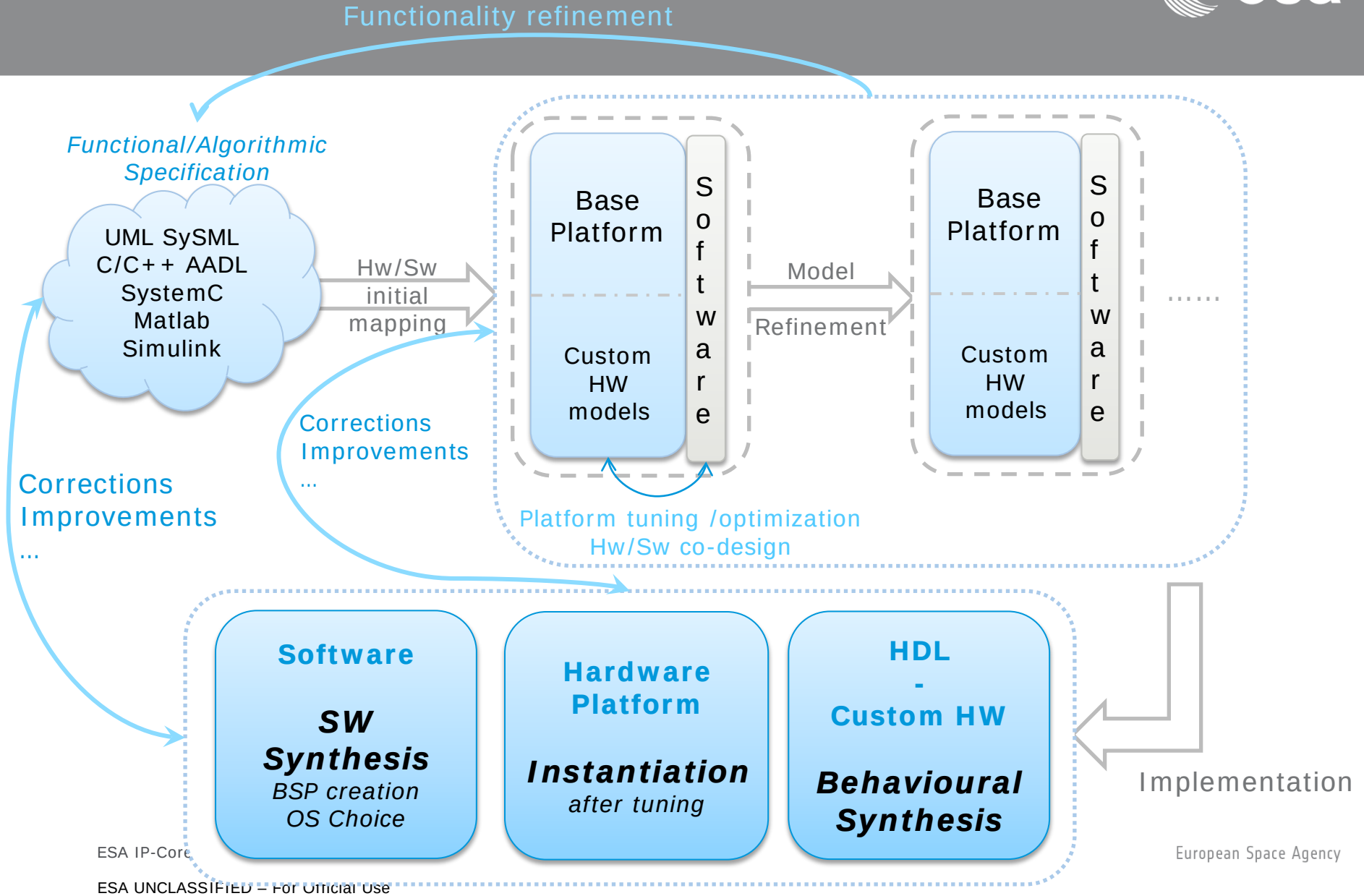
Thank You for Listening

For more information:

- Luca.Fossati@esa.int
- http://microelectronics.esa.int

- IP-Cores Workshop in September 2013 at ESTEC

ESL Design Flow



SystemC and TLM

SystemC

- ✓ IEEE standard, implemented as *a set of C++ classes*
- ✓ Standard C++ compiler can be used to generate an executable specification
- ✓ Addresses various levels of abstraction down to RTL

Transaction Level Modeling (TLM)

- ✓ Well-established methodology for modeling complex systems
- ✓ Separates *communication* from *computation*
- ✓ Modules communicate with the rest of the world by performing transactions
  - o Instead of modeling every single transferred bit, *data structures are exchanged*

Virtual Platform