SpaceWire-RT

SpaceWire-RT Status

SpaceWire-RT IP Core ASIC Feasibility

SpaceWire-RT Copper Line Transceivers

Overview of SpaceWire-RT Project

- Aims
  - The SpaceWire-RT research programme aims to:
    - Conceive and create communications network technology,
    - suitable for a wide range of demanding space applications
    - where responsiveness, determinism, robustness and durability are fundamental requirements.
  - A critical component technology for future spacecraft avionics and payloads.
  - QoS layer will be developed to support mixed avionics and data-handling applications.

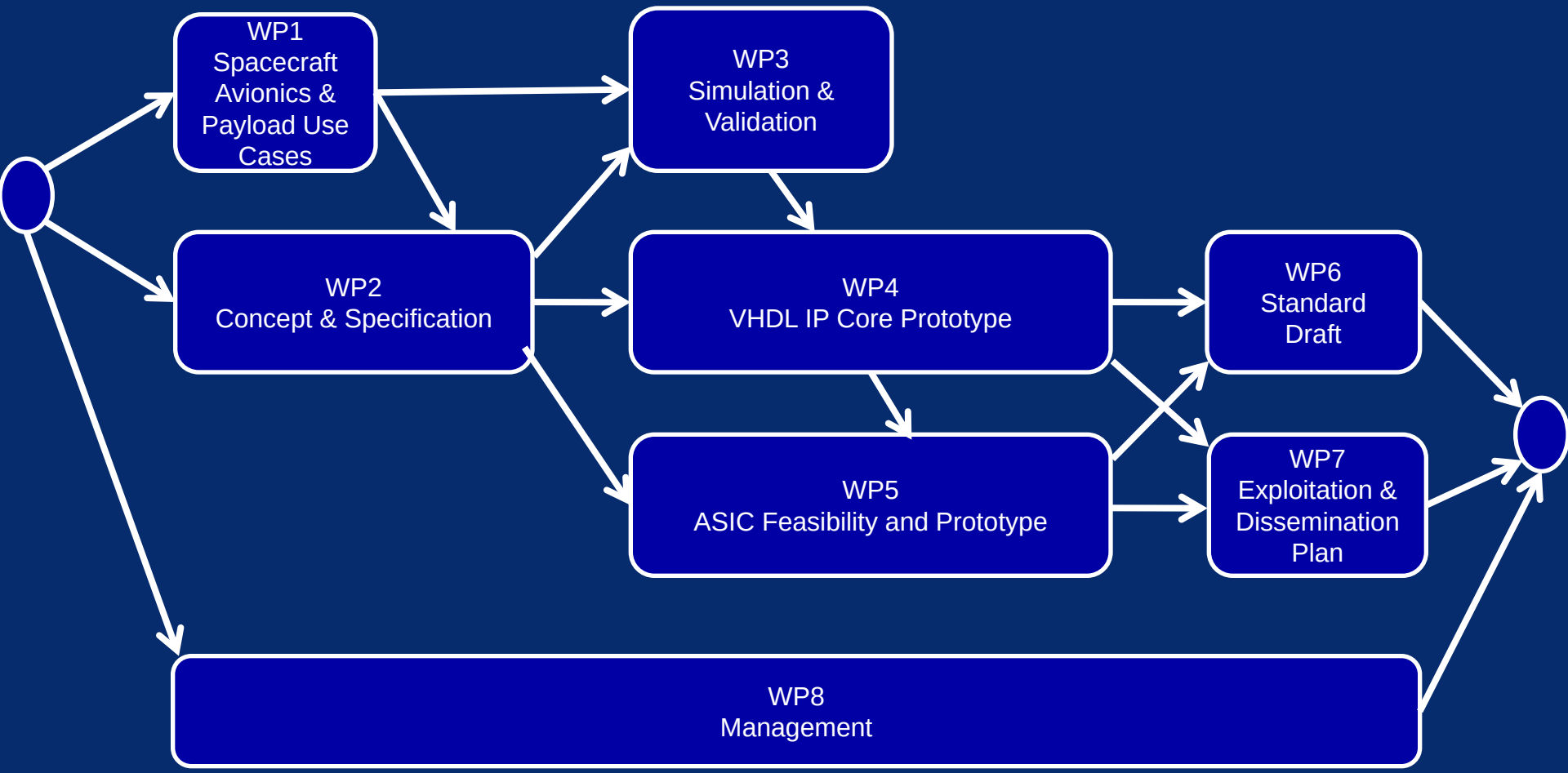
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Aims

	Distance	Rate	Latency	Packet size	QoS
Data-handling network	Short to long	Low to very high	Not important	Short to long	Reserved bandwidth
Control bus	Short to long	Low	Low	Short to long	Deterministic delivery
Telemetry bus	Short to long	Low	Low	Short	Reserved bandwidth
Computer bus	Short	Very high	Low	Short to long	Reserved bandwidth
Time-sync bus	Short to long	Low	Very low	Short	High priority
Side-band	Short	Low to high	Very low	Short	High priority

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

SpaceWire-RT Research Plan



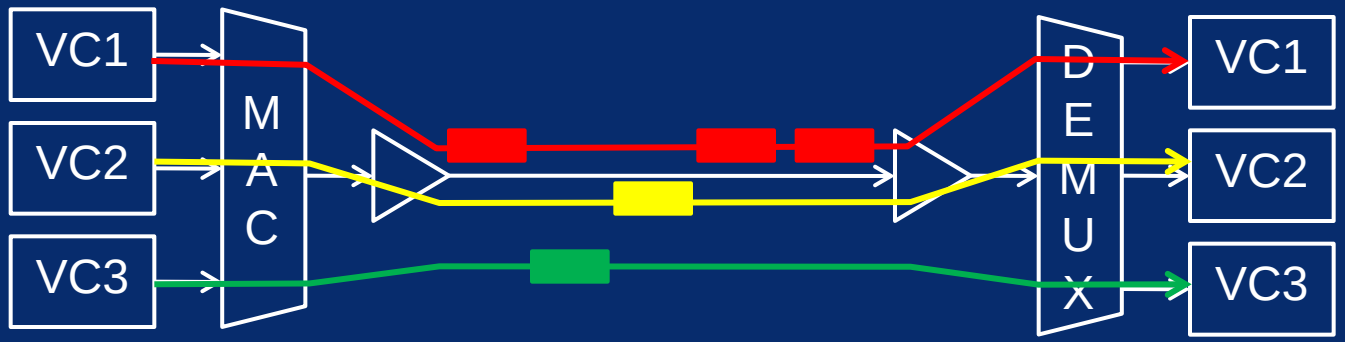
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

SpaceFibre Virtual Channels

- Virtual Channel Interface
  - Used to send and receive SpaceWire packets
    - Chops packet up into frames of up to 256 Nchars
    - For interleaving over the physical link
  - Comprises a number of virtual channel buffers
    - Output VCBs for sending SpaceWire packets
    - Input VCBs for receiving SpaceWire packets
    - Conceptual FIFO type interface
    - Accepts SpaceWire N-Chars (data + EOP/EEP)
  - Application
    - Loads packet information sequentially into VCB
    - Addressing and routing is identical to SpaceWire

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Virtual Channels



- VC sends when
  - Source VC buffer has data to send
  - Destination VC buffer has space in buffer
  - QoS for VC results in highest precedence
- A SpW packet flowing through one VC does not block another packet flowing through another VC

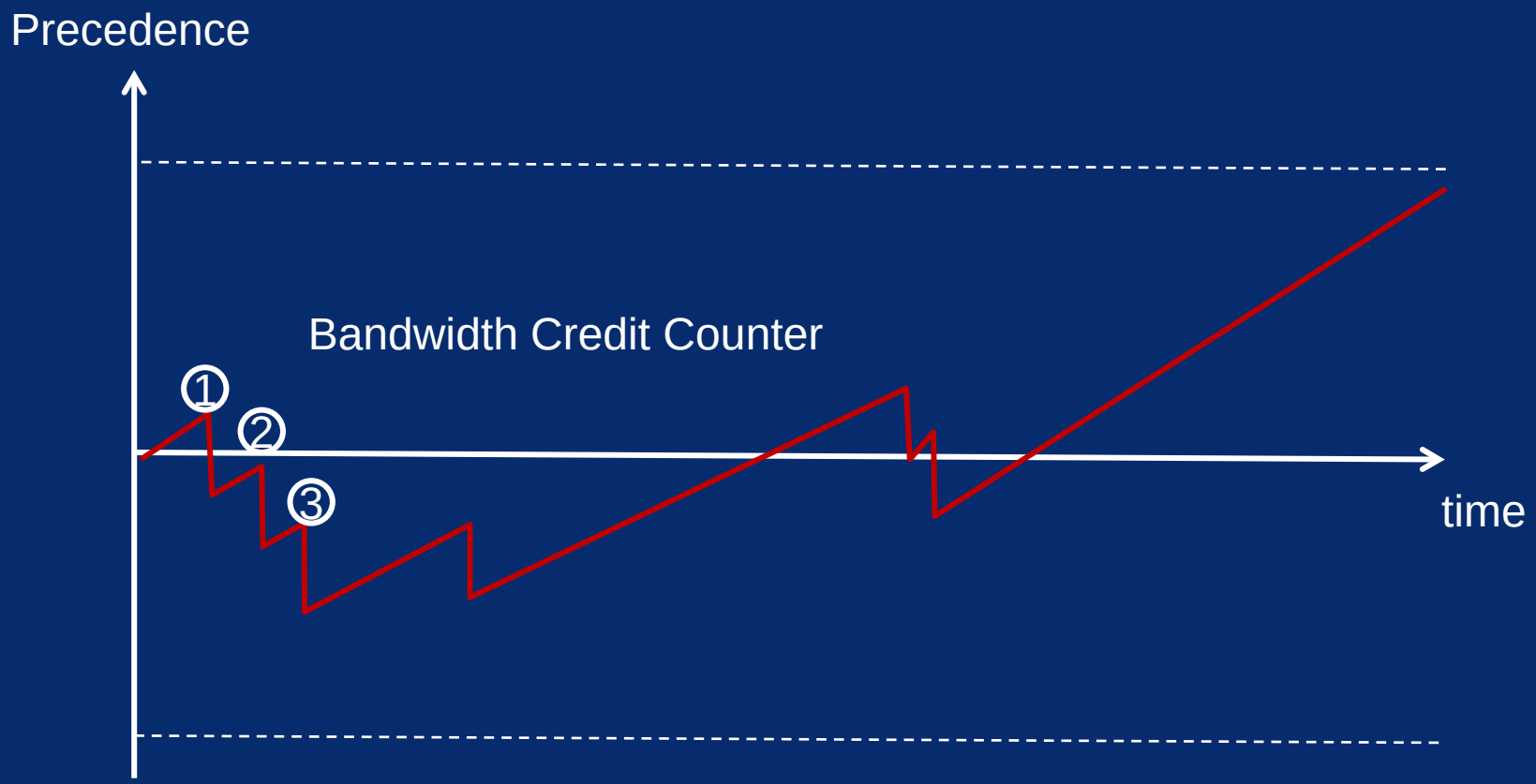
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

SpaceFibre QoS

- Integrated QoS scheme
  - Priority
    - VC with highest priority
  - Bandwidth reserved
    - VC with allocated bandwidth and recent low utilisation
  - Best Effort
    - VC can send when no other VC ready to send
  - Scheduled
    - Time-slots synchronised by broadcast messages
    - VCs allocated to specific time-slots
    - In allocated time-slot, VC allowed to send

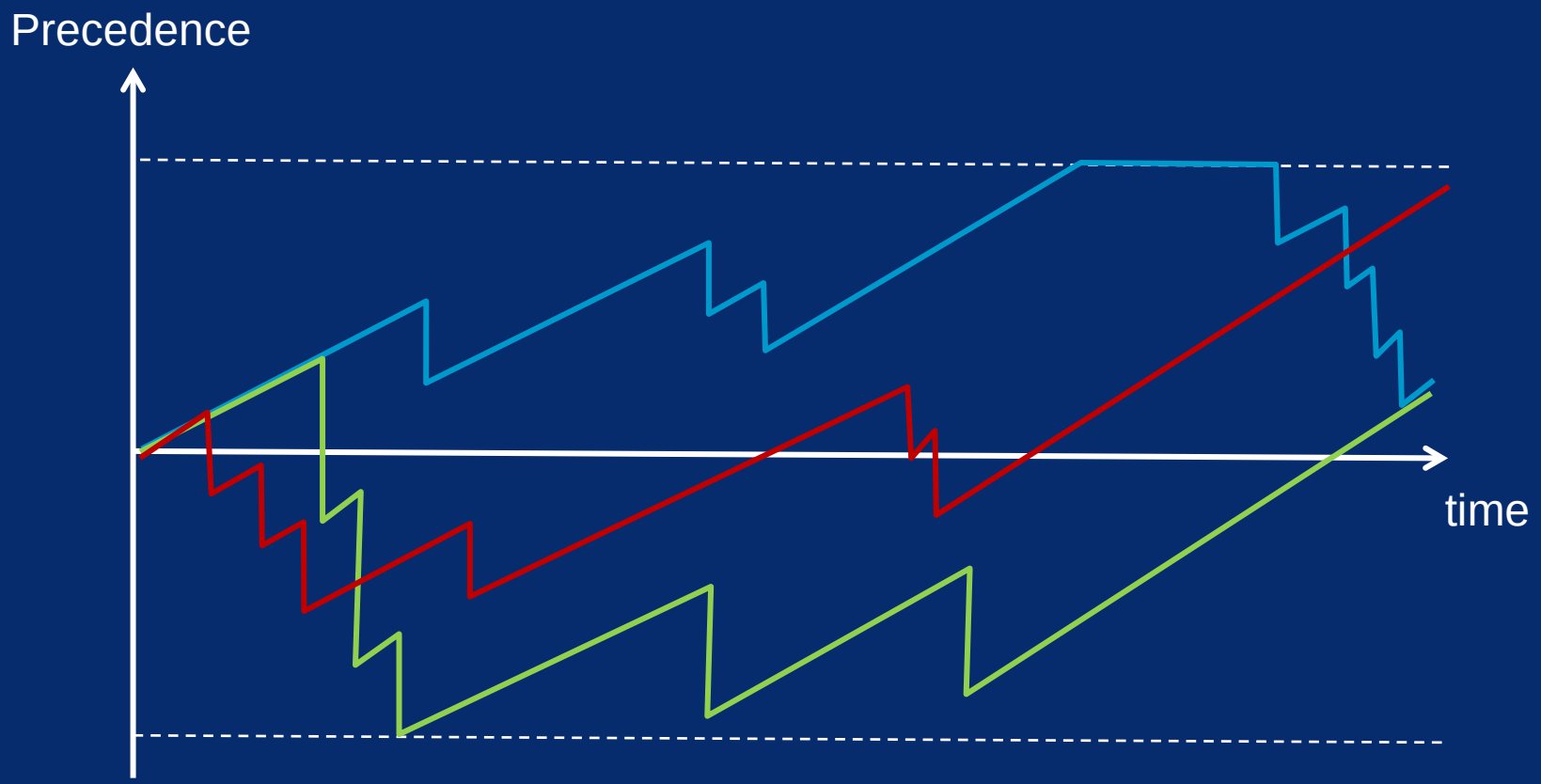
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

QoS: Bandwidth Reserved



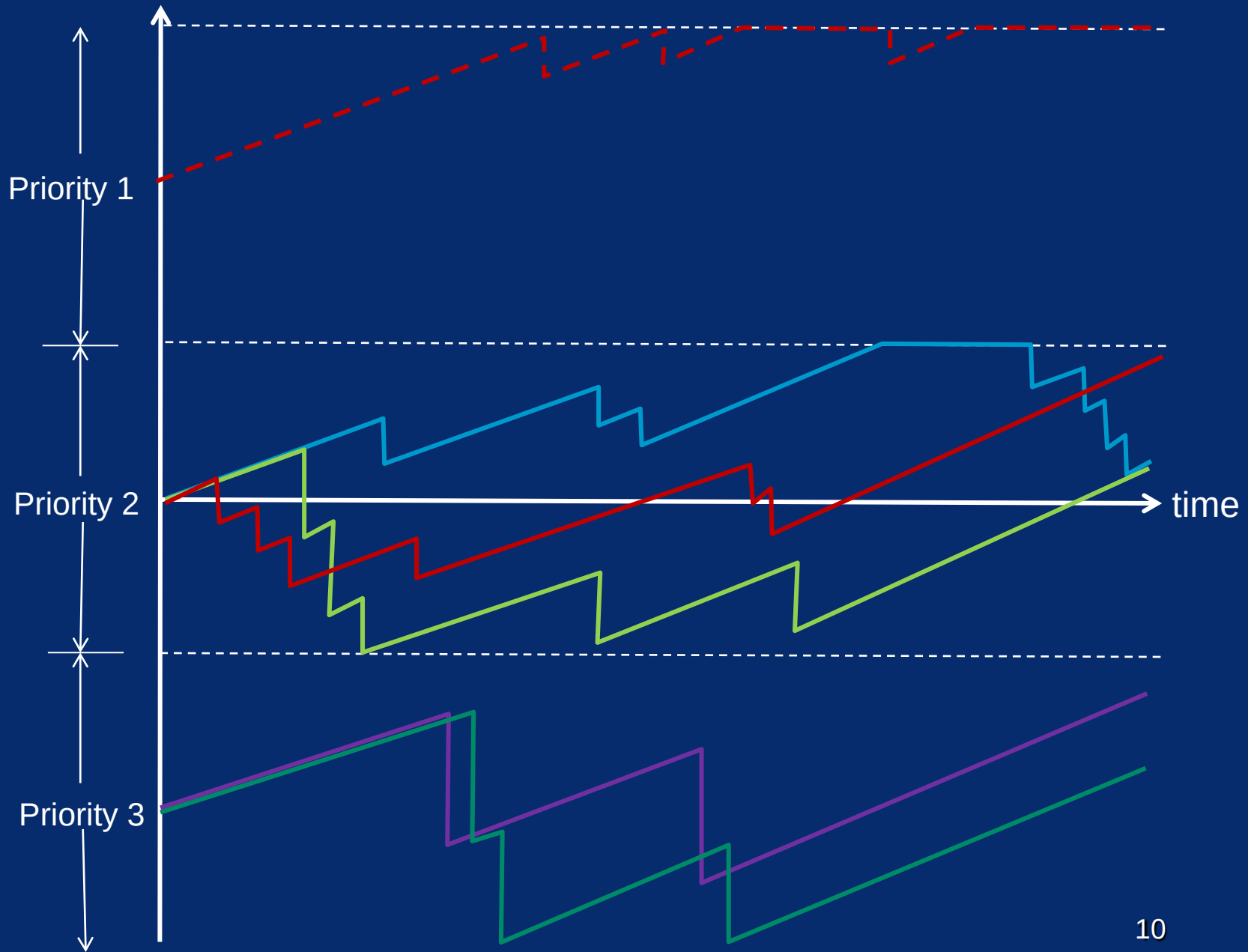
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

QoS: Bandwidth Reserved



The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

QoS Priority



FDIR Support in QoS

- Bandwidth credit counter also supports fault detection:
  - Excessive bandwidth utilisation
    - When BW credit counter reaches negative limit
  - Under utilisation of allocated bandwidth
    - When BW credit counter stays at maximum limit for long period of time
- Can be used to detect
  - Babbling idiots
  - Faulty units
- All provided with simple, low cost, mechanism

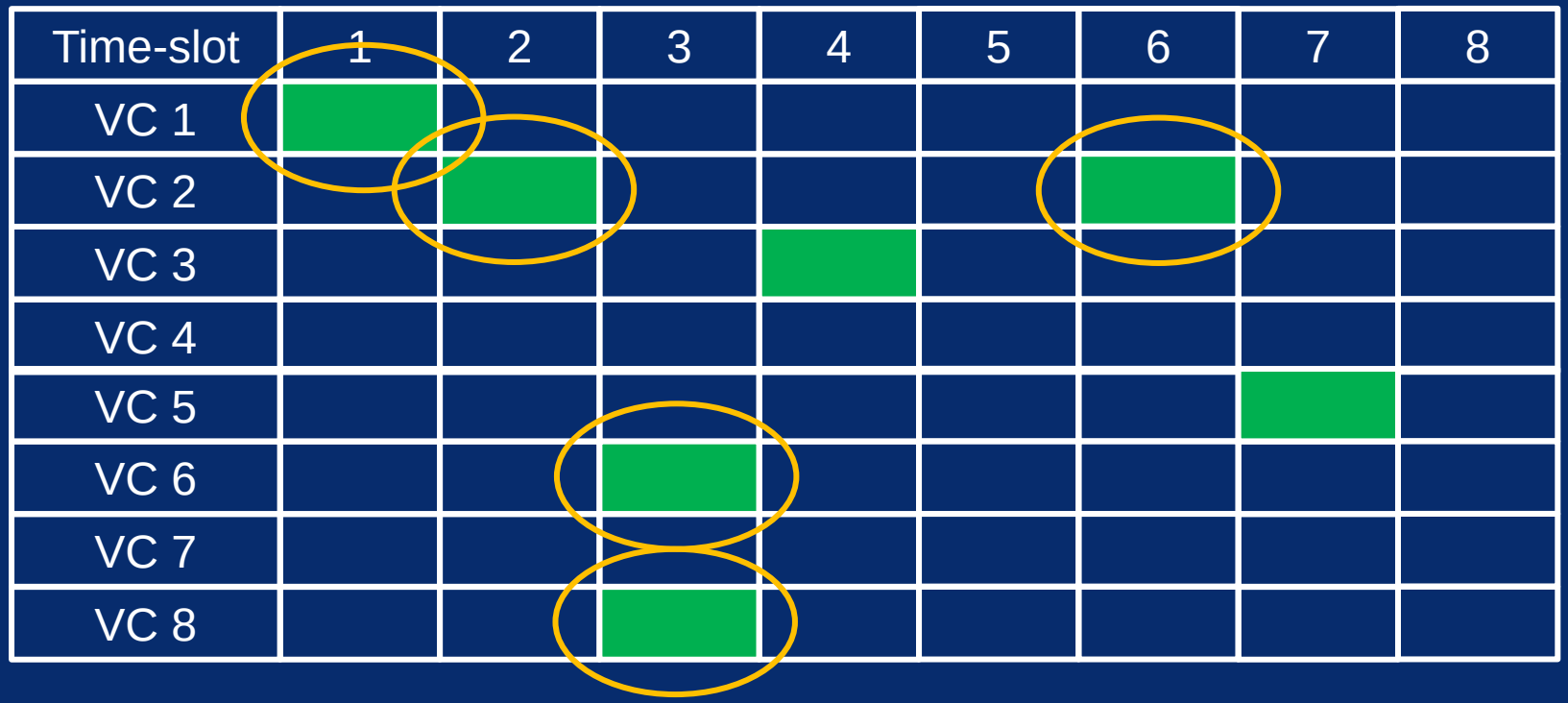
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Scheduled Precedence

- Time divided into time-slots
  - E.g. 64 time-slots of say 1 ms each
- Each VC allocated time-slots in which it is permitted to send data frames
- During a time-slot
  - If allowed to send in that time-slot
  - VC competes with other VCs also allowed to send in that time-slot
  - Based on precedence (priority and BW credit)
- A fully deterministic system would have one VC allowed to send in each time-slot

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Scheduled Precedence



Time-slot	1	2	3	4	5	6	7	8
VC 1								
VC 2								
VC 3								
VC 4								
VC 5								
VC 6								
VC 7								
VC 8								

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Configured for Priority and BW Reserved Only

Time-slot	1	2	3	4	5	6	7	8
VC 1								
VC 2								
VC 3								
VC 4								
VC 5								
VC 6								
VC 7								
VC 8								

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Mixed Deterministic and Priority/BW-Reserved

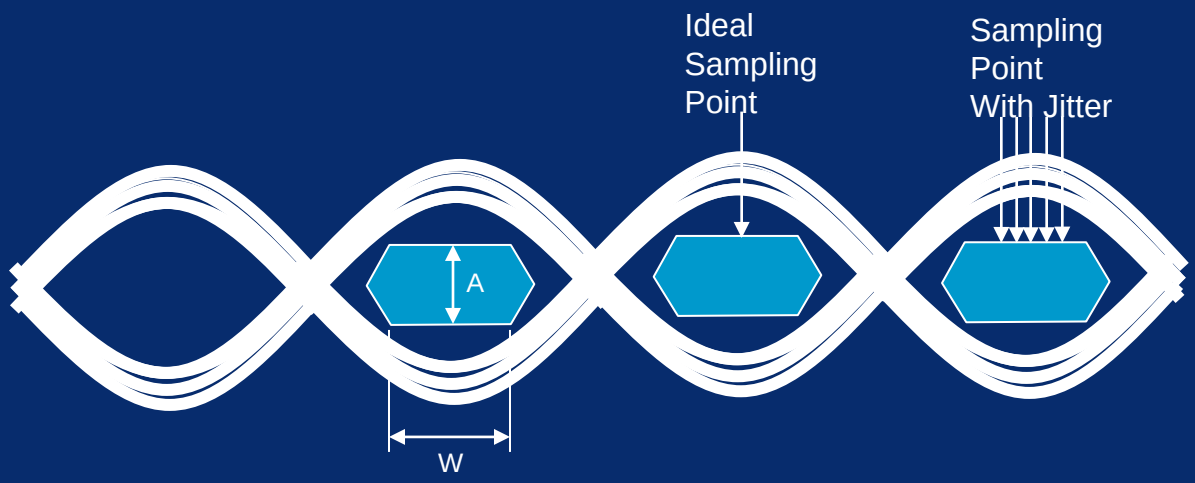
Time-slot	1	2	3	4	5	6	7	8
VC 1								
VC 2								
VC 3								
VC 4								
VC 5								
VC 6								
VC 7								
VC 8								

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Oversampling SpaceFibre

- Aims:
  - Simple implementation of SpaceFibre
  - In standard flight FPGA
  - No special clock and data recovery (CDR)
    - E.g. Phase-locked loop
  - Operate at modest speeds
    - E.g. 100 Mbits/s
  - Use LVDS instead of CML
  - Provide all the benefits of SpaceFibre
    - QoS
    - FDIR
    - Galvanic isolation
  - Key issue is recovering the data from the bit stream

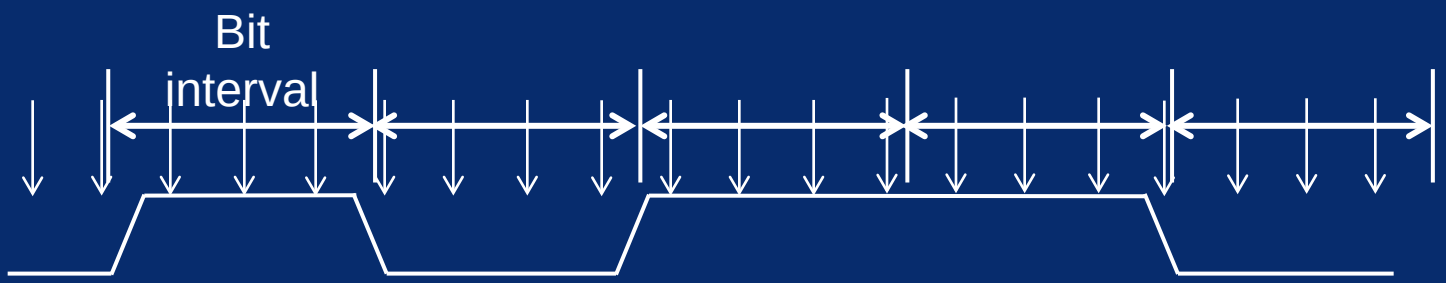
Oversampling SpaceFibre



a) Received eye pattern and sampling

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

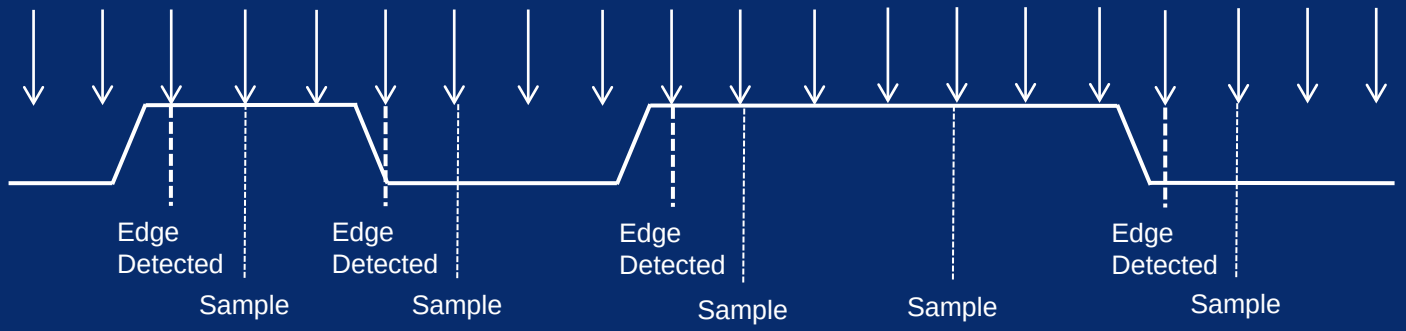
Oversampling SpaceFibre



b) Oversampling

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

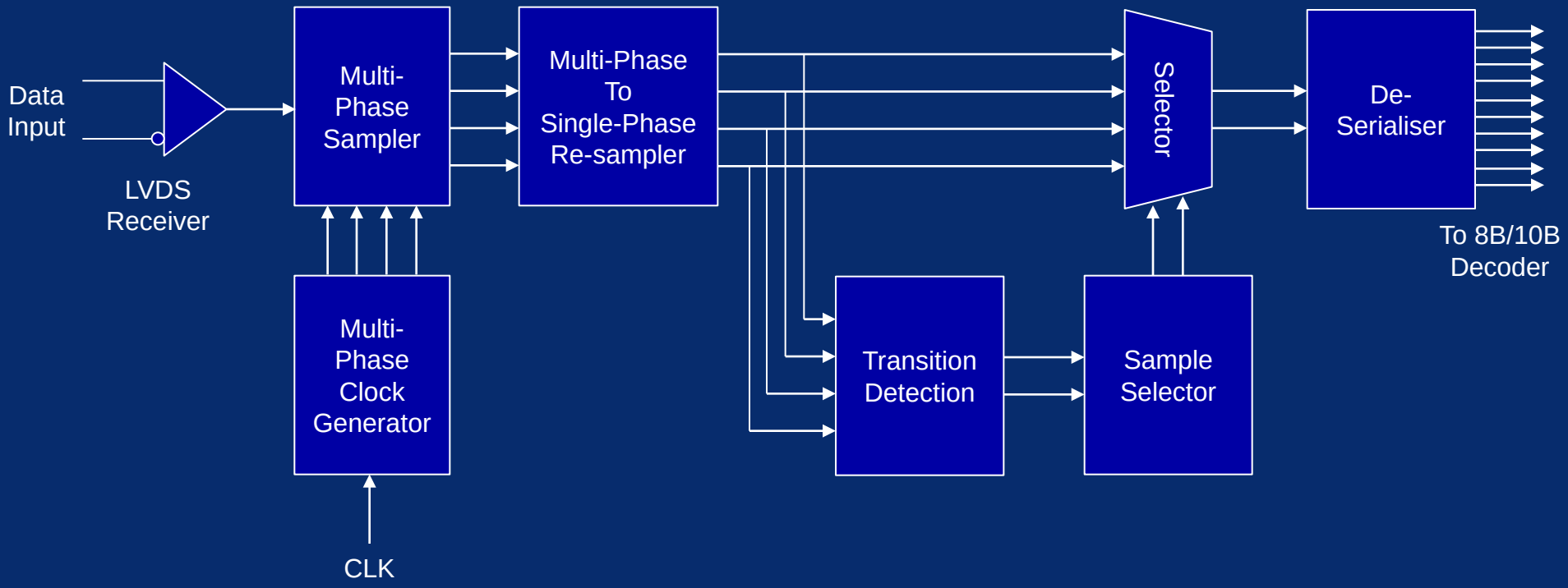
Oversampling SpaceFibre



c) Selecting the sample

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Oversampling Architecture



Basic oversampling idea from a Xilinx application note

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Oversampling SpaceFibre

- Advantages:
  - Clock recovery does not require PLL
  - Covers 1 Mbits/s to 100 Mbits/s (TBC) speed range
  - Lower cable mass than SpaceWire
  - Minor extension to the SpaceFibre standard
  - LVDS interfaces available on most FPGAs
  - LVDS proven in space flight
  - May save some power compared to CML (TBC)
  - Can interoperate with SpaceFibre-LVDS depending on speed used
- Disadvantage:
  - Limited maximum speed (100 Mbits/s TBC)

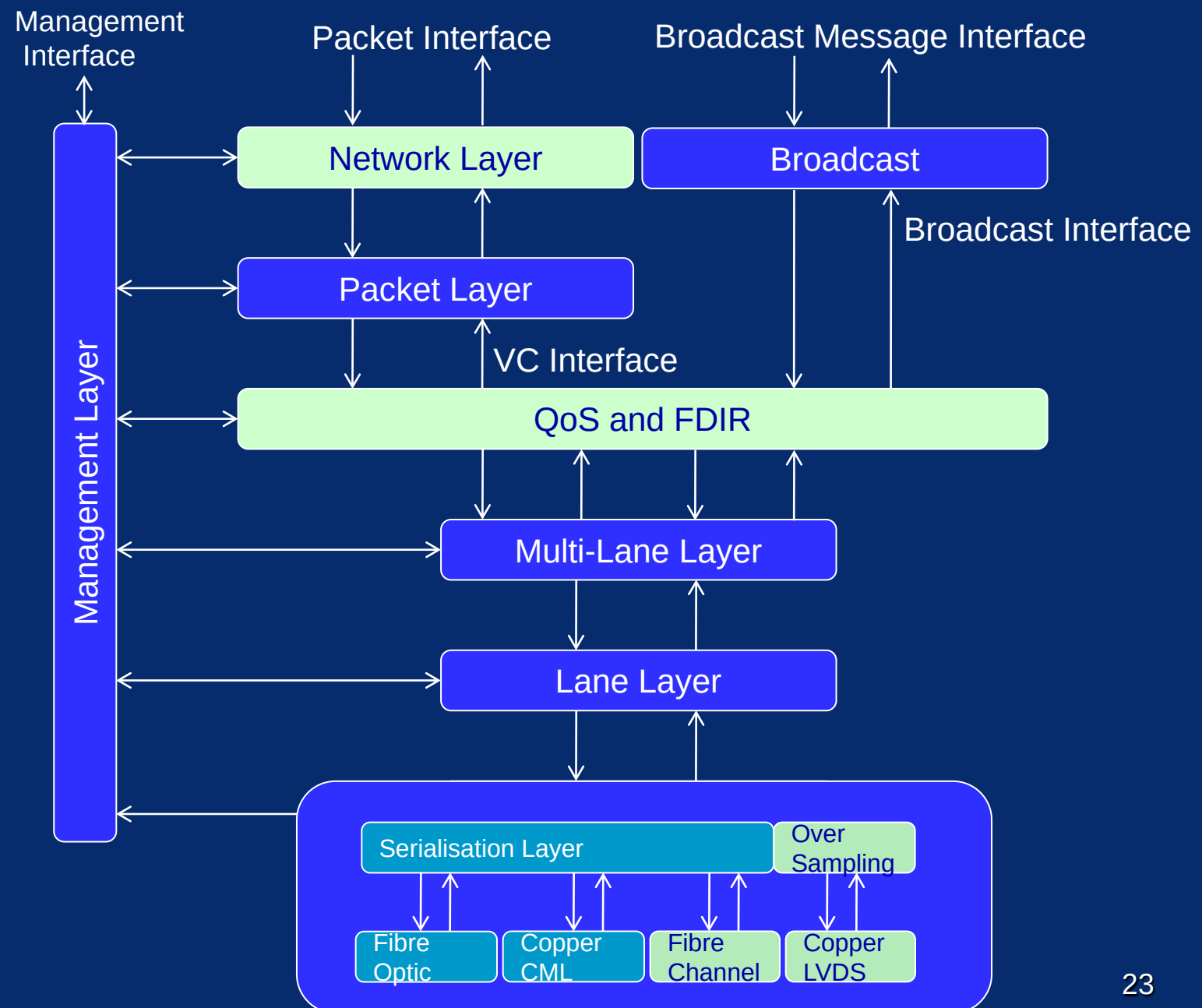
The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

Summary

- Oversampled SpaceFibre
  - Lower speed SpaceFibre
  - Galvanic isolation
  - All SpaceFibre QoS and FDIR capabilities
  - Uses LVDS
  - Can be implemented in current flight FPGAs
  - Simple CDR mechanism
  - Saves on cable mass
- Currently designing prototype
  - Expect to test this by end 2Q2013

The SPACEWIRE-RT project has received funding from the European Union Seventh Framework Programme (FP7/2007-2013) under Grant Agreement no. 263148

SpW-RT/SpFi Protocol Stack



SpaceWire-RT Achievements

- Requirements for spacecraft networks
- Selected SpaceFibre as basis for SpW-RT
- Developed missing parts of SpFi
- Contributions to SpaceFibre specification
  - Protocols
    - Network layer
    - QoS/FDIR layer
    - Oversampling LVDS
  - Validation
    - Simulation of drafts C, D and E
    - Feedback on various issues
    - Helping to shape the specification
  - Flight implementation feasibility
    - Feasibility of several ASIC technologies assessed
    - Very promising results