Preliminary feedbacks on the use SpFi for HiP CBC

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All the space you need

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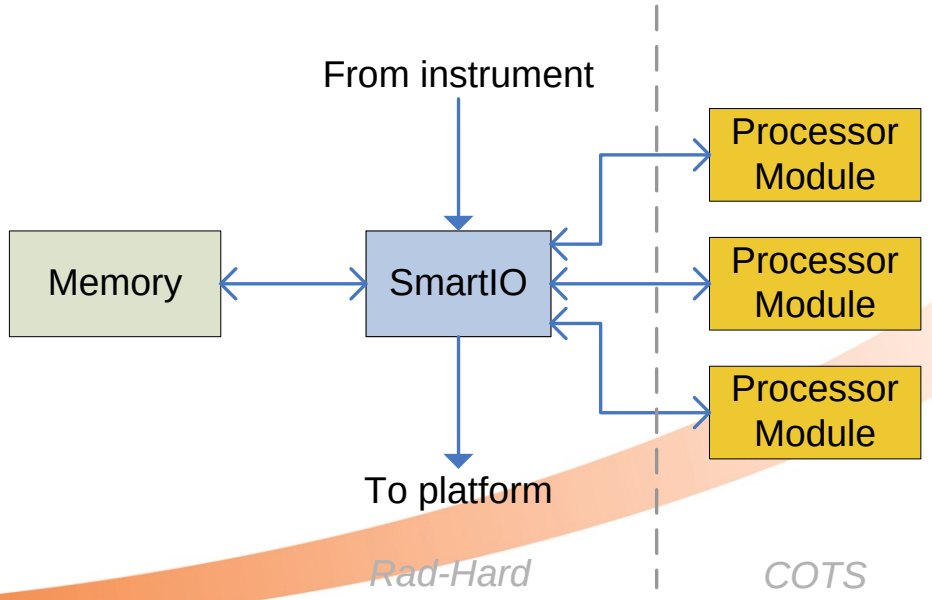
Outline

- HiP CBC introduction
- Context of use of the SpFi
- SpFi and AMBA interface
- SpFi IP in ProAsic with TLK2711

HiP CBC introduction

- High Performance COTS Based Computer
  - Aims at using rad-soft COTS components for payload data processing
  - On-going activity, KO 01/01/12, ends Q4 2013
- Overall architecture



Interest for SpFi for HiP CBC

- First iteration of architecture is based on SpW communication links
  - With RMAP
  - Using existing SpW IP
  - Target data rates of 160 Mbit/s
- Need for faster data links to saturate COTS components
  - Processing capability of 1Gop/s
  - Data link is the performance bottleneck for most applications

→ We need an “accelerated” SpW RMAP!

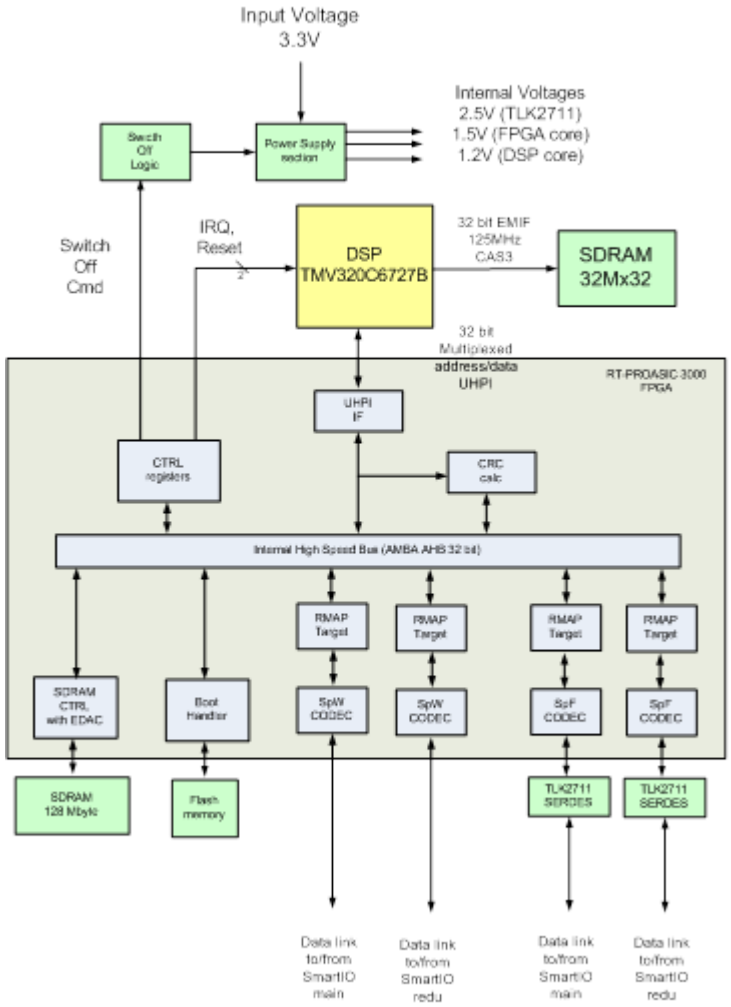
SpFi and AMBA interface

- Our need is AMBA bus to AMBA bus communication
  - RMAP transfers from SmartIO memory to Processing module memory
- As of today SpFi IP is not including an AMBA bus interface
  - We reused SpW RMAP IP
  - SpW RMAP IP is « glued » to the SpFi IP

SpFi and AMBA interface

- Problem: SpW RMAP IP was not designed to handle such high data rates
  - SpW RMAP IP is limiting the maximum data rate achievable
  - Maximum achievable data rates with current SpW RMAP IP in Spartan6 FPGA: 600-800 Mbit/s
  - Performance of other SpW RMAP IP unknown
- A dedicated SpFi AMBA AXI interface would be interesting

PM Overview



- Based on TI C6727
- 128Mbytes PM SDRAM
- 128Mbytes EDAC protected memory
- 32Mbyte local Flash
- 2 Spacewire interfaces
- 2 SpaceFibre interfaces on copper

SpFi interface on the PM

- The interface is implemented using the IP provided by UoD
- SERDES implemented using TI TLK2711
- Harness based on 4 coaxial cables
- 4 SMAs connectors on the board for each link
- Target data rate > 500 Mbit/s – maximum throughput supported by the FPGA/DSP interface
- IP shall be implemented on Actel PROASIC FPGA

SpFi design constraints

- The interface according to the IP documentation requires 4 clocks domains

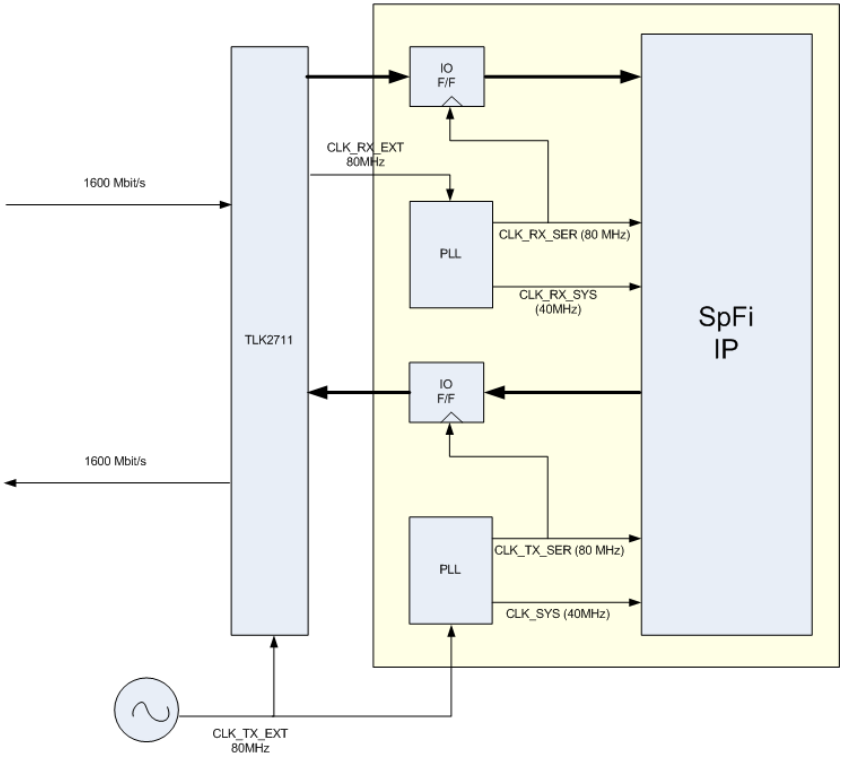
Signal	Type	Description	Nominal Frequency	Alignment
CLK_SYS	In	Reference clock of the SpFi IP Core	62.5 MHz	Reference clock
CLK_TX_SER	In	Clock used for the transmission of words to the SERDES module	125 MHz	To CLK_SYS
CLK_RX_SER	In	Clock used for the reception of symbols from the SERDES module	125 MHz	Supplied by the SERDES
CLK_RX_SYS	In	Clock used for the alignment of the received codes	62.5 MHz	To CLK_RX_SER

- Minimum TLK2711 input clock frequency is 80 MHz –> 1600 Mbit/s link

SpFi interface design

In the first design implemented in the Hi-P board were foreseen

- Use of two PLLs for generation of the RX clocks and TX clocks with phase alignment for each SpFi interface
- Minimum FPGA clock performances required
  - CLK_SYS and CLK_RX_SYS 40 MHz
  - CLK_TX_SER and CLK_RX_SER 80MHz



SpFi design constraints

Use of clock resources in the FPGA test design including 2 SpFi interfaces was planned as follow

2 Global clock networks for SpFi TX1 and TX2 clocks
2 Quadrant clock networks for SpFi RX1 clocks
2 Quadrant clock networks for SpFi RX2 clocks

SpFi interface design

Timing analysis of the FPGA shows that required clock performances cannot be achieved with PROASIC3 A3PE3000L in the configuration foreseen for Hi-P PM

In particular the CLK_SYS used in the TX section from our preliminary evaluation is limited to a frequency lower than 30MHz

Further investigations will be performed when the SpFi IP with added AMBA interface will be available