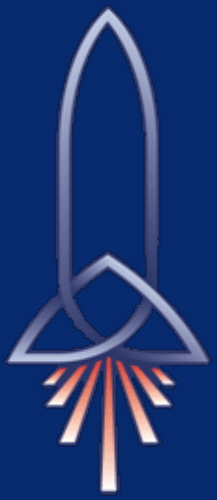

SpaceFibre

SpaceFibre Implementation and Demonstration

SpaceFibre IP Core Beta-Testing

SpaceFibre Interoperability Testing

SpaceFibre SpaceWire-RT (Wednesday)

SpaceFibre Simulation (Thursday)

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SpaceFibre Introduction

- Spacecraft on-board data-handling network
  - Compatible with SpaceWire at packet level
- SpaceFibre key features
  - High performance
  - Low latency
  - Integrated QoS
  - Integrated FDIR capabilities

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SpaceFibre Key Features

- High performance
  - 2.5 Gbits/s with current space qualified technology
  - 20 Gbits/s and higher with future tech and multi-laning
- Low latency
  - QoS precedence
  - Broadcast channels
- QoS
  - Integrated
    - Bandwidth reservation
    - Priority
    - Scheduling for deterministic data delivery

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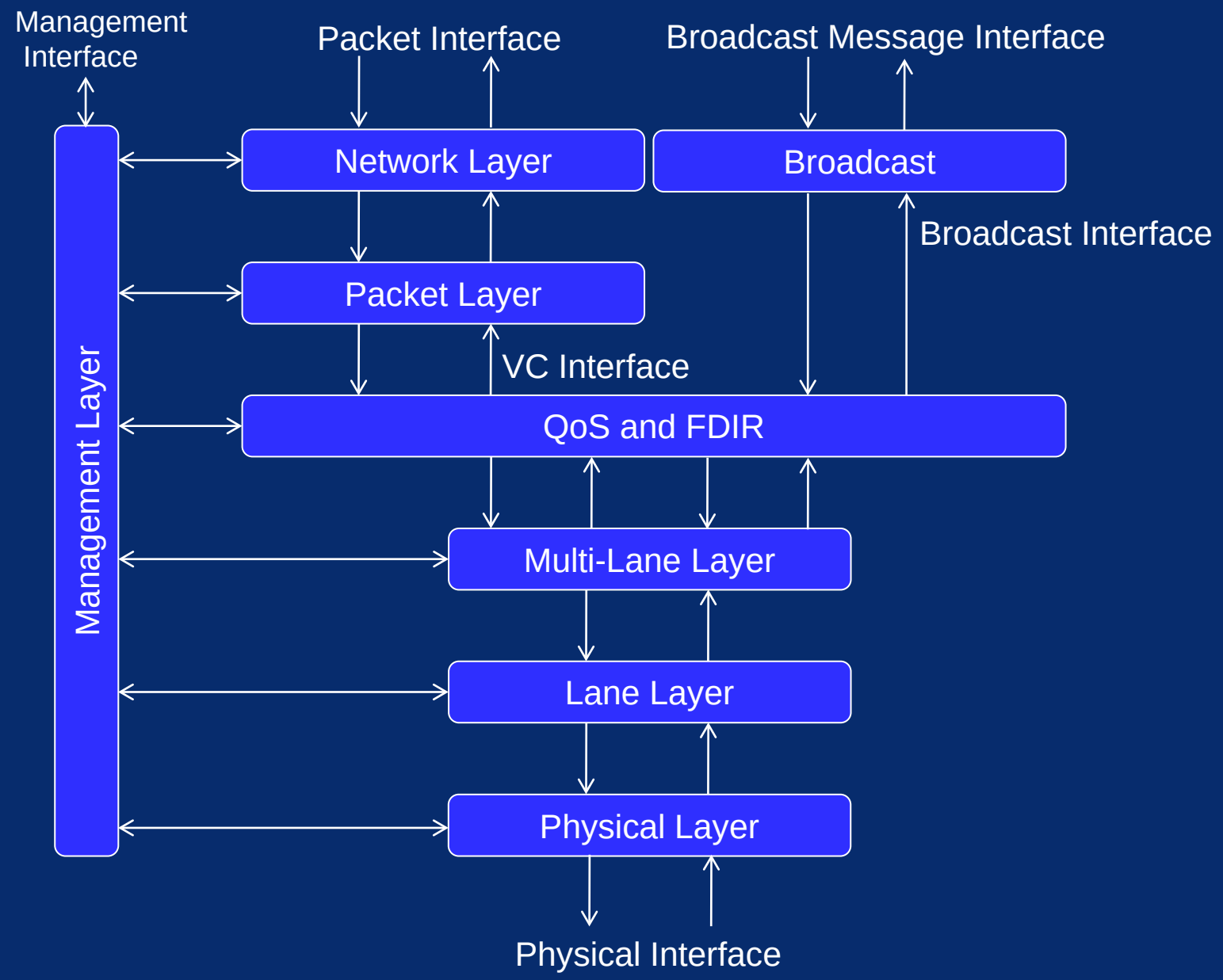
SpaceFibre Key Features

- FDIR
  - Fault detection
    - Parity/disparity
    - Invalid 8B/10B codes
    - Enhanced Hamming distance
    - CRC
    - Over and under utilisation of expected bandwidth
  - Fault isolation
    - Galvanic isolation (AC coupling)
    - Data framing – time containment
    - Virtual channels – bandwidth containment
  - Fault recovery
    - Rapid link-level retry
    - Graceful degradation on lane failure
    - Babbling idiot protection
    - Error reporting

SpaceFibre Overview



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SpaceFibre Layers

- **Network:**
  - Transfer of packets over network
  - Same routing concepts as SpaceWire
  - Path and logical addressing
- **Broadcast:**
  - Broadcasts short messages across network
  - Can carry time-codes, time messages, events
- **Packet:**
  - Packages information to be sent over link
  - <Destination Address><Cargo><EOP>
- **Management :**
  - Configures, controls and monitors status

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SpaceFibre Layers

- **QoS and FDIR**
  - **Virtual Channel:**
    - Quality of service and flow control
  - **Framing:**
    - Frames information to be sent over link
    - Scrambles SpaceWire packet data
  - **Retry:**
    - Recovers from transient errors
    - Can cope with bit error rate of 10^{-5}
- **Multi-Lane:**
  - Runs several SpaceFibre lanes in parallel
  - Provides higher data throughput and redundancy with graceful degradation

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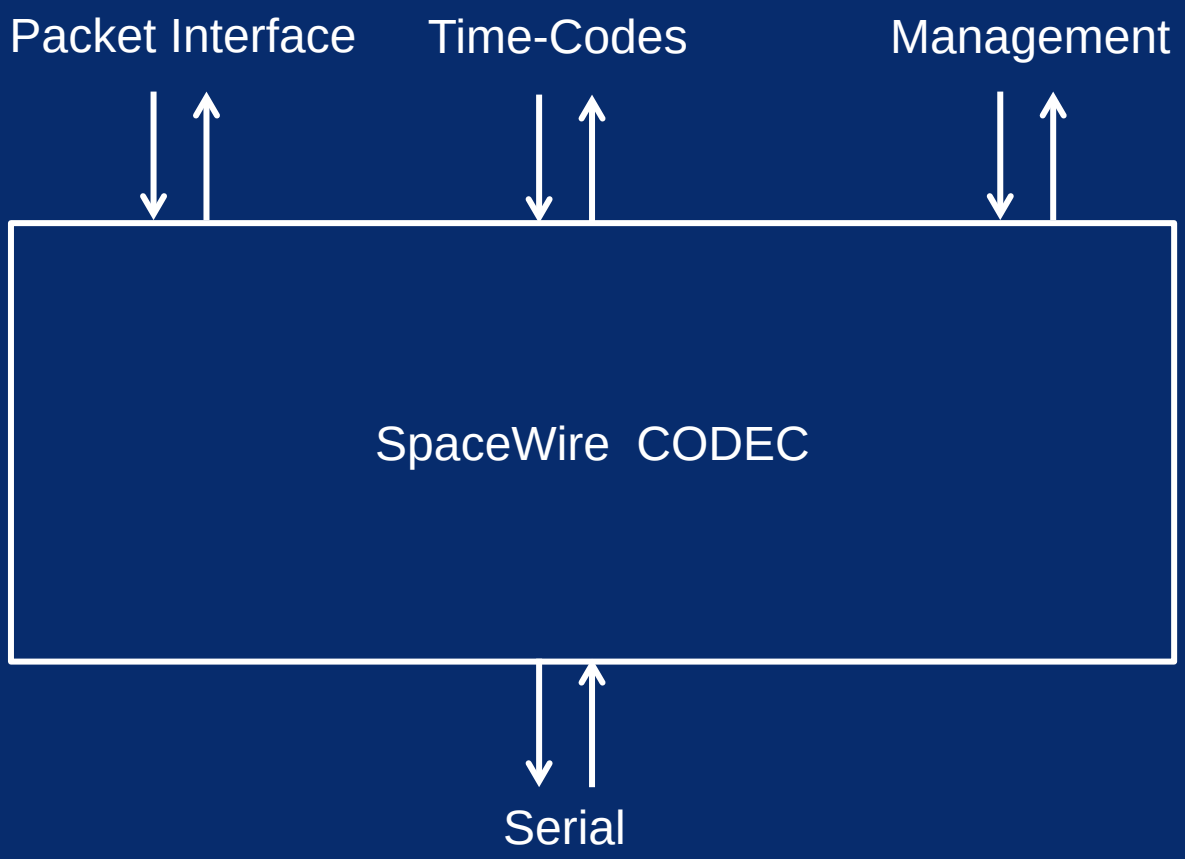
SpaceFibre Layers

- **Lane:**
  - Lane control
    - Lane initialisation and error detection
  - Encoding/Decoding:
    - Encodes data into symbols for transmission
    - 8B/10B encoding
    - DC balanced
  - Serialisation:
    - Serialises SpaceFibre symbols
    - Includes oversampling clock-data recovery
- **Physical:**
  - Fibre optic or electrical medium

SpaceWire CODEC



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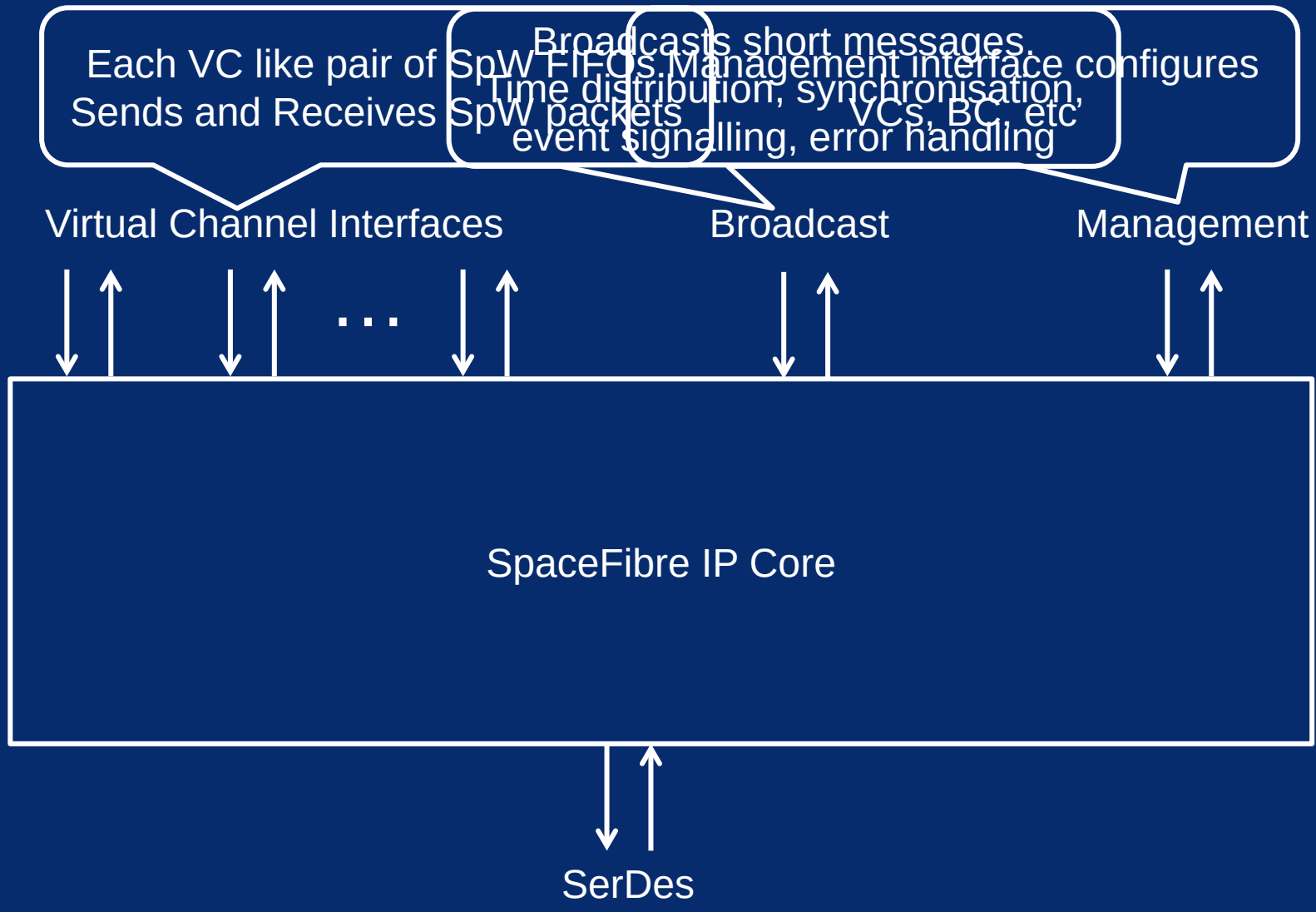
SpaceFibre IP Core



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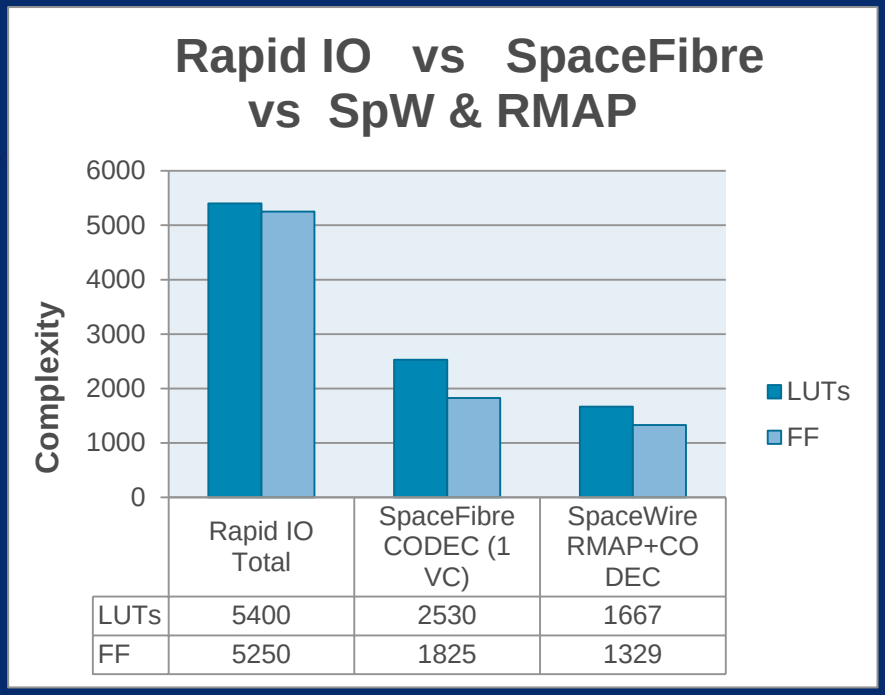
SpaceFibre Unique Features

- Compatible with SpaceWire at packet level
- FDIR
  - Improved data integrity
    - Single bit error cannot corrupt data or protocol operation
      - Careful selection of 8B/10B control codes
      - Data frame CRC
    - Cable BER of 10^{-10} (one error every 3 seconds)
      - Results in a link protocol BER of 10^{-25}
        - (one error every 100 million years)
    - Automatic reconnection when BER lower than expected
    - 16-bit data frame CRC
  - Link retry does not use timeouts
  - Short error recovery time of a few µs
  - Graceful degradation with multiple lanes

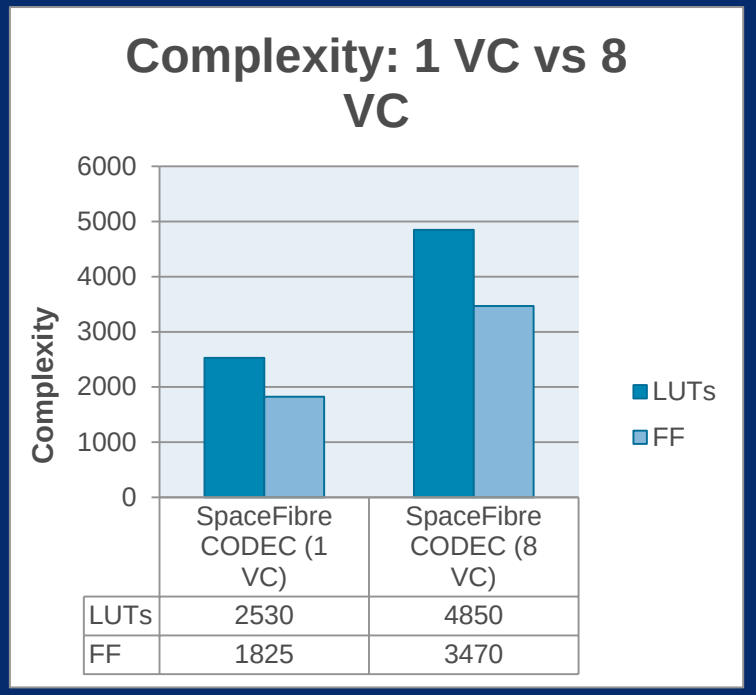
SpaceFibre Unique Features

- Integrated Quality of Service
  - Bandwidth reservation
  - Priority
  - Scheduled
    - Providing deterministic operation
- Low latency
  - High precedence VCs
  - Broadcast messages
- Low implementation complexity
  - 12% to 20% utilisation of AX2000S (1 or 2 VCs)
  - 3% to 6% utilisation of Spartan 6 75T (1 to 8 VCs)
  - Similar to SpaceWire+RMAP IP core

SpaceFibre smaller than RAPID IO



	Rapid IO Total	SpaceFibre CODEC (1 VC)	SpaceWire RMAP+CODEC
LUTs	5400	2530	1667
FF	5250	1825	1329



	SpaceFibre CODEC (1 VC)	SpaceFibre CODEC (8 VC)
LUTs	2530	4850
FF	1825	3470

Rapid IO v2.1 x1 (Based on Xilinx srio_ds696, Spartan 6 results)

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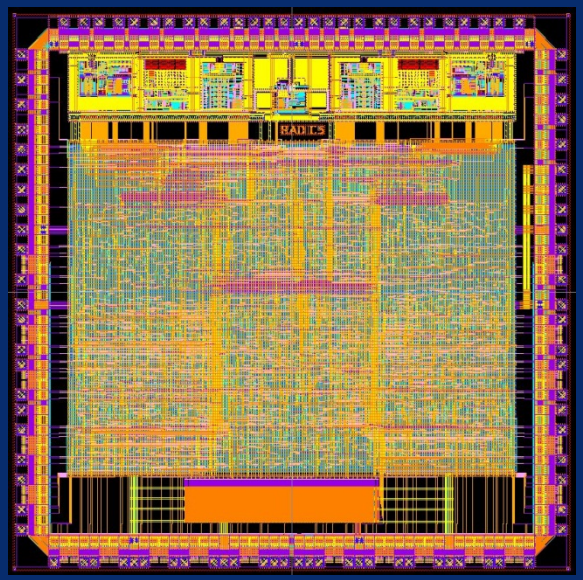
SpaceFibre IP Core

- VHDL IP Core
  - Compliant to current version of standard
  - Interfaces
    - Virtual channel interface
    - Broadcast channel interface
    - Management interface
  - QoS
    - Integrated priority and bandwidth reservation
    - Scheduling with 64 time-slots
  - Retry
    - Rapid retry
  - Single lane
    - Multi-lane support will be provided 2013
- Updated to latest version of standard

SpaceFibre Implementations



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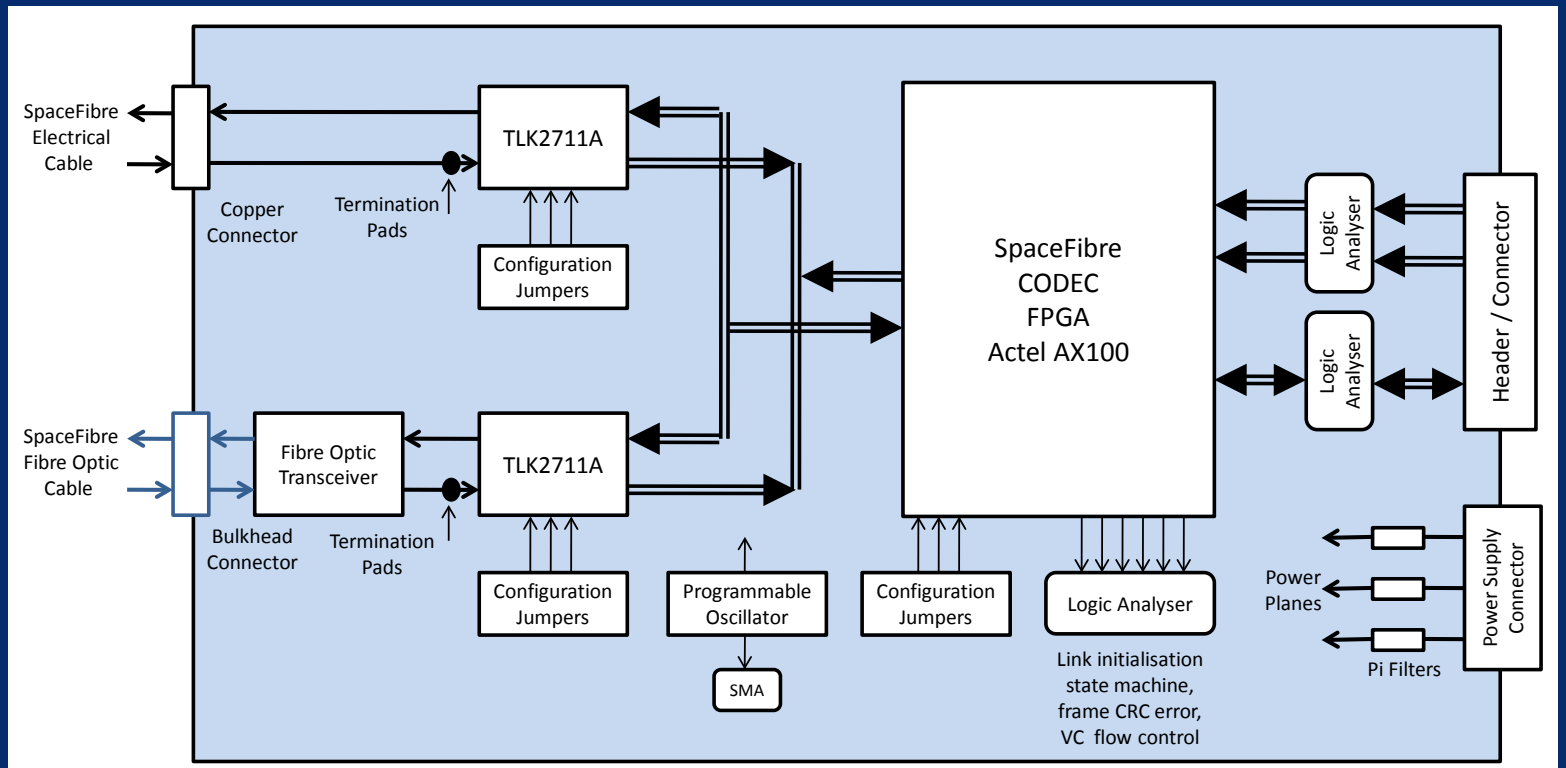
ESA Projects using SpaceFibre

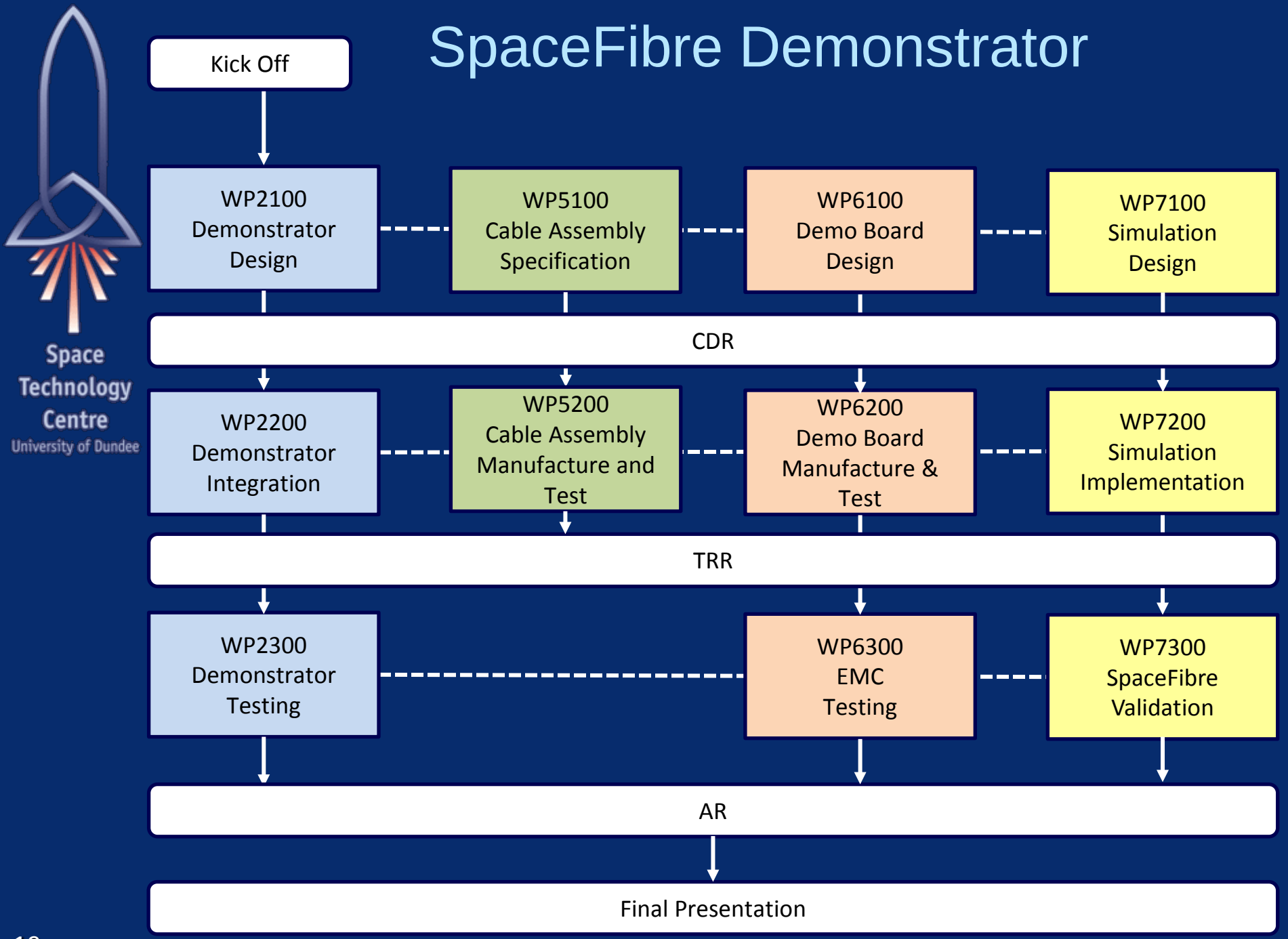
- 2 x High Performance COTS Based Computer, Step 2 (Prototyping and Validation), Astrium (Fr)
- 1 x Leon with Fast Fourier Transform Co-processor, SSBV (NL)
- 1 x FPGA Based Generic Module and Dynamic Reconfigurator, TWT (D)
- 2 x Next Generation Mass Memory, Astrium (D), IDA (D)
- 1 x High Processing Power DSP, Astrium (UK)

SpaceFibre Sub-Contracts

- ITTs to be issued 2Q2013
- SpaceFibre Demonstrator sub-contracts
  - Cables and Connectors
  - Demonstration Board and Testing
  - Simulation and Validation



SpaceFibre Demonstrator



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SpaceFibre Demonstration

- Basic Operation
- SpaceFibre
  - 5 m EGSE cable
  - Fibre optic cable
- Error recovery

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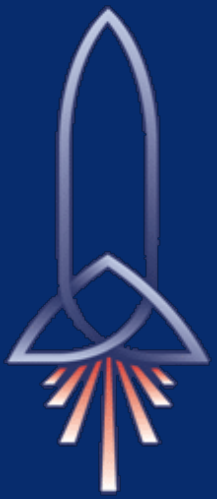

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SpaceFibre Standard Improvements

1. Restructured
   - Network, packet and management layers added
   - QoS and FDIR layer combines several functions
2. Efficient retry layer
   - Fastest error recovery time (2-5us at 2.5Gb/s)
   - Supports any link speeds (no timeouts used)
3. Lane initialisation state machine simplified and improved.
   - Robust link initialisation
   - Automatic link reconnection when BER is too low
4. More robust control word encoding scheme
   - Single bit flips in the line are detected by the 8B10B encoding and CRC
5. Management and physical layer described
   - Electrical connectors and cable assemblies added to physical layer