Versatile Test System for varying Hardware Configurations

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Why Yet Another Test System (1/3)

Situation

- Digital hardware and EGSE developments within TEC-EDP contracts
- EGSE and test software optimized for project test plan/ procedure
- EGSE used for all hardware models (BB/ EM/ QM/ FM)

Motivation

- Perform tests in parallel with the contractor
- Perform parallel failure investigations within the lab
- Perform additional tests not included in the test plan
- Provide independent test setup

Why YATS (2/3)

Difficulties

- Different EGSE with every contract
  - No synergy effects between projects
  - No synergy effects between technical officers
- Insufficient level of documentation
  - If available, focused on the EGSE usage
  - Limited information on the EGSE design

  => Difficult to extend the system
- EGSE delivered at project end

  => not available for intermediate testing
- Limited lab time available for technical officers
  - Should be spend with testing, not with EGSE

Why YATS (3/3)

Idea

- Define own, project independent and “easy” to use test system
  - Exploit synergy effects
  - Extend range of testability
  - Identify shortcomings of project EGSE

Requirements

- Facilitate steep learning curve
- Modular approach
- Flexible test sceneries
- Versatile interface support

The Approach

Picture source: http://www.ni.com/pxi/

Modular Instrumentation

- National Instruments PXI architecture
- Software-defined, modular architecture
- Variable COTS hardware components

  => Covers standard interfaces
- Common programming interface and API

  => Synergy effects between projects and technical officers

Project Specific Requirements

- Programmable FPGA module
  - Test vector generation/ comparison
  - Adaptation to non-standard DUT interfaces

Versatile FPGA Module

Adapter Module

- DUT physical layer adaptation
- Interchangeable I/O
- Customizable by user
- Development kit available

FPGA Module

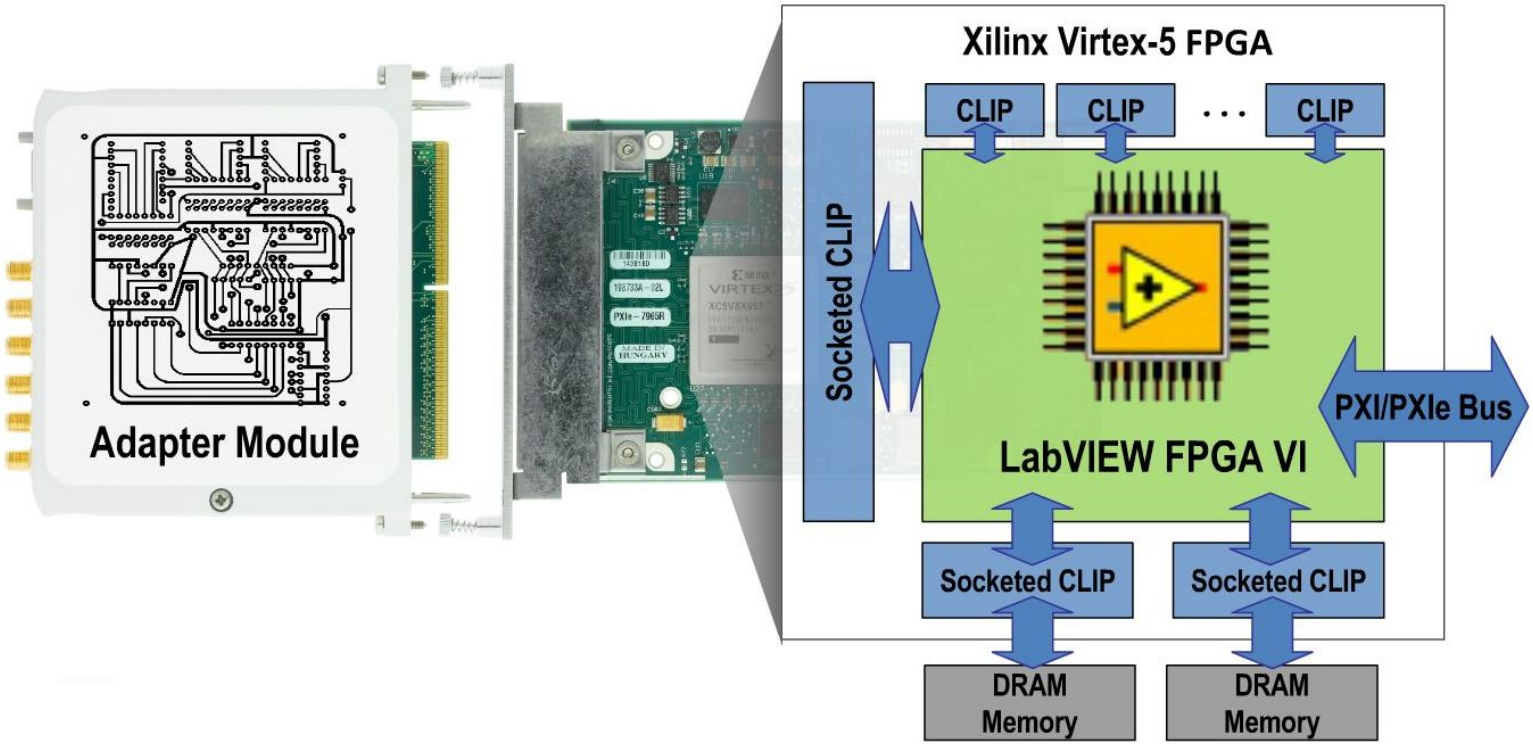
- Test vector generation & comparison
- Interface CODECs
- Timers, triggers, aob
- on-board DRAM Memory

Backbone

Picture source: http://www.ni.com/pxi/

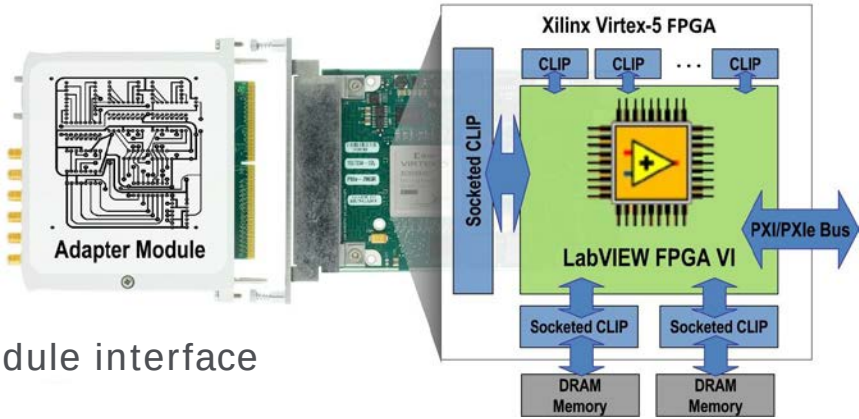
- Intel PC module running Labview main program
- PXI/ PXIe interconnects
- Clocking/ triggering
- Power/ cooling

LabView FPGA and Adapter Module



Picture source: http://www.ni.com/pxi/

SpaceWire Interface Test



Picture source: http://www.ni.com/pxi/

- Adapter Module
  - COTS LVDS interface
- FPGA Module
  - CLIP: 2x SpW CODEC IP
  - Socketed CLIP: PXIe & adapter module interface
  - LabView FPGA VI as glue logic
- Test Scenario
  - Data transfer to Spacewire test equipment
  - Data transfer between 2 Spacewire CODECs
  - PXIe Data transfer between backbone PC and Spacewire CODEC

SpW Test Results

- Test Results
  - Successful integration of Spacewire IP core
  - Data rate up to 400Mbps
  - no bottlenecks in PXIe data streaming

Picture source: http://www.ni.com/pxi/

- FPGA Resource Usage (Virtex-5 SX95T)
  - Labview FPGA infrastructure 13%
  - SpW CODEC
    - Stand-alone 1%
    - Integrated as CLIP 14%
    - 2, 4, 8 SpW CODECS as CLIP 16, 21, 27%

Conclusion & Outlook

- Test and verify project deliverable HW
  - One system for all projects
  - Extended EGSE functionality
  - Independent failure investigation
- Versatile FPGA based DSP capabilities
  - Test pattern generation
  - Test pattern comparison
  - Precise timing of test vectors
- Planned tasks
  - Implementing SpaceFiber codec in FPGA
  - Implementing SpaceWire and SpaceFiber adapter module
  - Developing test setup for upcoming GSTP projects

Picture source: http://www.ni.com/pxi/

Thank you for your attention

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NI FlexRIO FPGA Modules for PXI

- Virtex-5 FPGA
  - LX30, LX50, LX85, LX110
- Direct access to FPGA I/O
  - 132 single-ended lines or 66 differential pairs
  - 400 Mbps single-ended
  - 1 Gbps differential
- 128 MB onboard DRAM
  - 2x 64 MB banks
  - 800 MB/s per bank
- Adapter module required for I/O

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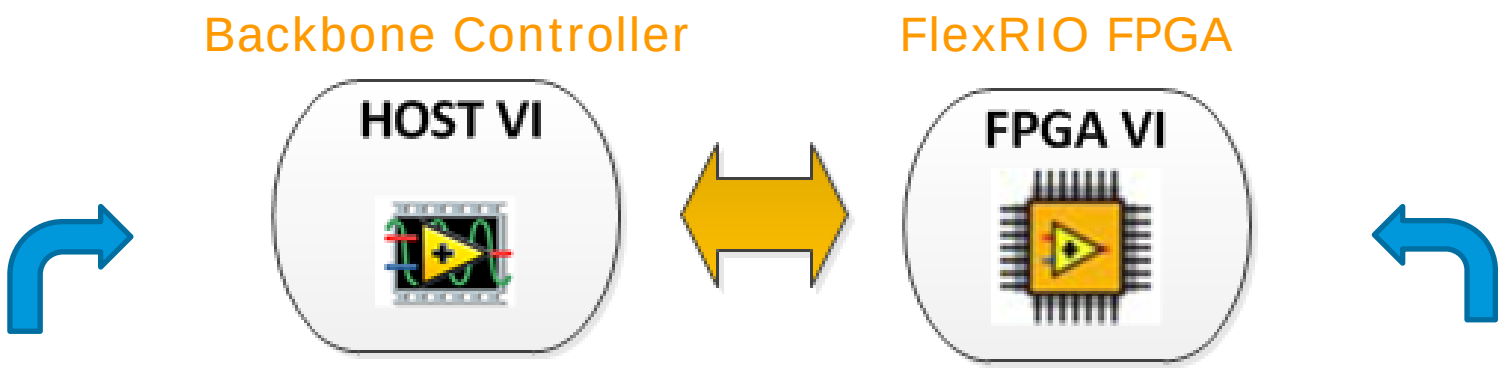
FPGA Configuration

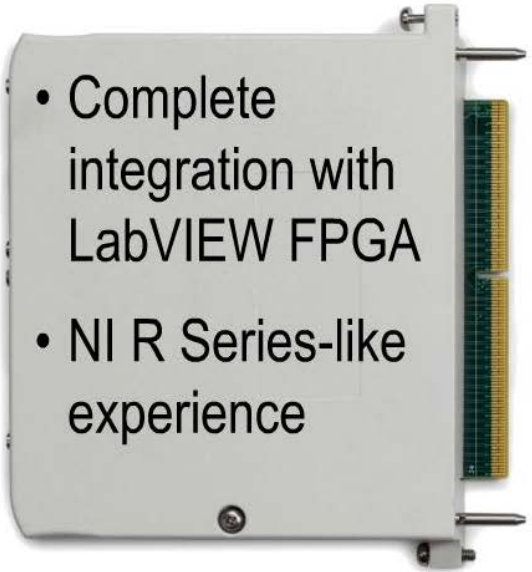


- Implemented within Labview PC program
- FPGA configuration
- Control of data flow

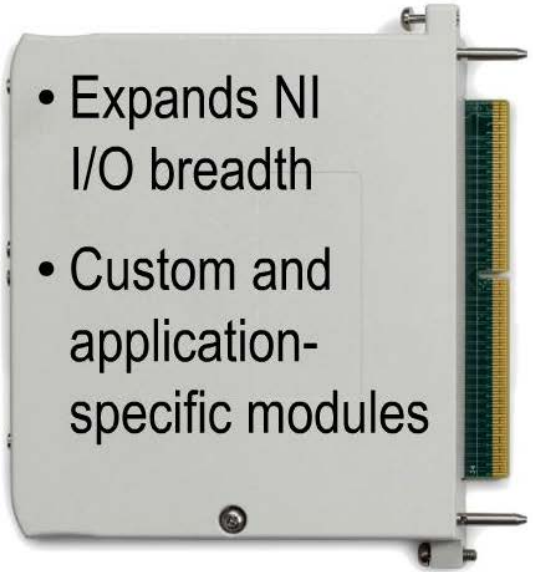
- Implements Labview FPGA environment
- Contains Labview FPGA program
- IP core integration

NI FlexRIO Adapter Modules

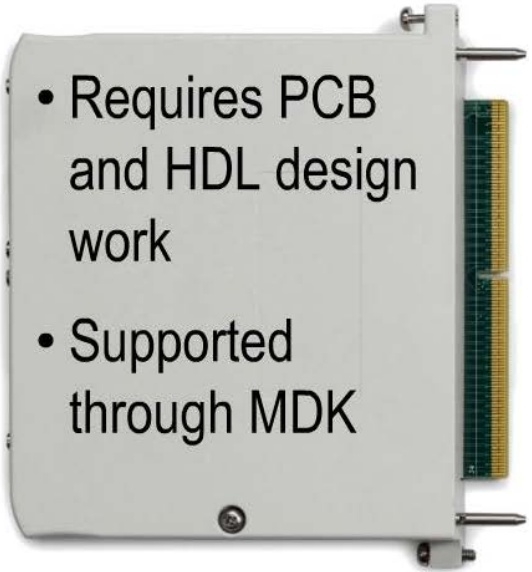
NI Modules



Third Party Modules



Custom Modules



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NI FlexRIO Adapter Module Development

Hardware
- PCB
- Firmware
- LabVIEW FPGA

Software
- API
- Application
- Examples

Mechanical
- PCB
- Connectors
- Thermal

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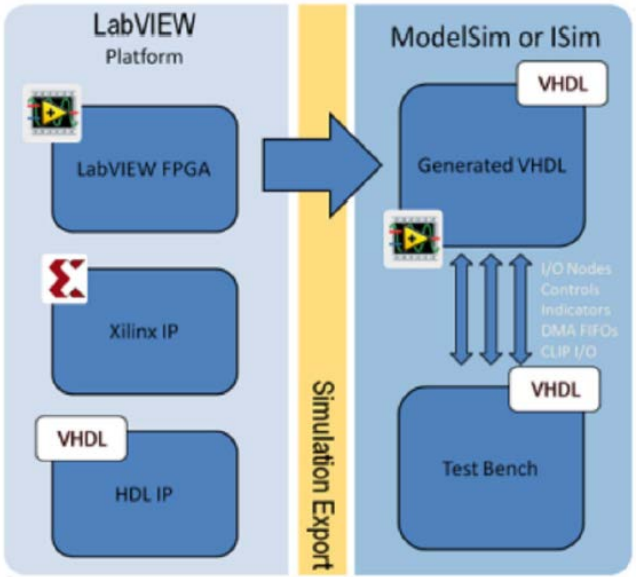
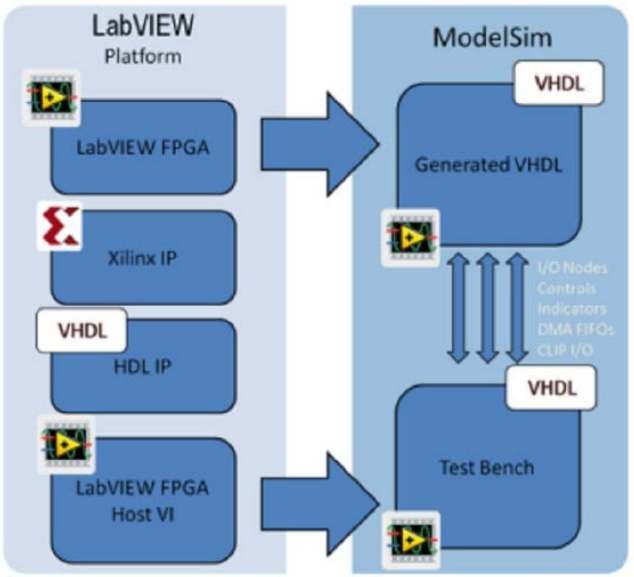
FPGA Verification

Co-simulation with ModelSim

OR

Realization of VHDL Test Bench & use of a third party simulator (ModelSim or ISIM)





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