MOST (Modelling of SpaceWire Traffic)

MTG-I simulation presentation

05/10/2012

Ref.:

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ThalesAlenia Space

A Thales / Finmeccanica Company

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INTRODUCTION, HISTORY and CONTEXT

MTG SpaceWire Network – MOST presentation (1/5)

- MOST **(Modelling of SpaceWire Traffic)** was initially developed in year 2006 by TAS-F and was based on OPNET toolkit 12.0. It is supported by ESA since 2010:
  - To support SpW network **design** and **optimization**
  - To allow SpW networks **performances analysis** from the beginning, without waiting for system testing phase
  - To offer a progressive tool for SpW experts who would like to integrate **specific SpW components**, or, to update existing library with regard to **standard upgrades**
- MOST has been presented at DASIA 2007, at ISC 2010, DASIA 2011, DASIA 2012 and multiple SpW working groups

MOST is the result of a continuous and intensive development effort

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MTG SpaceWire Network – MOST presentation (2/5)

- Current steps of development:
  - Validated simulator delivery and installation in ESA facilities in Q4 2011
  - TAS: simulation activities & continuous development
  - ESA: simulation activities & development of specific needs
  - Now: merging of both developments, adding of new features & new simulation activities to come

- People involved in MOST:
  - ESA:
    - David Jameux
  - 4Links:
    - Barry Cook
    - Paul Walker
  - Scisys:
    - Peter Mendham
    - Stuart Fowell
  - TAS-F Cannes:
    - Brice Dellandrea
    - Philippe Fourtier
    - Loic Parent
    - Baptiste Gouin

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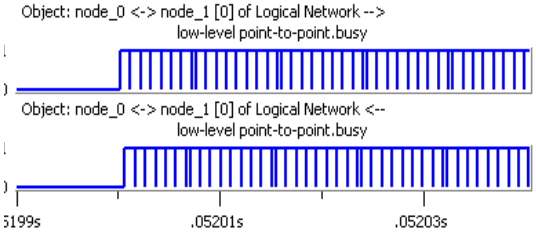
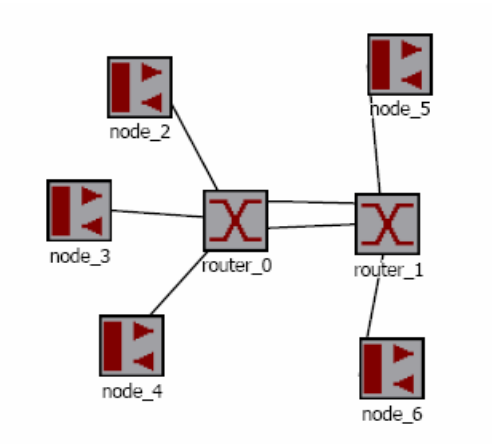
MTG SpaceWire Network – MOST presentation (3/5)

MOST simulator is dedicated to the following users:

- System engineers who have to design network topology and to perform validation tests
- Developers who would need to test new component features or protocol





MOST can be used during all phases of a project:

§ During early steps of projects, MOST mainly plays a role in the following design activities :

§ Phase A and before : performs evaluations, starting from a preliminary specification of network and nodes

§ Phase B : consolidate design by enhancing and completing nodes models behavior in terms of data provider and consumer

§ During development steps of a project, MOST participates to :

§ Phase C, D : design, validation and investigation

§ During maintenance step of a project, MOST takes part to :

§ Phase E : investigations, support to very specific operations

METOP-SG SpaceWire Network – MOST presentation (4/5)

- Exemple of available statistics:
  - The buffer size of a module
  - Output port attribution of the router :
    - This shows which output port of the router has been used to route a packet in function to the simulation time.
  - Transmission of each character on a link :
    - This statistics shows the traffic flow on a link, showing each byte as a function of the simulation time.
  - End-to-End delay (seconds):
    - This shows the value in seconds for a packet to transit from the source node to the destination node. Possible to obtain ETE per packet type (SC, CMD, HK, TM…)
  - End-to-End delay round trip (seconds):
    - This statistics enables to know the time taken by a node to receive the response of its command.

MTG SpaceWire Network – MOST presentation (5/5)

- The following library has been developed, tested with 2 representative study cases, cross-validated through comparison with real hardware and extensively used on MTG-simulation:
- Nodes: Generic nodes to test developed protocols
- Protocols:
  - SpaceWire Links, nodes, routers and networks
  - RMAP
  - Packet Transfer Protocol
- Components:
  - SPW 10X Router
  - SMCS116SPW & SMCS332SPW
  - Remote Terminal Controller
  - ***New from MTG-I: Generic Buffer coupling node (for instruments)***
  - ***New from MTG-I: Generic Virtual Channel Multiplexer (for MTG DDU)***
- Links: SpaceWire link

MOST allows simulation of networks based on currently available components

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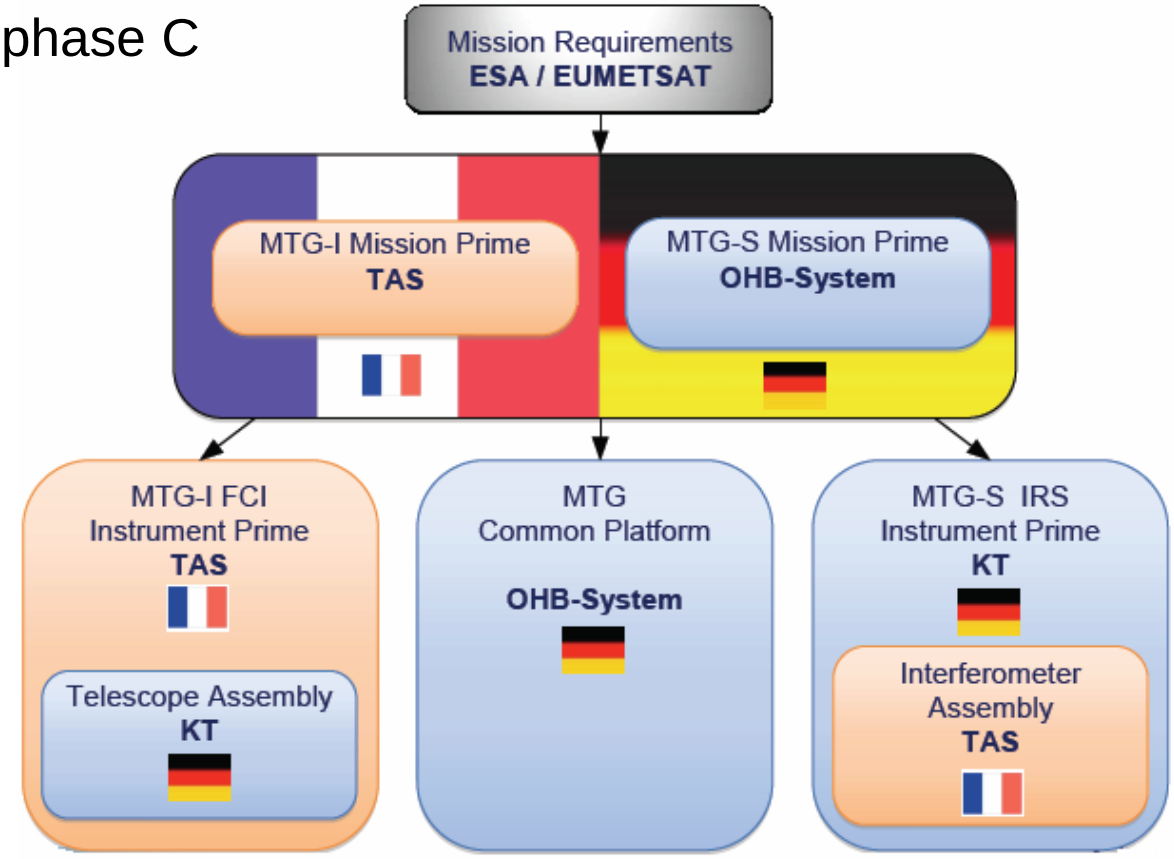
MOST MTG-I Simulation: overview

MTG SpaceWire Network – MTG-I simulation overview (1/4)

- MTG is a six-satellite system of:
  - 4 imaging satellites (MTG-I)
  - 2 satellites equipped with atmospheric sounders (MTG-S)
- First launch in 2017, currently in phase C
- ESA: Procurement authority
- EUMETSAT: End User
- TAS: MTG & MTG-I Prime
- OHB: MTG-S Prime
- **MTG-I instruments:**
  - FCI (Flexible Combined Imager)
  - LI (Lighting Imager)
  - DCP (Data Collection Plaform)
  - S&R (Search & Rescue relay)
- MTG-S instruments:
  - IRS (InfraRed Sounding)
  - UVN (Ultraviolet, Visible & Near-infrared sounding mission)



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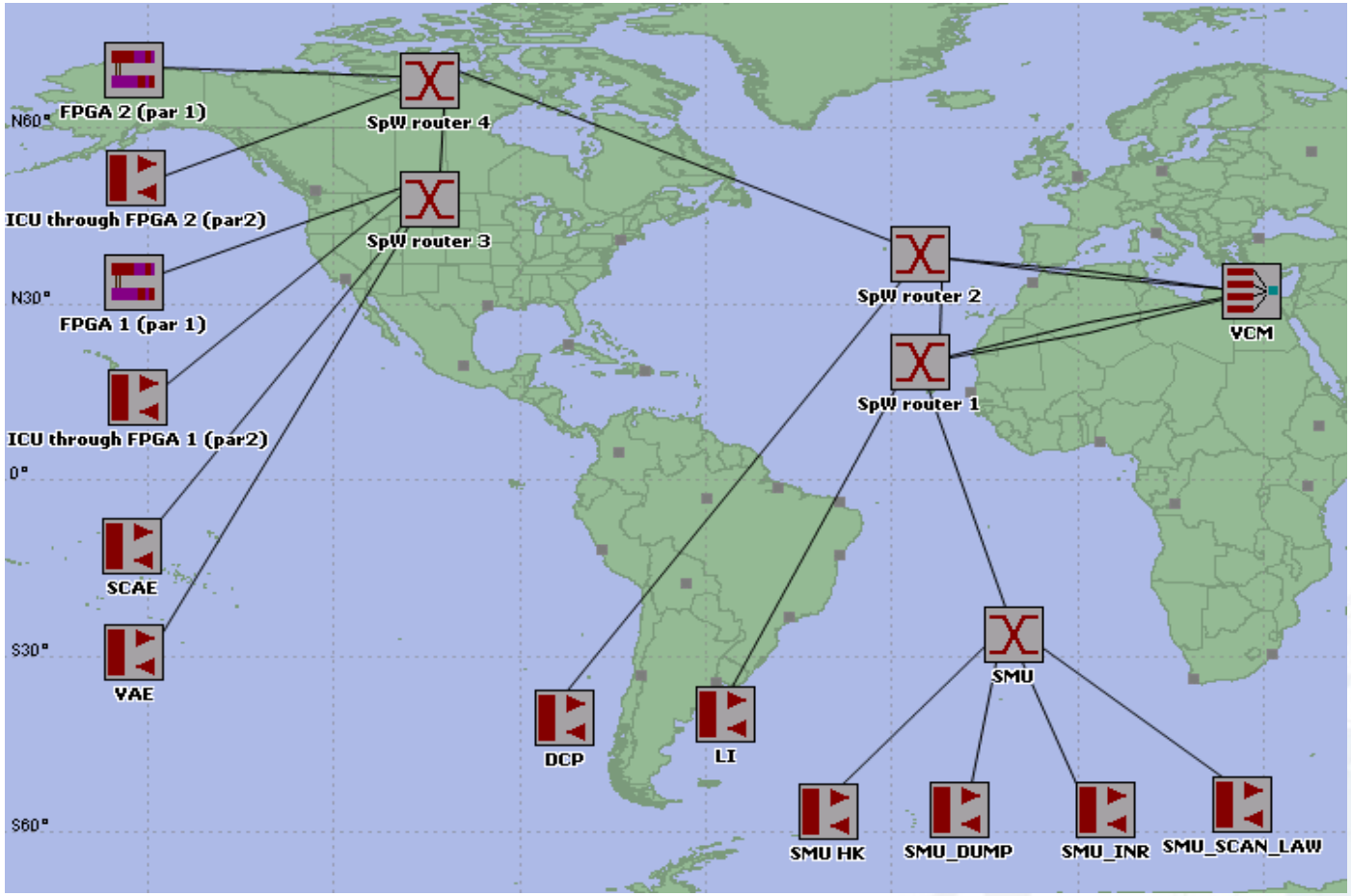
MTG SpaceWire Network – MTG-I simulation overview (2/4)

- MOST simulation of the MTG-I Topology:
  - **3 instruments, 1 SMU, 1 DDU incl. routing function & VC Multiplexing**
  - DDU is the Data Distribution Unit performing payload data multiplexing and conditionning (virtual channel multiplexing, CCSDS framing, encryption, coding)



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MTG SpaceWire Network – MTG-I simulation overview (3/4)

- Other MTG Constraints
  - Transmittion of packets over the network according to SpW PTP
  - Compliance to ECSS-E-ST-50-12C, ECSS-E-ST-50-51C, ECSS-E-ST-50-52C, ECSS-E-ST-50-53C
  - **Network shall support maximum spacewire interruption or delay up to 2ms**
  - Some instrument transmitting nodes **have no buffer** and rely on **coupling nodes** with buffer capability (either character forwarding or packet forwarding)
  - MOST shall analyse:
    - All SpaceWire buffers occupancy and variation
    - DDU and Virtual Channels behavior
    - Margins of each SpaceWire link according to the specified link-rate
    - Latency between packet generation and reception on the correct VCA shall be measured
    - Effect of 2ms failure of the DDU (Data Distribution Unit)
    - Impact of character forwarding instead of packet forwarding

à 3 study cases: network with packet forward, character forward, and worst-case with 2ms traffic stall

MTG SpaceWire Network – MTG-I simulation overview (4/4)

- Coupling Node to provide buffer capabilities
  - 2 ways of operation settable by an attribute: packet or character forwarding

- Virtual Channel Multiplexer Node to simulate MTG-I DDU behaviour
  - Settable “Bandwidth Allocation Table” with modular number of slots (here: 32)
  - Round-Robin capability if not enough data is present to generate a CCSDS frame

DDU

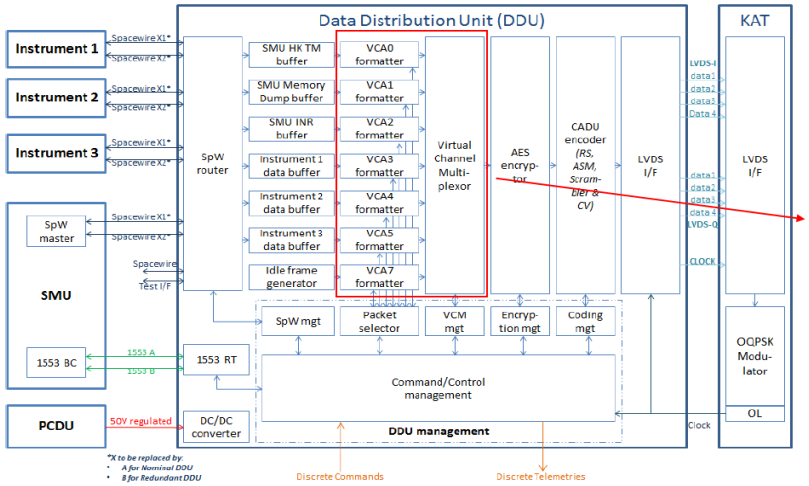
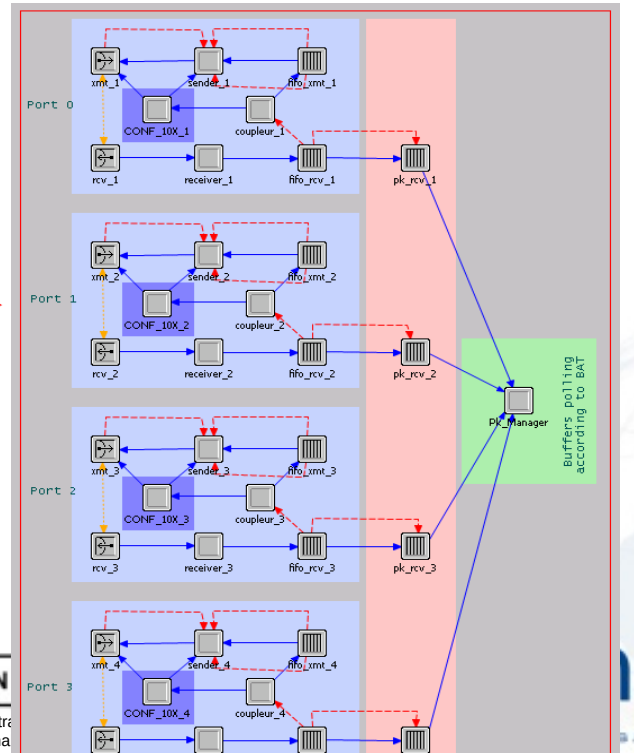


Figure 4-1: Detailed Data Distribution Unit (DDU) structure (indicative only) (ID: PDD-DDU_209)



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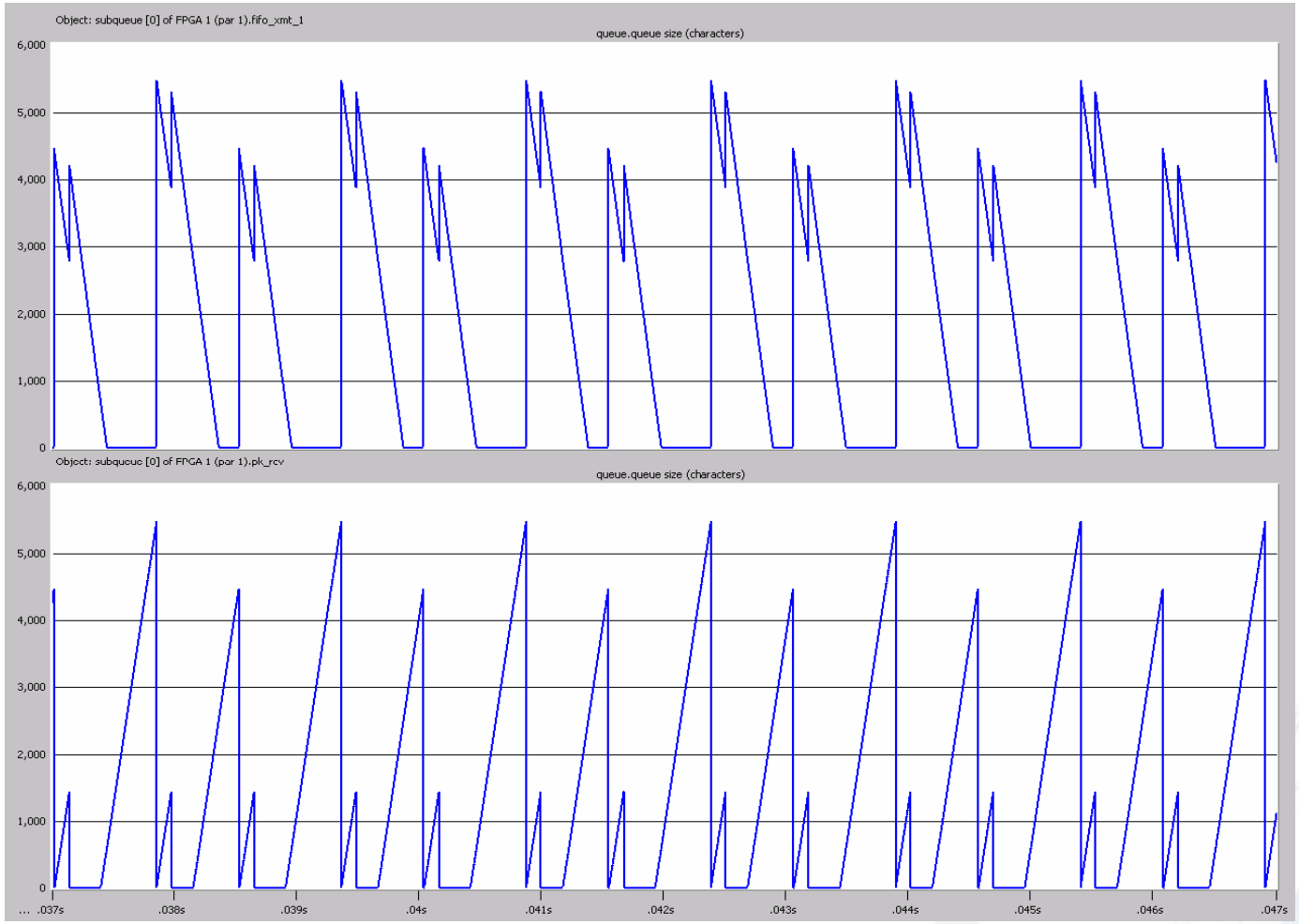
Study Case 1: MTG-I network with **packet forwarding** capability of FCI coupling nodes

(including worst-case traffic condition at 50 ms corresponding to a synchronization of emission time of multiple packets, creating congestion)

MTG SpaceWire Network – Study case 1: packet forward (1/10)

FCI/FPGA 1 Coupling Buffer occupation and variation

- The maximal FPGA 1 buffer occupation in worst-case is **5861** characters



Tx buffer

Rx buffer

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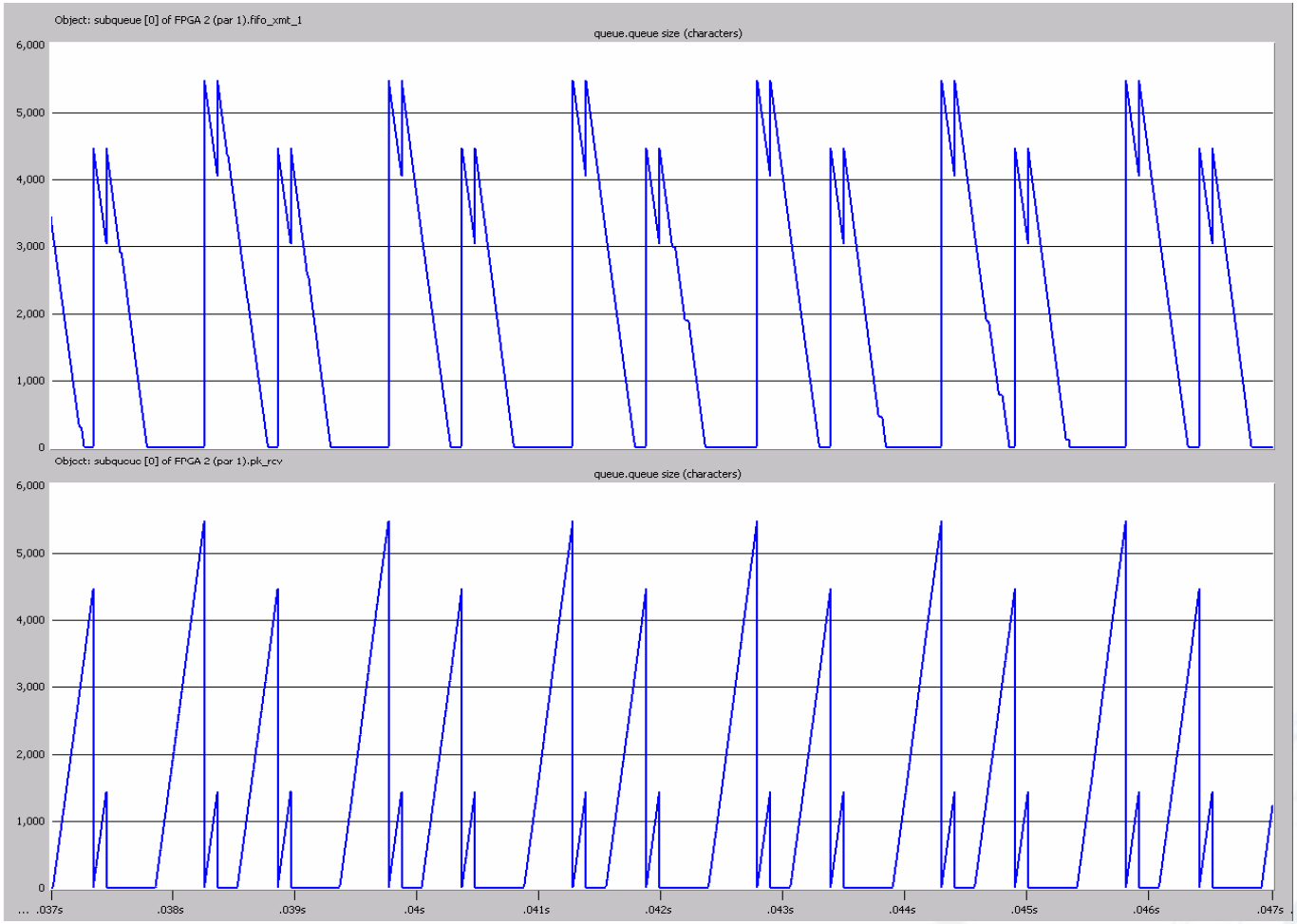
MTG SpaceWire Network – Study case 1: packet forward (2/10)

FCI/FPGA 2 Coupling Buffer occupation and variation

- The maximal FPGA 2 buffer occupation in worst-case is **5465** characters



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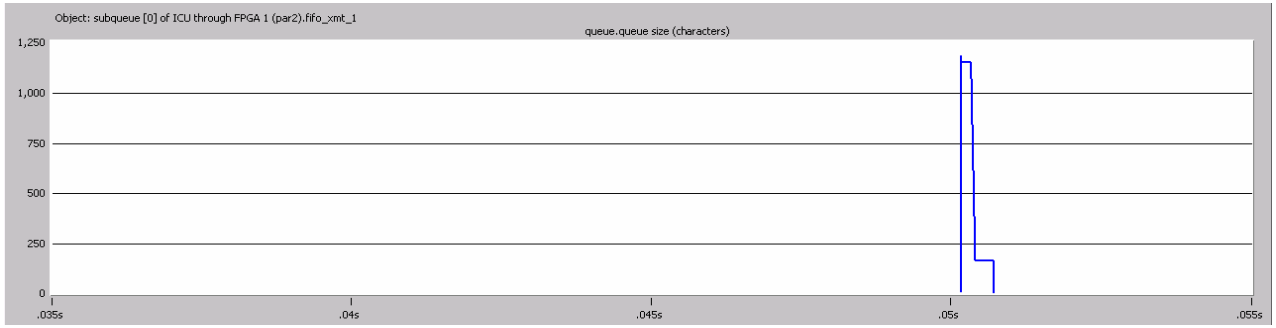
MTG SpaceWire Network – Study case 1: packet forward (3/10)

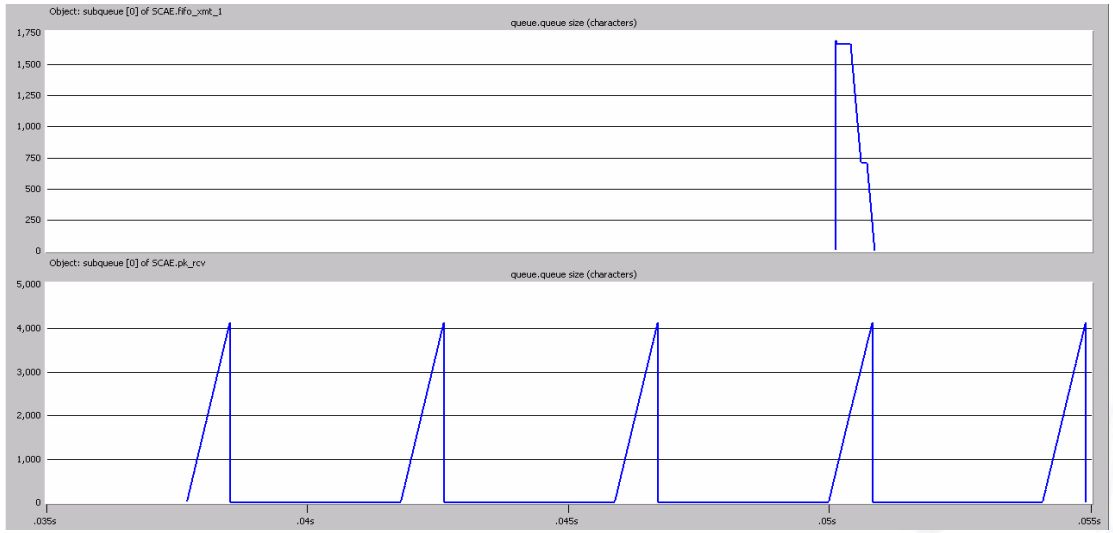
FCI/ICU Buffer occupation and variation

- The maximal ICU buffer occupation in worst-case is **1183** characters



FCI/SCAE Buffer occupation and variation

- The maximal SCAE buffer (rx+tx) occupation in worst-case is **5792** characters



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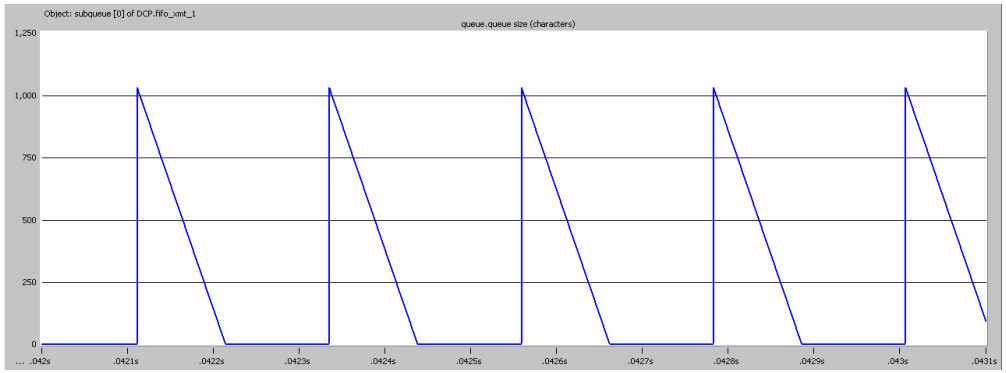
MTG SpaceWire Network – Study case 1: packet forward (4/10)

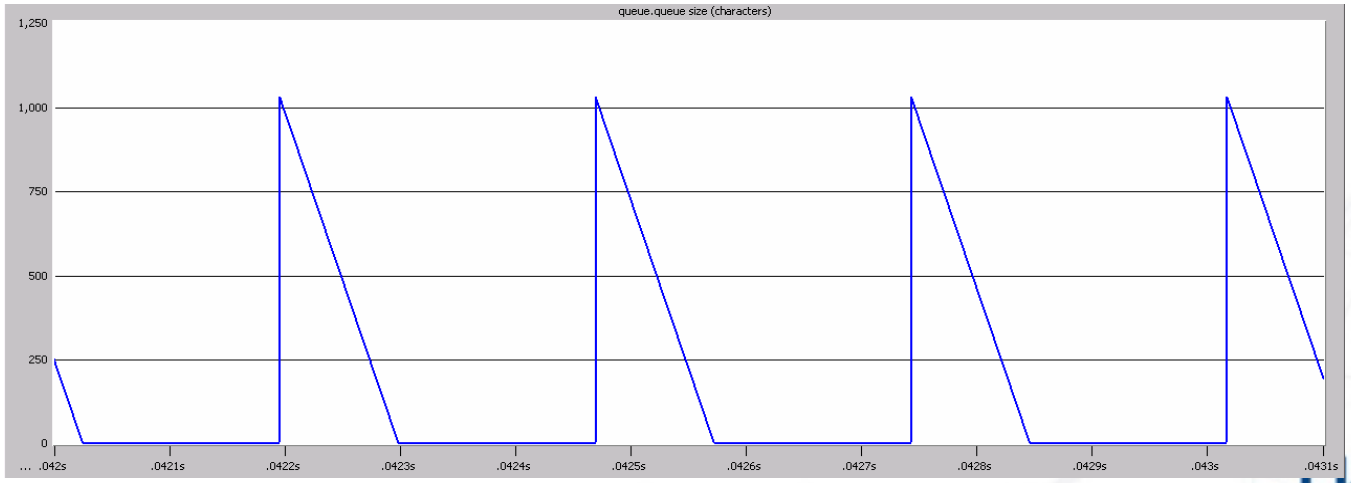
DCP Buffer occupation and variation

- The maximal DCP buffer occupation in worst-case is **1029** characters



LI Buffer occupation and variation

- The maximal LI buffer occupation in worst-case is **1029** characters



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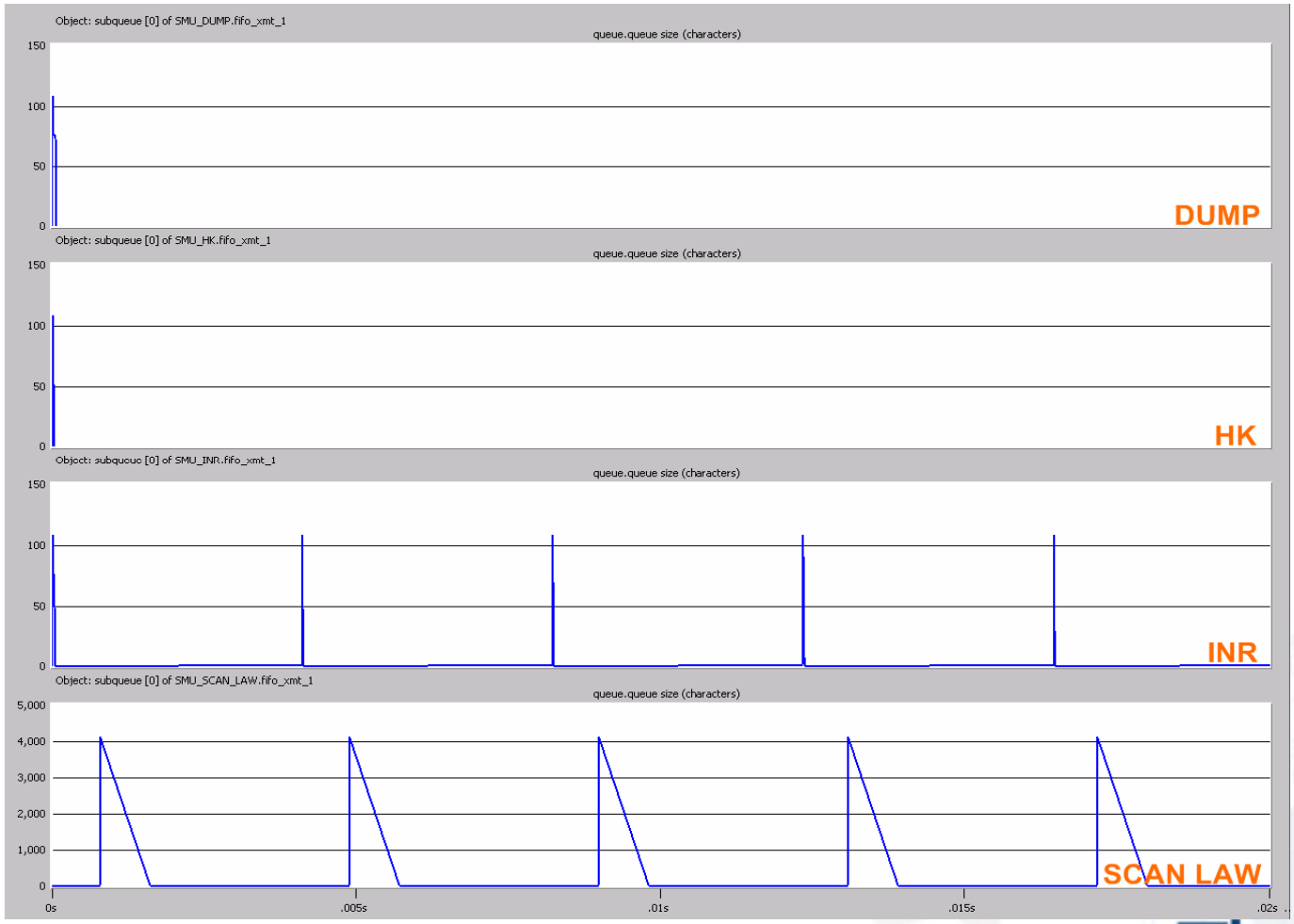
MTG SpaceWire Network – Study case 1: packet forward (5/10)

SMU Buffer occupation and variation

- The maximal SMU buffer occupation (all source nodes cumulated) in worst-case is **4109** characters



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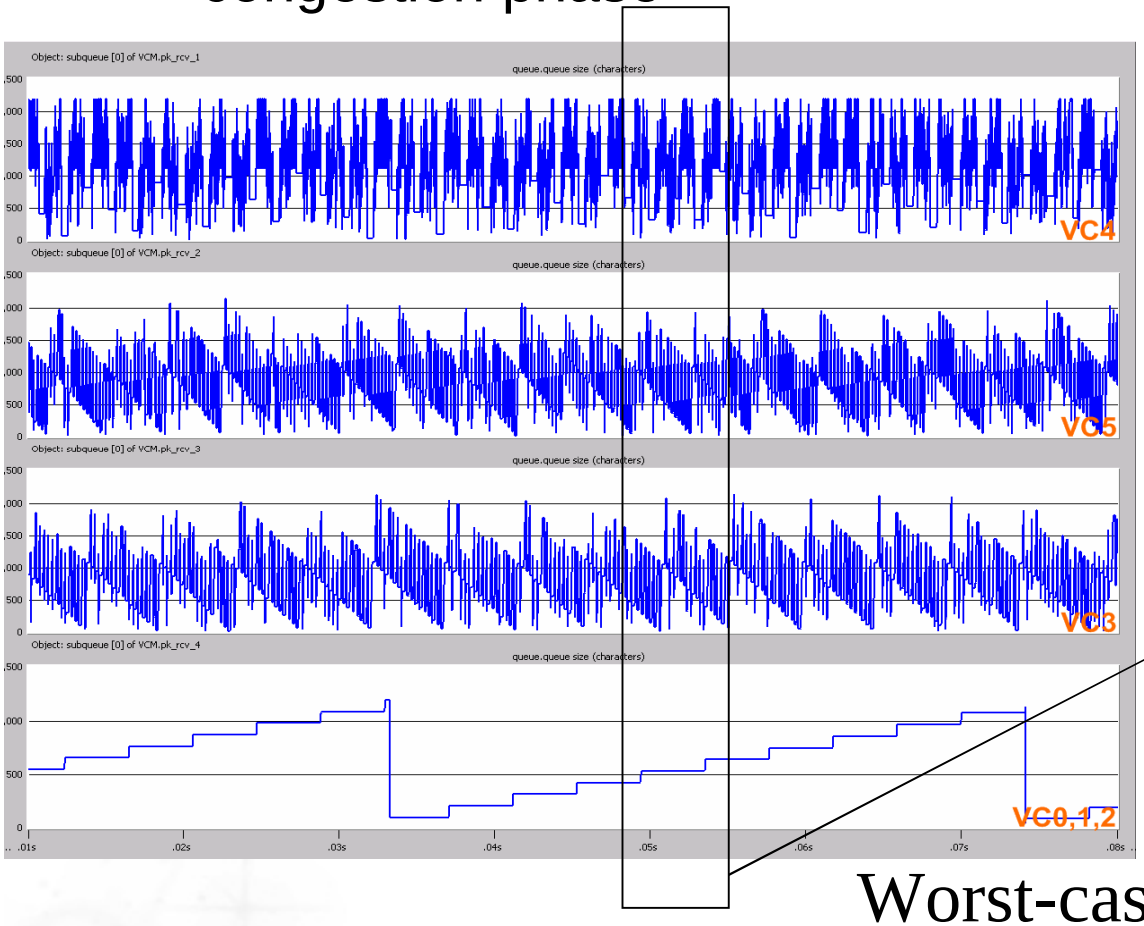
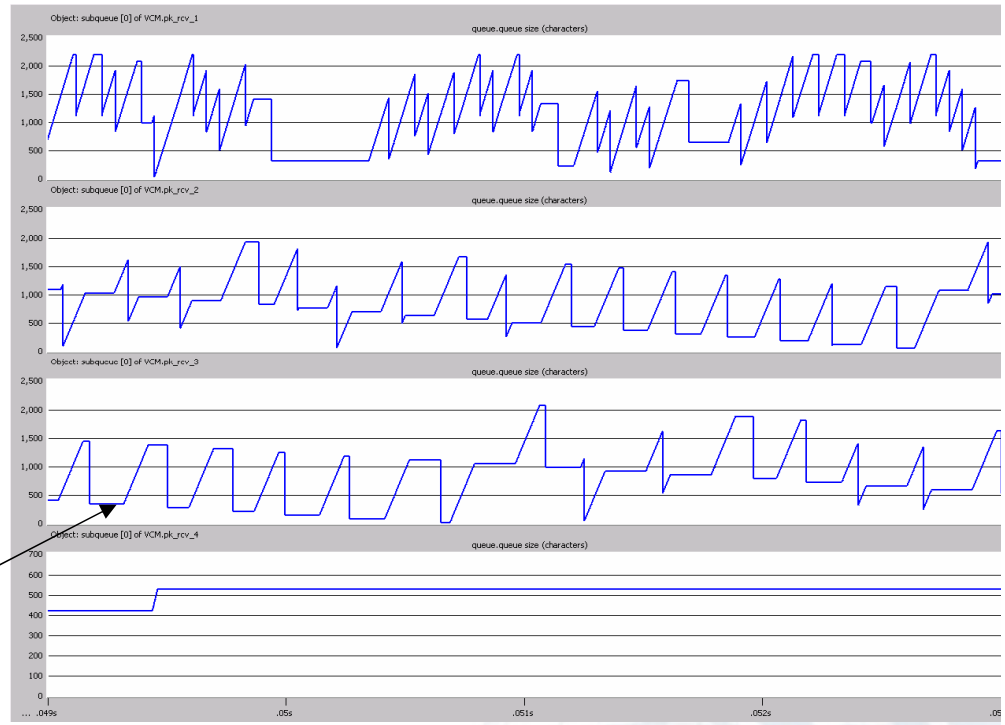
MTG SpaceWire Network – Study case 1: packet forward (6/10)

DDU/VCM Buffer occupation and variation

- Saturation is reached for VC4, VC5, VC3. Never for VC0,1,2 even in congestion phase





Worst-case zoom

MTG SpaceWire Network – Study case 1: packet forward (7/10)

DDU behavior

- DDU is programmable with a Bandwith Allocation Table (BAT), and implements a Round-robin search mechanism
- First DDU searches for allocated input buffer to generate CCSDS Frames
- If not enough data is available in this buffer, then perform a round-robin search on other inputs
- The green lines shows were actual allocated slots have been transferred w/o round-robin search

Simulation Time	Slot allocated in BAT	Slot selected with Round-Robin Algorithm
0,05005	VC4->	->VC5
0,050105	VC5->	No frame
0,050159	VC4->	No frame
0,050214	VC3->	->VC5
0,050269	VC4->	->VC3
0,050324	VC5->	No frame
0,050378	VC4->	No frame
0,050433	VC3->	->VC4
0,050488	VC4->	->VC5
0,050543	VC5->	->VC4
0,050597	VC4->	->VC4
0,050652	VC3->	->VC3
0,050707	VC4->	->VC4
0,050761	VC5->	->VC5
0,050816	VC0,1,2->	->VC4
0,050871	VC0,1,2->	->VC4
0,050926	VC0,1,2->	->VC5
0,050980	VC5->	->VC4
0,051035	VC4->	->VC4
0,051090	VC3->	->VC3
0,051144	VC4->	->VC4
0,051199	VC5->	->VC5
0,051254	VC4->	->VC3
0,051309	VC3->	->VC4
0,051363	VC4->	->VC4
0,051418	VC5->	->VC5
0,051473	VC4->	->VC4
0,051528	VC3->	->VC4
0,051582	VC4->	->VC3
0,051637	VC5->	->VC5
0,051692	VC4->	->VC4
0,051746	VC3->	No frame
0,051801	VC4->	No frame
0,051856	VC5->	->VC5
0,051911	VC4->	->VC4
0,051965	VC3->	->VC3
0,05202	VC4->	->VC4

MTG SpaceWire Network – Study case 1: packet forward (8/10)

Links usage & occupation

- The higher link usage is 63.42% inside the FCI (character transfer time versus link capability), whereas maximal link/port occupation is 73.5%.

	Link usage	**Link occupation** *(incl. congestion delays)*		
	T_{char} / $T_{simulation}$	Average usage (Mean + $T_{FCT/2}$)	Accuracy (+/- $T_{FCT/2}$)	**Upper bound (Mean + T_{FCT})**
R3 -> R4 *(1)*	60.77 %	62.88 %	0.18 %	63.07 %
R4 -> R3 *(2)*	10.35 %	22.03 %	1.51 %	23.54 %
R4 -> R2 *(3)*	60.58 %	65.22 %	0.18 %	65.41 %
R2 -> R4 *(4)*	10.34 %	22.02 %	1.51 %	23.53 %
R1 -> R2	7.33 %	20.52 %	0 %	20.52 %
R2 -> R1	0.37 %	0.37 %	-	0.37 %
FPGA2 -> R4 *(5)*	63.23 %	66.47 %	1.51 %	67.97 %
R4 -> FPGA 2 *(6)*	63.40 %	64.34 %	1.51 %	65.84 %
VAE -> R3 *(7)*	70.51 %	70.52 %	0 %	70.52 %
R3 -> VAE	3.53 %	3.53 %	-	3.53 %
ICU -> R3	0.087 %	0.55 %	0 %	0.55 %
R3 -> ICU	0.004 %	0.004 %	-	0.004 %
SCAE -> R3	1.7 %	1.4 %	0.51 %	1.92 %
R3 -> SCAE	20.55 %	20.55 %	0.02 %	20.56 %
FPGA1 -> R3 *(8)*	63.12 %	63.95 %	1.5 %	65.46 %
R3 -> FPGA1*(9)*	63.42 %	71.99 %	1.5 %	73.5 %
DCP -> R2	45.93 %	45.93 %	0 %	45.93 %
R2 -> DCP	2.3 %	2.3 %	-	2.3 %
LI -> R1	37.51 %	37.51 %	0 %	37.51 %
R1 -> LI	1.88 %	1.88 %	-	1.88 %
SMU -> R1	21.09 %	21.09 %	0 %	21.09 %
R1 -> SMU	1.06%	1.06 %	-	1.06 %

- Link occupation presents the allocation of a link to a packet and is measured in MOST as a port allocation to a given transmission in a router.

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MTG SpaceWire Network – Study case 1: packet forward (9/10)

End-to-end delays

Delay	DCP	ICU	SCAE	VAE	DUMP	HK	INR	LI
Max	665.6µs	964.5µs	1.32ms	1.52ms	33.31ms	33.31ms	41.21ms	707.8µs
Min	233.9µs	800.4µs	663.7µs	1.06ms			4.13ms	278.2µs
Average	347.7µs	882.5µs	952.5µs	1.26ms			20.27ms	405.1µs
95% after *(2 sigma)*	492µs	Not relevant	1.24ms	1.44ms			37.10ms	564µs

- The end-to-end delay is computed as the duration between packet generation in the Source Node and its consumption by the VCM (frame removing and sending toward board/ground link).

- DUMP, INR and HK packets end-to-end delays are affected by the merging of VC0,1 and 2 in the simulation, and should be approximately 100 ms in real conditions.

MTG SpaceWire Network – Study case 1: packet forward (10/10)

- Study Case 1 Synthesis
  - The traffic congestion triggered at 50ms has no impact on the DDU VCM
  - Output port arbitration operated by “Router 3” creates a little increase of FPGA 1 coupling buffer occupation in worst-case phase
  - ETE delays are under 42ms for all sources (including worst-case phase)
  - BAT polling coupled with Round-Robin mechanism reduces Virtual Channel saturation by reallocating VC0,1,2 time slots when no frame is available

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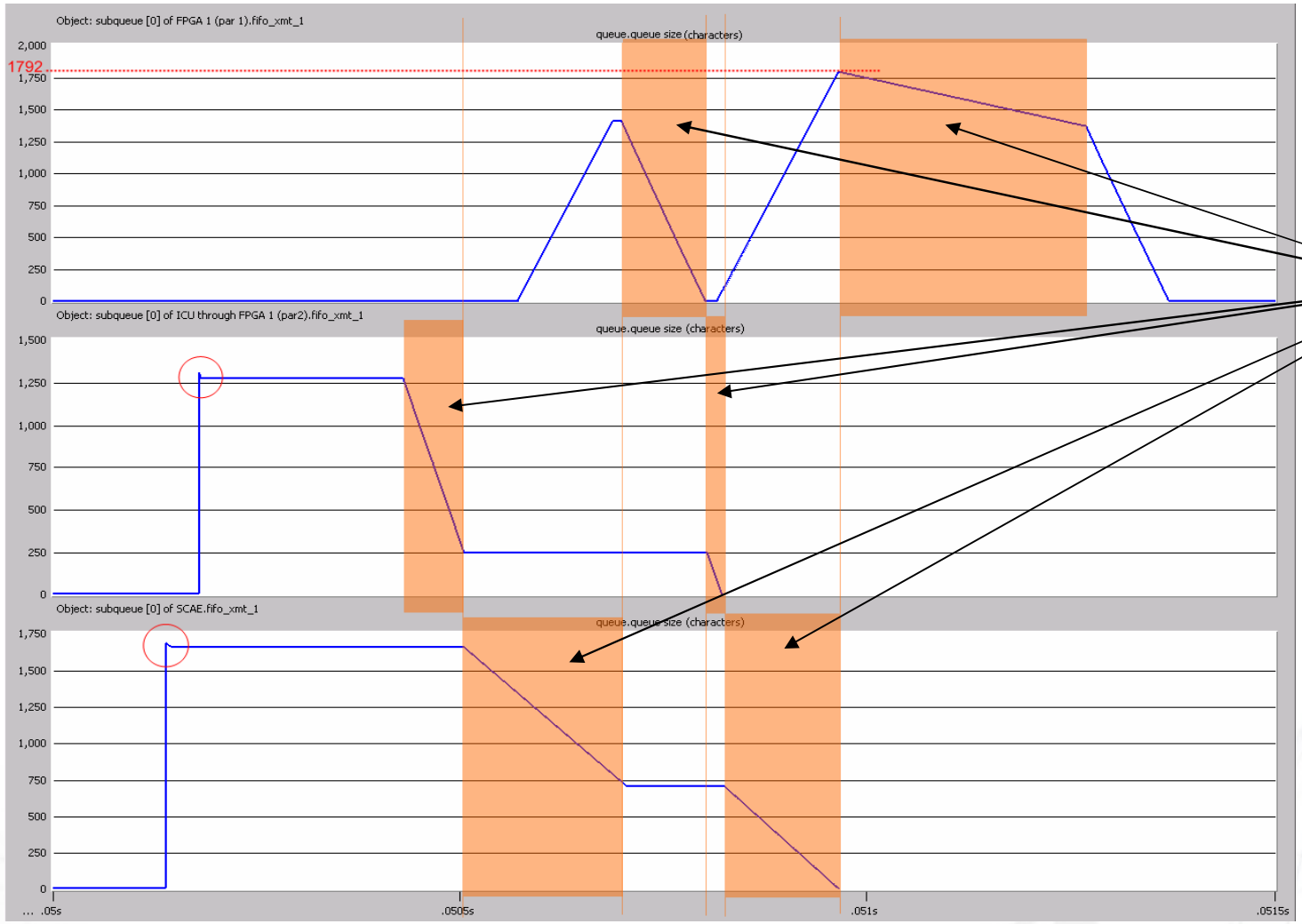
Study Case 2: MTG-I network with **character forwarding** capability of FCI coupling nodes

(including worst-case traffic condition at 50 ms corresponding to a congestion in DDU VCM)

MTG SpaceWire Network – Study case 1: character forward (1/5)

FCI/FPGA 1 Coupling Buffer occupation and variation

- The maximal FPGA 1 buffer occupation in worst-case is **1792** characters

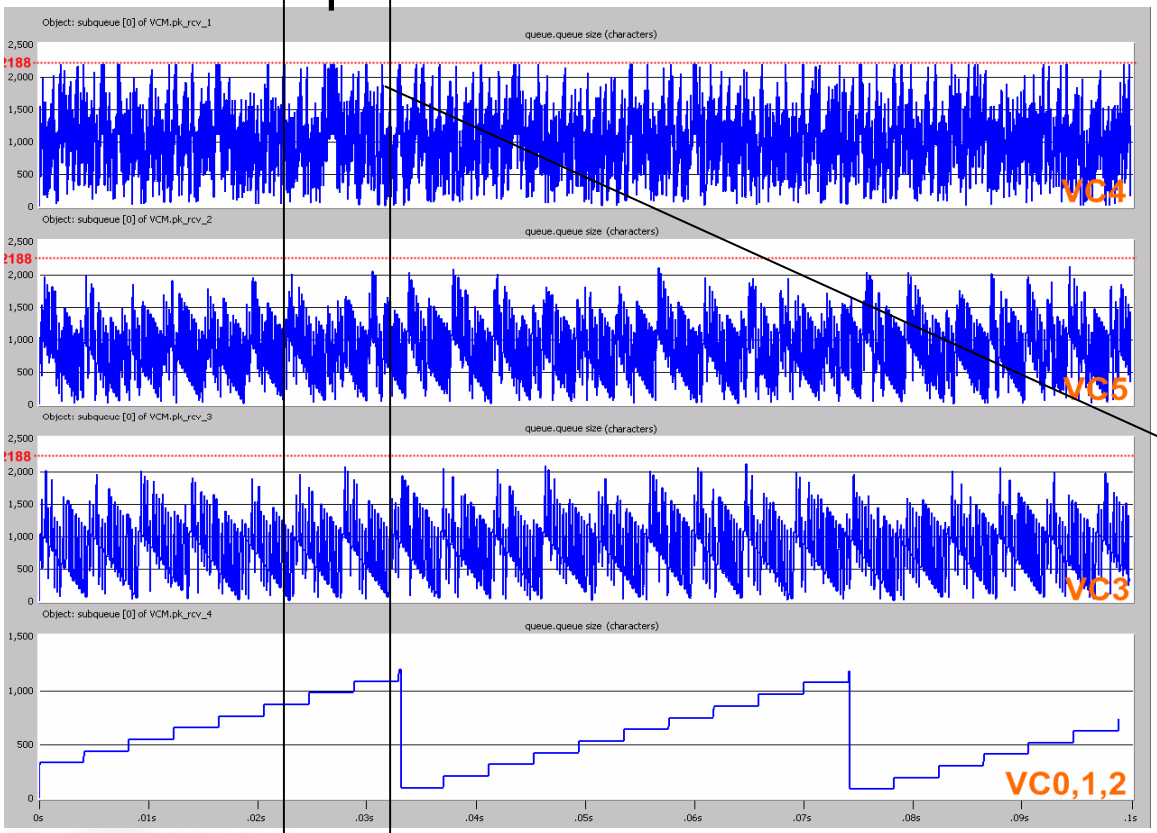


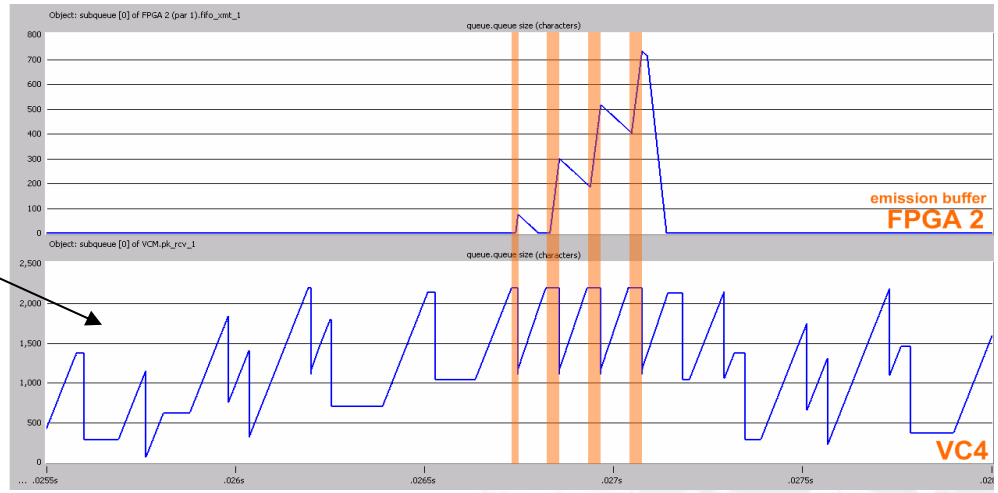
Router 3 arbitration

MTG SpaceWire Network – Study case 1: character forward (2/5)

DDU/VCM Buffer occupation and variation

- Saturation is reached for VC4. Never for VC3, VC5 and VC0,1,2 over the 100 ms of simulation
- Saturation of VC4 around 27ms creates an increase of FPGA2 buffer occupation





Worst-case zoom

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MTG SpaceWire Network – Study case 1: character forward (3/5)

- Links usage & occupation
  - The higher link usage is 70.58% inside the FCI (character transfer time versus link capability), whereas maximal link/port occupation is 74.53%.

	Link usage	**Link occupation** *(incl. congestion delays)*		
	T_{char} / $T_{simulation}$	Average usage (Mean + T_{FCTi2})	Accuracy (+/- T_{FCTi2})	**Upper bound** (Mean + T_{FCTi})
R3 -> R4 *(1)*	61.16 %	71.37 %	0.18 %	71.56 %
R4 -> R3 *(2)*	10.37 %	22.04 %	1.52 %	23.56 %
R4 -> R2 *(3)*	61.14 %	71.7 %	0.18 %	71.89 %
R2 -> R4 *(4)*	10.37 %	22.04 %	1.52 %	23.56 %
R1 -> R2	7.33 %	20.52 %	0 %	20.52 %
R2 -> R1	0.37 %	0.37 %	-	0.37 %
FPGA2 -> R4 *(5)*	63.81 %	73.01 %	1.52 %	74.53 %
R4 -> FPGA 2 *(6)*	63.81 %	72.69 %	1.52 %	74.21 %
VAE -> R3 *(7)*	70.58 %	70.6 %	0 %	70.6 %
R3 -> VAE	3.53 %	3.53 %	-	3.53 %
ICU -> R3	0.096 %	0.64 %	0 %	0.64 %
R3 -> ICU	0.005 %	0.005 %	-	0.005 %
SCAE -> R3	1.7 %	1.63 %	0.51 %	2.15 %
R3 -> SCAE	20.55 %	20.54 %	0.02 %	20.56 %
FPGA1 -> R3 *(8)*	63.5 %	72.46 %	1.51 %	73.98 %
R3 -> FPGA1 *(9)*	63.5 %	72.07 %	1.51 %	73.58 %
DCP -> R2	45.93 %	45.93 %	0 %	45.93 %
R2 -> DCP	2.3 %	2.3 %	-	2.3 %
LI -> R1	37.51 %	37.51 %	0 %	37.51 %
R1 -> LI	1.88 %	1.88 %	-	1.88 %
SMU -> R1	21.09 %	21.09 %	0 %	21.09 %
R1 -> SMU	1.06%	1.06 %	-	1.06 %

  - It was 63.42% and 73.5% for packet forward.

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MTG SpaceWire Network – Study case 1: character forward (4/5)

End-to-end delays with Character forwarding:

Delay	DCP	ICU	SCAE	VAE	DUMP	HK	INR	LI
Max	609.3µs	855.1µs	895.1µs	775.1µs	33.15ms	33.15ms	41.27ms	703.5µs
Min	230.3µs	417.5µs	280.8µs	191.2µs			4.19ms	278.1µs
Average	340.6µs	636.3µs	560.6µs	461.4µs			20.95ms	396.2µs
95% after *(2 sigma)*	469µs	Not relevant	882.8µs	681.7µs			40.9ms	558.9µs

Vs Packet forwarding:

Delay	DCP	ICU	SCAE	VAE	DUMP	HK	INR	LI
Max	665.6µs	964.5µs	1.32ms	1.52ms	33.31ms	33.31ms	41.21ms	707.8µs
Min	233.9µs	800.4µs	663.7µs	1.06ms			4.13ms	278.2µs
Average	347.7µs	882.5µs	952.5µs	1.26ms			20.27ms	405.1µs
95% after *(2 sigma)*	492µs	Not relevant	1.24ms	1.44ms			37.10ms	564µs

MTG SpaceWire Network – Study case 1: character forward (5/5)

- Study Case 2 Synthesis
  - A VCM saturation (VC4) occurs near 27ms due to
    - a maximization of DDU inputs over the network in this period,
    - an unfavorable reading position in the BAT,
    - a buffer filling just under the “Data Frame” limit prior the reading period, creating an increase in FPGA2 buffer occupation at that time.
  - Output port arbitration operated by “Router 3” creates an increase of FPGA 1 buffer occupation when triggering a traffic congestion in FCI at 50ms
  - ETE delays are under 900µs except for INR packets originated from SMU which reach 42ms
  - The character forwarding process creates a degradation of the FCI port occupation statistics compared to the packet forwarding one: 71.89% R4->R2 port occupation versus 65.41% for packet forwarding
  - BAT polling coupled with Round-Robin mechanism reduce Virtual Channel saturation by reallocating VC0,1,2 time slots when no frame is available

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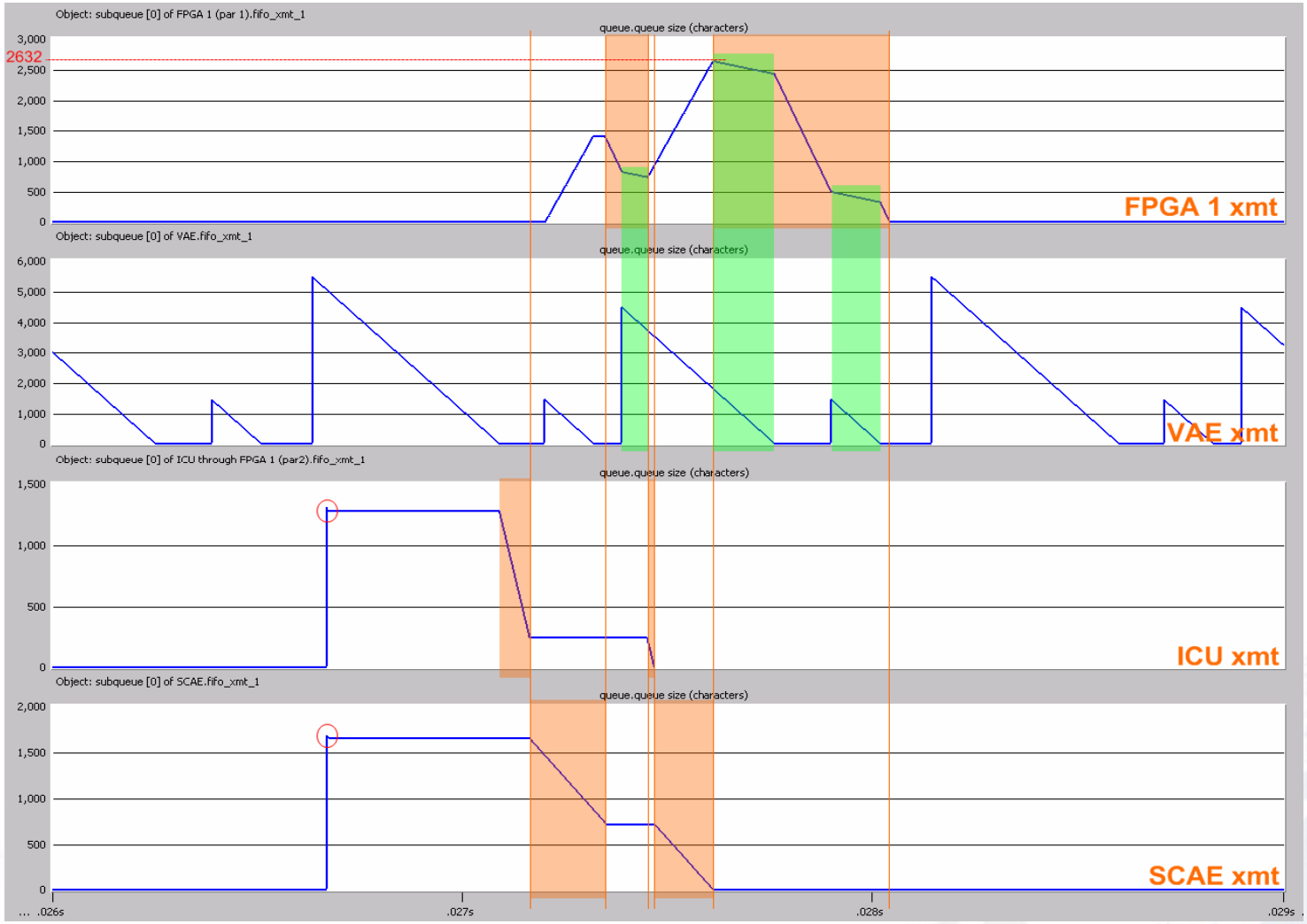
Study Case 3: MTG-I network with character forwarding capability of FCI coupling nodes and 2 ms traffic stall

(including worst-case traffic condition at 27 ms corresponding to a congestion in DDU VCM coupled with a 2 ms DDU VCM stall)

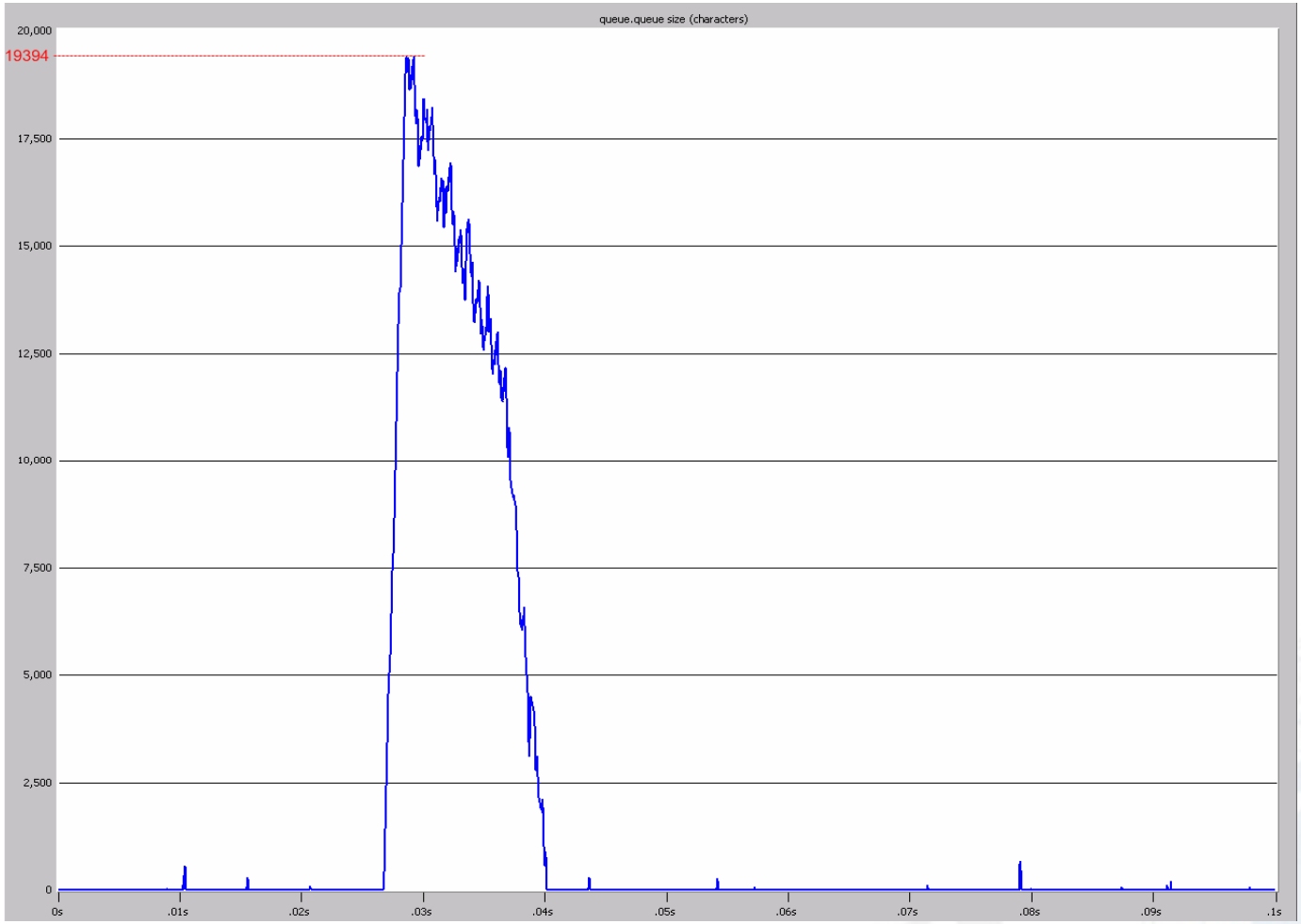
FCI/FPGA 1 Coupling Buffer occupation and variation

- The maximal FPGA 1 buffer occupation in worst-case is **2632** characters



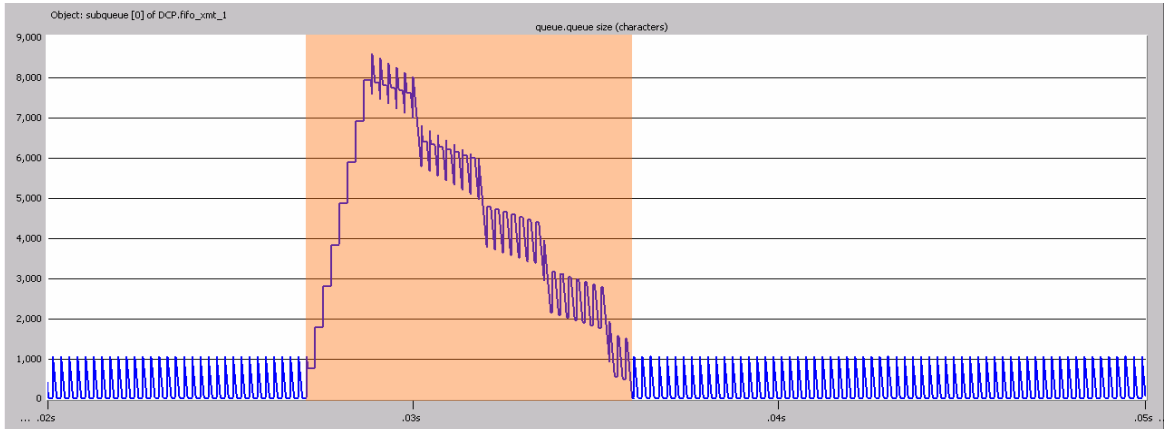
FCI/FPGA 2 Coupling Buffer occupation and variation

- The maximal FPGA 2 emission buffer occupation in worst-case is **19394** characters



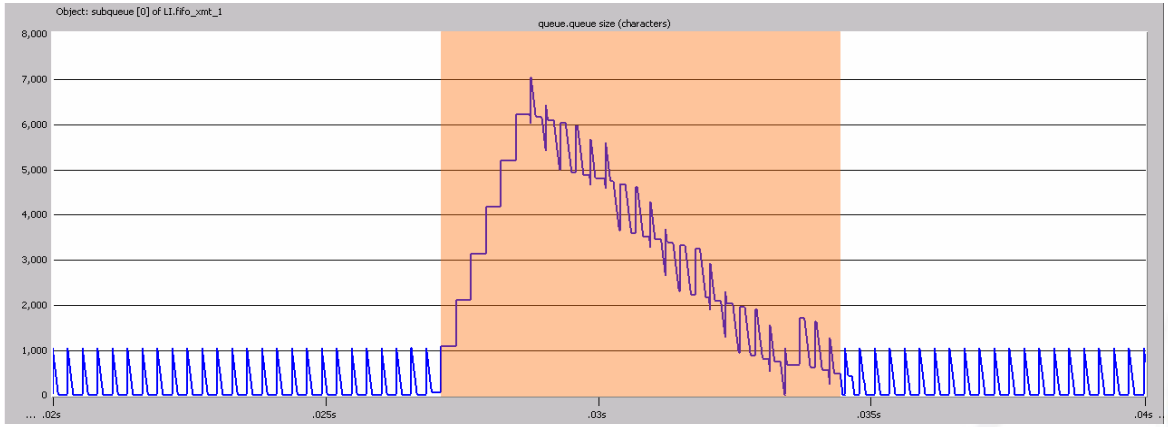
DCP Buffer occupation and variation

- The maximal DCP buffer occupation in worst-case is **8586** characters



LI Buffer occupation and variation

- The maximal LI buffer occupation in worst-case is **7033** characters



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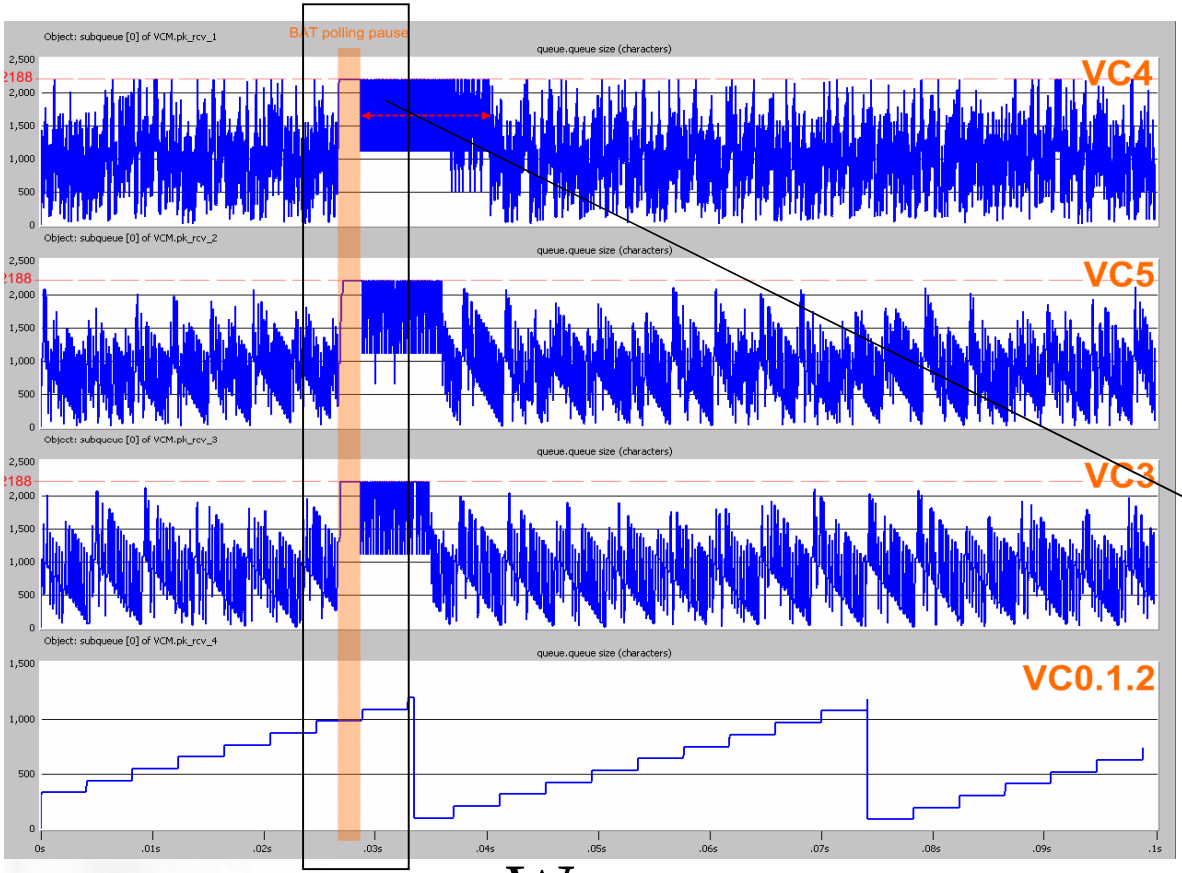
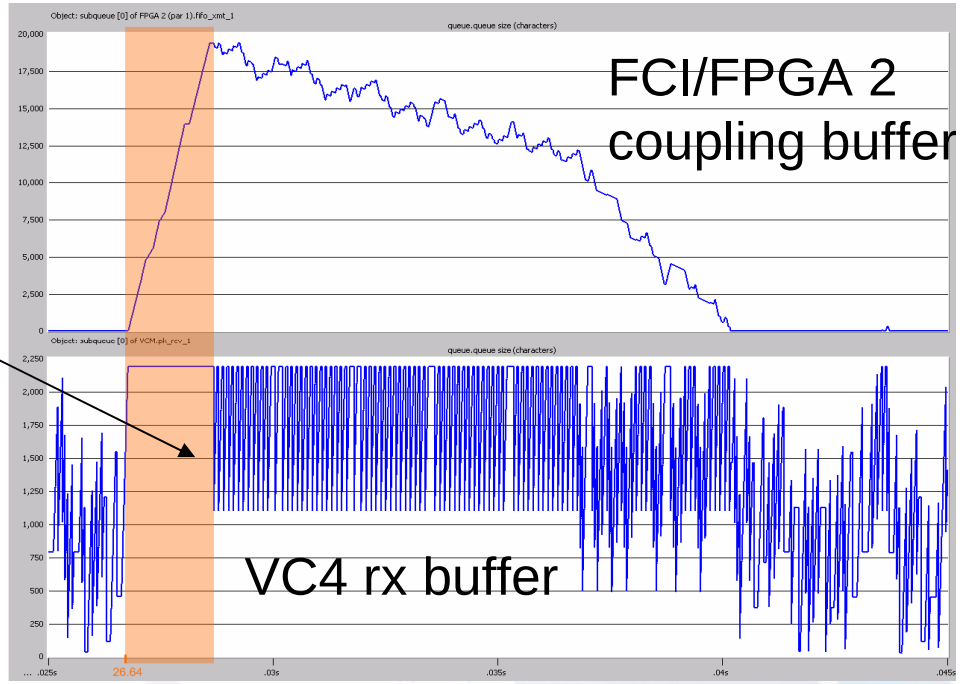
SMU Buffer occupation and variation

- The maximal SMU buffer occupation in worst-case is **4109** characters

OPEN

- VCM Buffer occupation and variation
  - During the 2ms VCM stall, saturation is reached for all VC except VC0,1,2.
  - Saturation of VC4 from 27ms to recovery at ~40ms creates an increase of FPGA2 buffer occupation as visible on the second graph





Worst-case zoom

OPEN

Links usage & occupation

- The higher link usage is 70.58% inside the FCI (character transfer time versus link capability), whereas maximal link/port occupation is 77.94%.

	Link usage	**Link occupation** *(incl. congestion delays)*		
	T_{char} / $T_{simulation}$	Average usage (Mean + T_{FCTi2})	Accuracy (+/- T_{FCTi2})	**Upper bound** (**Mean + T_{FCTi}**)
R3 -> R4 *(1)*	61.16 %	71.34 %	0.18 %	71.53 %
R4 -> R3 *(2)*	10.37 %	22.04 %	1.52 %	23.56 %
R4 -> R2 *(3)*	61.14 %	75.09 %	0.18 %	75.28 %
R2 -> R4 *(4)*	10.37 %	22.04 %	1.52 %	23.56 %
R1 -> R2	7.33 %	20.52 %	0 %	20.52 %
R2 -> R1	0.37 %	0.37 %	-	0.37 %
FPGA2 -> R4 *(5)*	63.81 %	76.42 %	1.52 %	77.94 %
R4 -> FPGA 2 *(6)*	63.81 %	72.66 %	1.52 %	74.18 %
VAE -> R3 *(7)*	70.58 %	70.6 %	0 %	70.6 %
R3 -> VAE	3.53 %	3.53 %	-	3.53 %
ICU -> R3	0.096 %	0.8 %	0 %	0.8 %
R3 -> ICU	0.005 %	0.005%	-	0.005 %
SCAE -> R3	1.7 %	2.17 %	0.51 %	2.69 %
R3 -> SCAE	20.55 %	20.53 %	0.02 %	20.55 %
FPGA1 -> R3 *(8)*	63.5 %	72.44 %	1.51 %	73.95 %
R3 -> FPGA1 *(9)*	63.5 %	72.07 %	1.51 %	73.58 %
DCP -> R2	45.93 %	50.72 %	0 %	50.72 %
R2 -> DCP	2.3 %	2.3 %	-	2.3 %
LI -> R1	37.51 %	42.33 %	0 %	42.33 %
R1 -> LI	1.88 %	1.88 %	-	1.88 %
SMU -> R1	21.09 %	21.1 %	0 %	21.1 %
R1 -> SMU	1.06%	1.06 %	-	1.06 %

Study Case 3 Synthesis

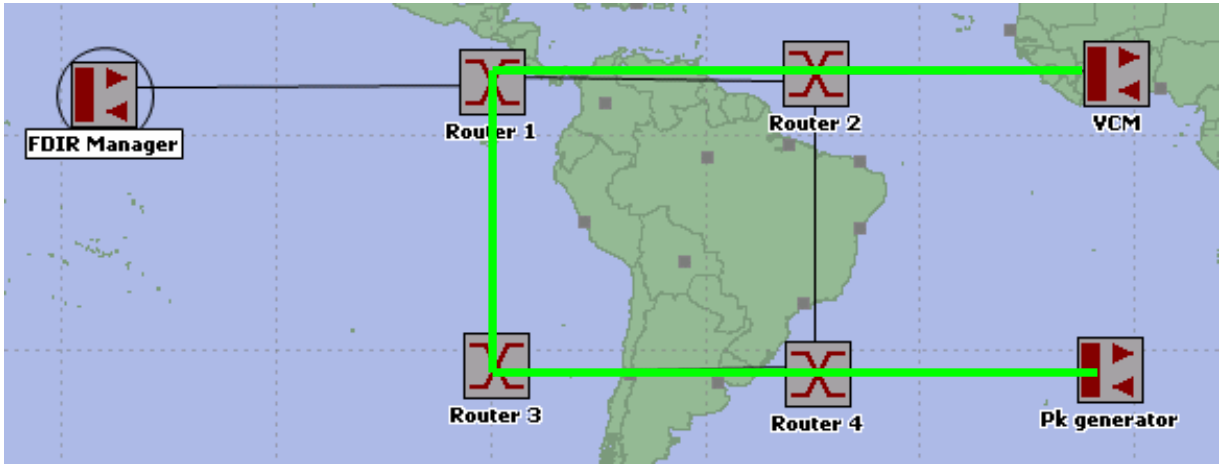
- A network failure of 2ms requires 13.8ms to recover (nominal buffer occupations & ETE delays)
- Gap between link usage and link occupation can reach up to 14% in this simulation. Link occupation is more representative as it includes congestion delays and provides the real port/link availability.
- A network failure (VCM stall) of 2ms generates a port occupation increase up to 5% versus “study case 2”
- The 2 ms VCM stall has a major impact on packets whose transfer is interrupted (more than +2 ms on ETE delays). However ETE delays remain under 3.1ms for worst-case phase except for INR packets which reach 41.3ms

Conclusion

- Demonstration based on representative study cases showed that the simulator can be used for current mission to support SpW network traffic analysis, predictions and validation
- MOST offers SpW experts the possibility to test new designs
- MOST concept provides a progressive tool, built with independent SpW building blocks which can be exchanged to test new SpaceWire technology or even SpW standard evolutions, without waiting for HW development

Under development

- New capabilities: FDIR (failure detection, isolation & recovery)



- 3. Reconfiguration:

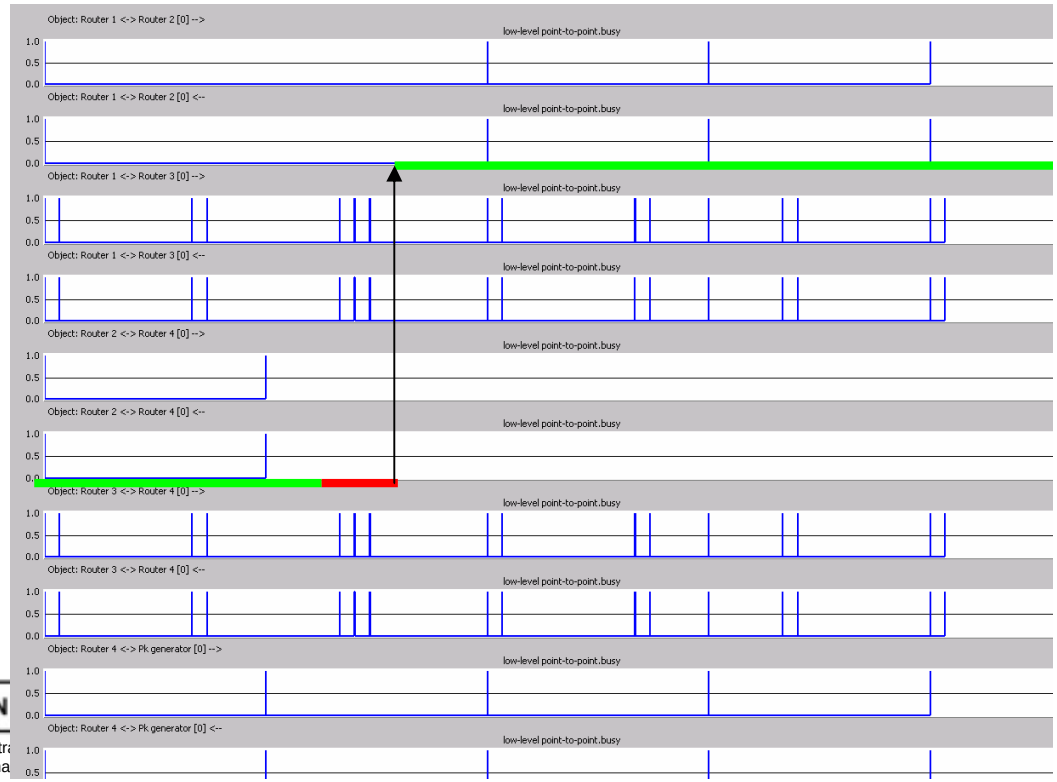
  Pk generator à R4

  R4 à R3

  R3 à R1

  R2 à VCM

- MOST implements a new FDIR manager able to monitor And reconfigure networks using RMAP messages



Thanks for your attention !