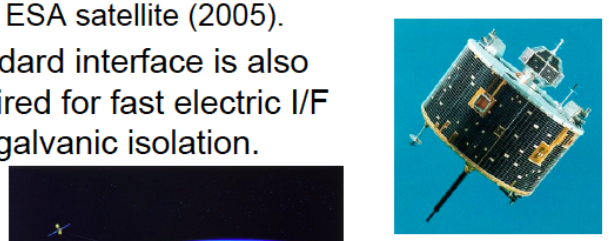
SpaceFiber
- activities in Japan -

- SpaceFiber
  - High speed
  - Optical / Electrical
  - Reliability / Nomblocking
- NEC's activity
- MELCO's activity
- Other activities

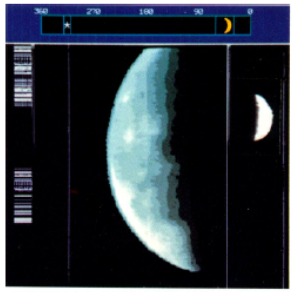
1. Our GOAL in SpaceFibre activities

- Standard interface specification is required for high speed data transmission using optical fibre and devices.
  - HITEN saw the reverse side of the moon using optical fibre transmission system (1993).
  - OICETS succeeded in laser communication with ESA satellite (2005).
- Standard interface is also required for fast electric I/F and galvanic isolation.

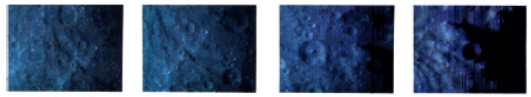


HITEN (1993)

OICETS (2005)



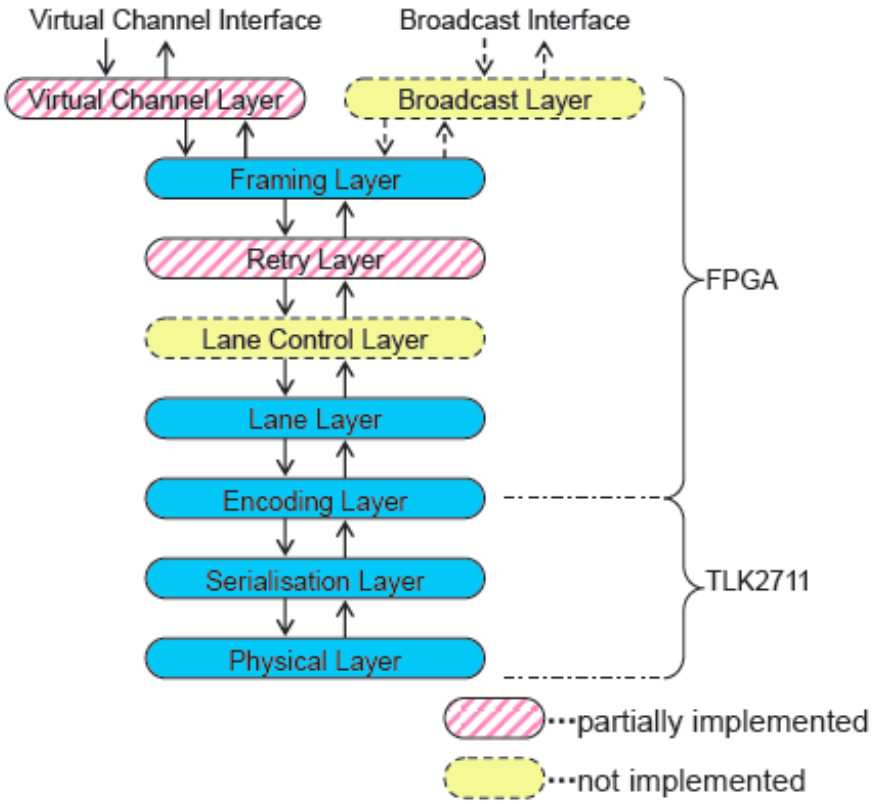
ONSの捉えた月（中央）と地球（右）

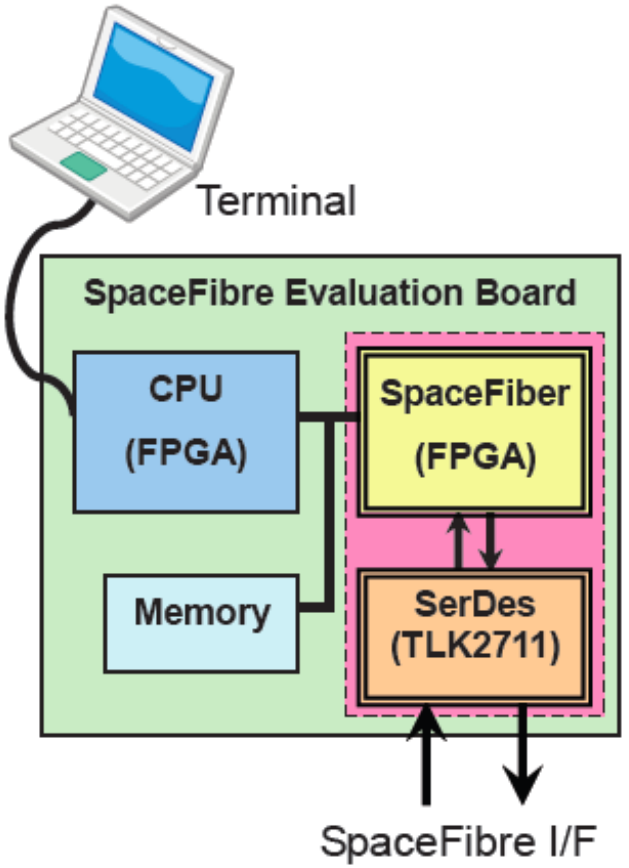


月面落下直前、クレーターが次第に大きく迫り、やがて日陰部に入る（1993年4月11日）

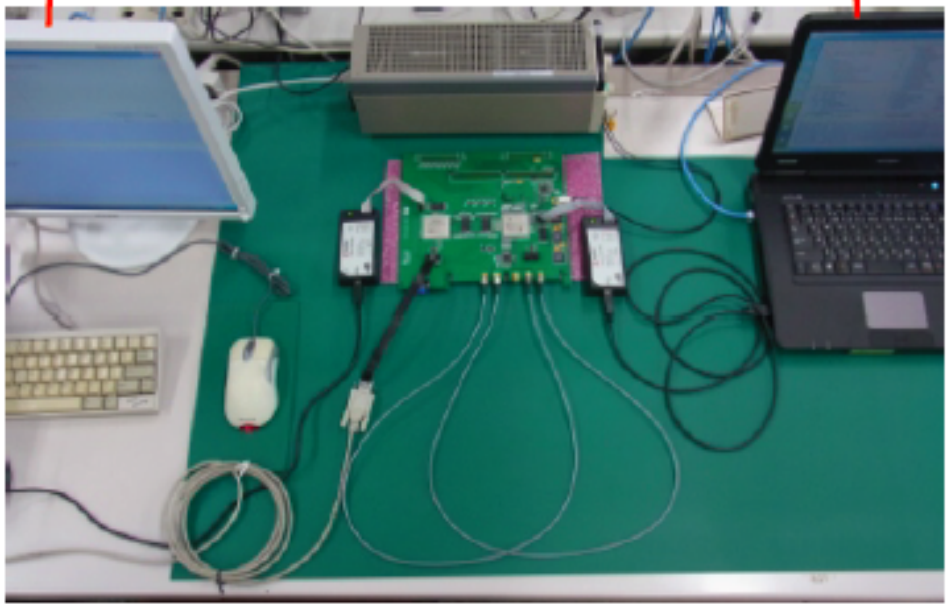
Melco's work (1/3)

- Melco is implimenting SpaceFibre CODEC on FPGA with TLK2711.
- At the beginning, Melco implemented minimum functions.
- Melco is planning interoperability tests with a company in Japan and with Uod.

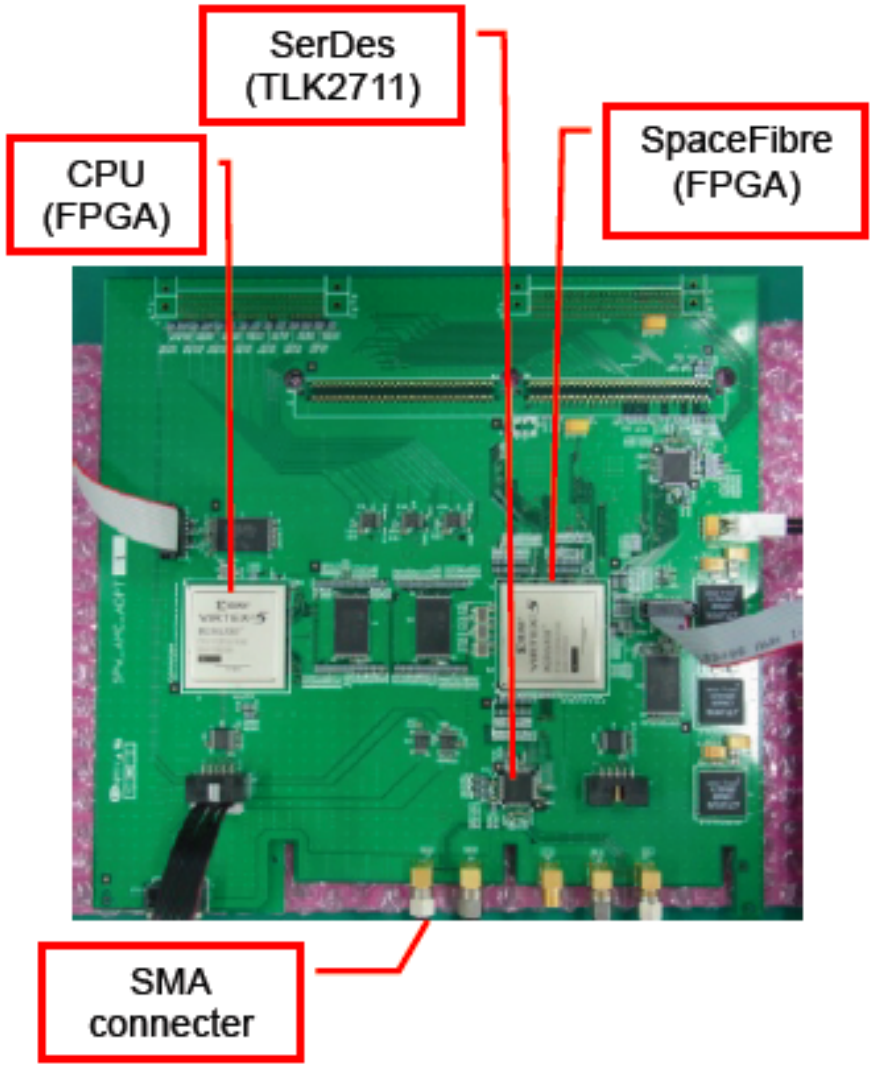




Melco's work (2/3)



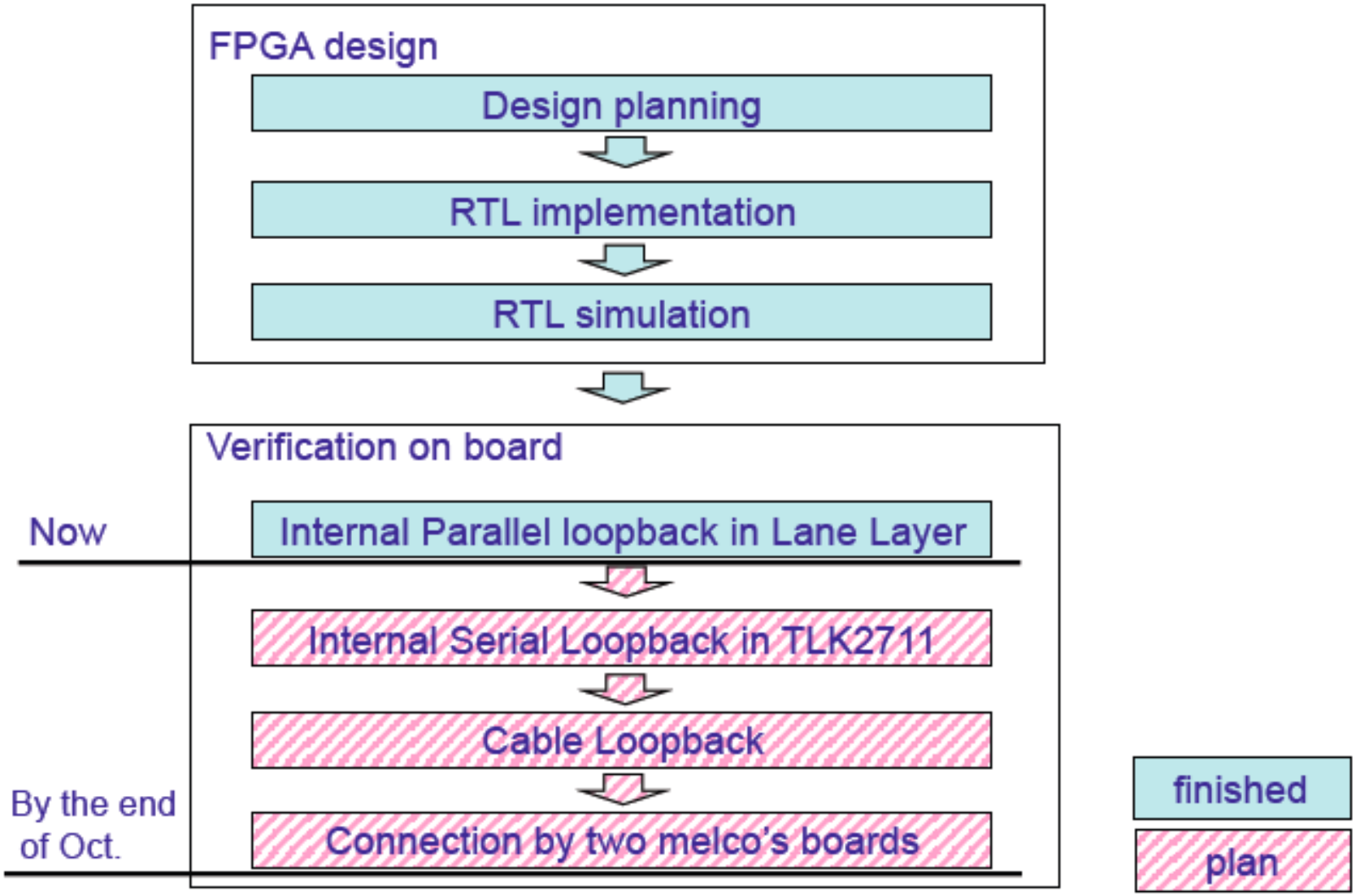
Experimental installation



SpaceFibre Evaluation Board

Melco's work (3/3)

Status of development



TK1-12-151

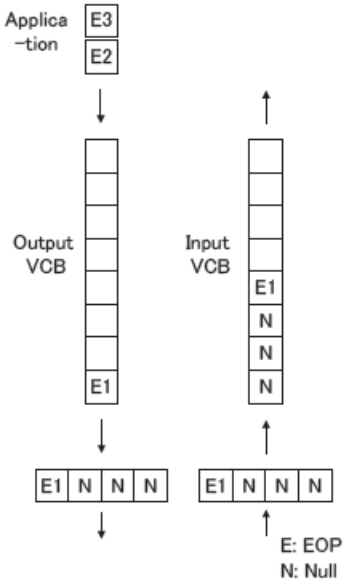
Comments for SpaceFiber Specifications

2012 Oct.

MITSUBISHI ELECTRIC CORPORATION

Comments for SpaceFibre Draft D (1/7)

- SpaceWire Null
  - If VCB's width is 8bit and EOPs are putted one by one on output VCB, input data rate is increased up to 4 times of the output rate. Isn't it problem? However, this case is caused in low speed, so it may be not problem.



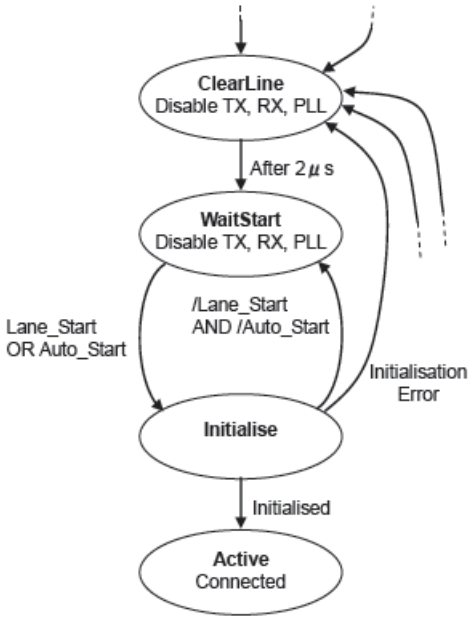
- 5.3.2.2 SpaceWire Null
  - c. When the data available from the output virtual channel buffer to be put in the data frame is not a multiple of four N-Chars, Null symbols shall be added to the end of the data field to pad the last word out to a complete data word.
  - d. Nulls shall be transported across the SpaceFibre link and placed in the input virtual channel buffer at the receiving end of the link.

"Null" is changed to "Fill" in draft E.
"Fill" should be removed at the destination.
To avoid waste of bandwidth.

MITSUBISHI ELECTRIC
Changes for the Better

Comments for SpaceFibre Draft D (2/7)

- Lane Initialisation State Machine
  - States' Mismatch ?
    - In Initialise super-state, receiving and sending control words are needed to change state.
    - On the other hand,
      - In WaitStart State, disable TX, RX, PLL,
      - In Active State, enable TX, RX, PLL.
  - Lack of description
    - "Lane_Start" and "Auto_Start" have to be defined.



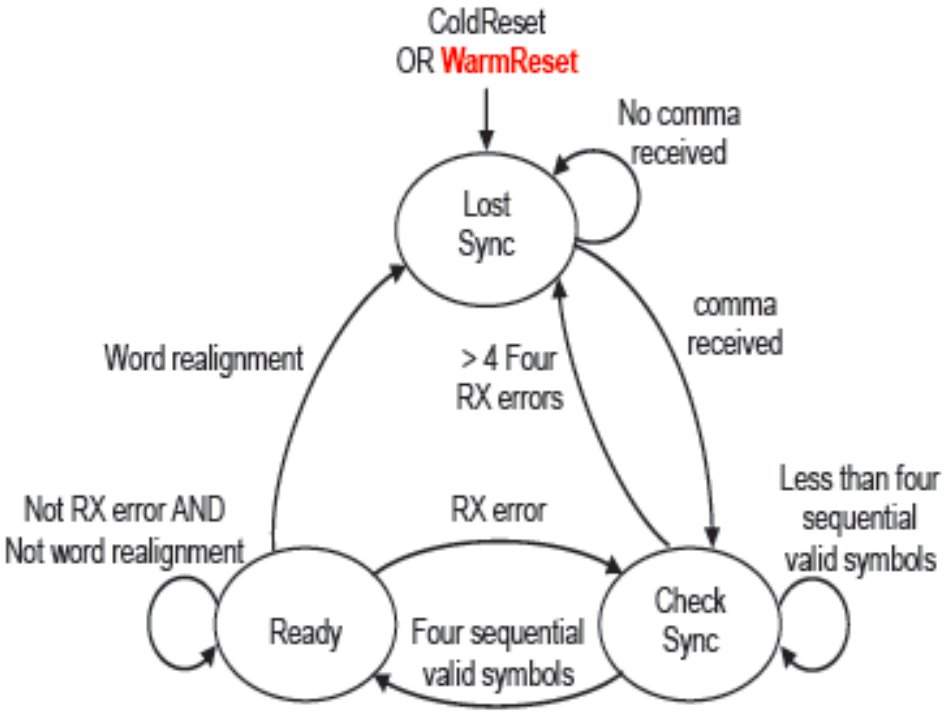
Enabling sequence should be defined.
Improved in Draft E

Comments for SpaceFibre Draft D (3/7)

- Data rate adjustment
  - Description's Mismatch
    - 4.3.7.2: To do this the transmitter sends SKIP control words periodically, at least every 5000 control words or 32-bit data words.
    - 5.9.3: A skip control word shall be sent every 5,000 words.

Comments for SpaceFibre Draft D (4/7)

- Receive Synchronisation State Machine
  - Description's Mismatch
    - Fig5-11: WarmReset is asserted, move to LostSync state.
    - 5.10.3.2.2 c.2: When WarmReset is asserted, move to the CheckSync state.



MITSUBISHI ELECTRIC
Changes for the Better

Comments for SpaceFibre Draft D (5/7)

for a greener tomorrow

- Receive Synchronisation State Machine
  - It is supposed that the state machine is based on 8bit-input implementation.
  - Therefore, in the 16bit-input implementation, in order to achieve the transition to the same state for the same input sequence, it is necessary to double the 16bit-input clock rate.
  - As well, in the 32bit-input implementation, the state machine's clock rate have to be four times of 32bit-input clock rate.
  - It can be avoid by the state machine based on the 32bit-input implementation.
  - In addition to that, flexibility of the number of symbols is needed (e.g. State changes by 4-7 sequential symbols.)
  - By the flexibility, the state can change in the 32bit boundary, regardless of the position of the comma code.

Input sequence : C | V | V | V | V | Er

Clock cycle	8bit-input implementation: 8bit input (0 7)	8bit-input implementation: State	16bit-input implementation: 16bit input (0 7)	16bit-input implementation: State
1	C	→ Check Sync	C | V	→ Check Sync
2	V		V | V	
3	V		V | Er	→ Ready? → Check Sync?
4	V			
5	V	→ Ready		
6	Er	→ Check Sync		

C: Comma
V: Valid symbol
Er: RX Error

Flexible state machine based on 32bit-input

C | V1 | V2 | V3	→ Check Sync	- | - | - | C	→ Check Sync
V4 | V5 | V6 | V7	→ Ready	V1 | V2 | V3 | V4	→ Ready

Behavior of the sequencer is not the same for 8/16/32 bit implementations.
It seems to be taken into account in Draft-E.

Comments for SpaceFibre Draft D (6/7)

- Word Synchronisation
  - Setting the previous word to K0.0 is necessary?
    - Draft says that if a word contains a K0.0 symbol, all the symbols in the word and the previous word will be set to K0.0. (5.10.4 i. NOTE)
    - To achieve this function, a buffer for a previous word is needed (It is complexity).
    - If 4 RXERRs are enough for higher layer, the buffer can be omit.
    - Otherwise, it is easy that the next word instead of the previous word is set to K0.0.

Comments for SpaceFibre Draft D (7/7)

- If there is a list of Mandatory functions and Optional ones, it's useful.
- The state transition diagrams of The Lane Initialisation State Machine are not accurate. Accurate state transition diagrams or state transition tables are needed.

Melco's other comments are on following table.

Other coments fro MELCO

- Miscs. 5 comments
- Virtual channel layer 4 comments
- Framing layer 2 comments
- Lane layer 15 comments
- Encoding layer 4 comments

Miscs.

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
1	–	–		Y	If there is a list of Mandatory functions and Optional ones, it's useful.	1				
2	14	3.2 Terms specific to the present standard			There are similar two words. 3.2..5 bandwidth used 3.2..38 used bandwidth "bandwidth used" is used only 5.4.4.2 Bandwidth credit's f. Isn't it typo of "used bandwidth"?					1
3	52	4.4.18 Reset			Cold reset's explanation is in "5.9.2.1.2 ColdReset State" a.2. For this explanation, "4.4.18 Reset" is better section.					1
4	57	5.2.3 Link management service			What is connected by this interface?		1			
5	78	5.3.3.3 Broadcast frame			Typo: Fig5-4 line2 left DATA 1 MS -> DATA 1 LS				1	
						1	1	0	1	2

Virtual channel layer

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
1	75	5.3.2.2 SpaceWire Null		Y	If VCB's width is 8bit and EOPs are putted one by one on output VCB, input data rate is increased up to 4 times of the output rate. Isn't it problem? However, this case is caused in low speed, so it may be not problem.					1
2	87	5.4.4.2 Bandwidth credit			It's better to describe the dimensions and units of each variable. I supposed following. ExpectedBandwidth: no-dimension (rate) LastFrameBandwidth:byte BandwidthAllowance:byte BandwidthCredit:byte BandwidthCreditLimit:byte LinkBandwidth:byte (per 1 sec.)	1				
3	87	5.4.4.2 Bandwidth credit	d		Typo?: two times "except for". "d. NOTE This is zero except for all virtual channels except for the one that sent the last frame."				1	
4	87	5.4.4.2 Bandwidth credit	f		Typo? :f Bandwidth Used -> Used Bandwidth				1	
						1	0	0	2	1

Framing layer

No.	section page	section	alphabet	see PPT	comments
1	96	5.6.2 Framing			There is no explanation for "FRAME FCT" of Fig.4-2.
2	96	5.6.2 Framing			There is no explanation for "EXTRACT FCT" of Fig.4-2.

Suggestion	Insufficient	Lack	Typo	Others
		1		
		1		
0	0	2	0	0

Lane layer (1/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
1	119	5.9.1.1 TX_WORD.request			When the following control words are sent, are TX-words discarded? IDLE, INIT, IACK, RCLR, RACK, STANDBY, LOS		1			
2	120	5.9.2 Lane initialisation and standby management		Y	The state transition diagrams of The Lane Initialisation State Machine are not accurate. Accurate state transition diagrams or state transition tables are needed.		1			
3	120	5.9.2 Lane initialisation and standby management			mistake of Section number. * after 5.9.2, 5.9.2.1.2 come. * after 5.9.2.1.13, 5.9.2.1.1 come.				1	
4	123	5.9.2.1.2 ColdReset State	b		b.1: What has to be done for "Reset of the SpaceFibre Lane" ?		1			
5	123	5.9.2.1.2 ColdReset State		Y	In Initialise super-state, receiving and sending control words are needed to change state. On the other hand, * In WaitStart State, disable TX, RX, PLL, * In Active State, enable TX, RX, PLL. Are they states' mismatch ?		1			

Lane layer (2/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
6	124	5.9.2.1.3 ClearLine state	b		b.4: TLK2711 can't do "receiver bit inversion". It should be optional.					1
7	127	5.9.2.1.4 WaitStart State	c	Y	c.3, c.4: "Lane_Start" and "Auto_Start" have to be defined.			1		
8	128	5.9.2.1.6 Active State			The following sentences are same meanings? d.5:"When No Signal At Receiver signal is asserted" 5.9.2.1.12 StartPolarity state c.3:"When No Signal is detected at the receiver inputs"					1
9	128	5.9.2.1.6 Active State			How does lane layer get an error occurs in an upper layer?			1		
10	135	5.9.2.1.12 StartPolarity state	b		There is no description of "send IDLE". In Fig5-9, "send IDLE" exists.					1

Lane layer (3/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
11	137	5.9.2.1.1 NearEndStarted state			INIT_1 and INIT_2 in Fig.4-2 may be old spec's signal.					1
12	142	5.9.2.1.5 StartRecovery state	b		"which are to be evaluated in the order given:" have to be described in "c." 5.9.2.1.6 NearEndRecovering state: ditto.				1	
13	142	5.9.2.1.5 StartRecovery state			Description's Mismatch. c.4: eight or more 5.9.2.1.6 NearEndRecovering state a.1: more than eight				1	
14	145	5.9.3 Data rate adjustment		Y	Description's Mismatch. 4.3.7.2: To do this the transmitter sends SKIP control words periodically, at least every 5000 control words or 32-bit data words. 5.9.3: A skip control word shall be sent every 5,000 words.				1	
15	-	-			In Lane Layer of Fig.4-2, there is IDLE input to RX-path before RECEIVE ELASTIC BUFFER, but is there the explanation of it?			1		
						0	4	3	4	4

Encoding layer (1/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
1	149	5.10.3.2 Receive Synchronisation State Machine		Y	Description's Mismatch. Fig5-11: WarmReset is asserted, move to LostSync state. 5.10.3.2.2 c.2: When WarmReset is asserted, move to the CheckSync state.				1	

Encoding layer (2/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
2	149	5.10.3.2 Receive Synchronisation State Machine		Y	Receive Synchronisation State Machine. It is supposed that the state machine is based on 8bit-input implementation. Therefore, in the 16bit-input implementation, in order to achieve the transition to the same state for the same input sequence, it is necessary to double the 16bit-input clock rate. As well, in the 32bit-input implementation, the state machine's clock rate have to be four times of 32bit-input clock rate. It can be avoid by the state machine based on the 32bit-input implementation. In addition to that, flexibility of the number of symbols is needed (e.g. State changes by 4-7 sequential symbols.)	1				

Encoding layer (3/3)

No.	section page	section	alphabet	see PPT	comments	Suggestion	Insufficient	Lack	Typo	Others
3	149	5.10.3.2 Receive Synchronisation State Machine			Hierarchy's Mismatch. In Fig.4-2, "SYMBOL SYNC" and "RECEIVE SYNC STATE MCH" are separated, but "5.10.3.2 Receive Synchronisation State Machine" is in "5.10.3 Symbol synchronisation".				1	
4	152	5.10.4 Word Synchronisation		Y	Setting the previous word to K0.0 is necessary? Draft says that if a word contains a K0.0 symbol, all the symbols in the word and the previous word will be set to K0.0. (5.10.4 i. NOTE) To achieve this function, a buffer for a previous word is needed (It is complexity). If 4 RXERRs are enough for higher layer, the buffer can be omit. Otherwise, it is easy that the next word instead of the previous word is set to K0.0.	1				
						2	0	0	2	0

Summary

- Implementation of Draft D
  - It is on the way in NEC and MELCO
  - Got several comments / suggestions
- Connectivity test
  - By December
  - Draft E (?)
  - Electrical