Development and Manufacturing of SpaceWire Router - GSTP-5 activity

Marko Isomäki

Aeroflex Gaisler AB
Kungsgatan 12, SE-411 19 Göteborg, Sweden

marko@gaisler.com

www.Aeroflex.com/Gaisler

Introduction

Aeroflex Gaisler has been awarded a contract within the ESA GSTP-5 for developing and manufacturing a SpaceWire Router ASIC

The purpose is to develop a router with a sufficient number of ports in a single component to satisfy the needs of the majority of missions in the near future

The other key properties is to have support for the new revision of the SpaceWire standard and SpaceWire-D

This activity will produce a prototype chip and an evaluation board.

The long term intention is to produce a qualified rad-hard product.

Development plan

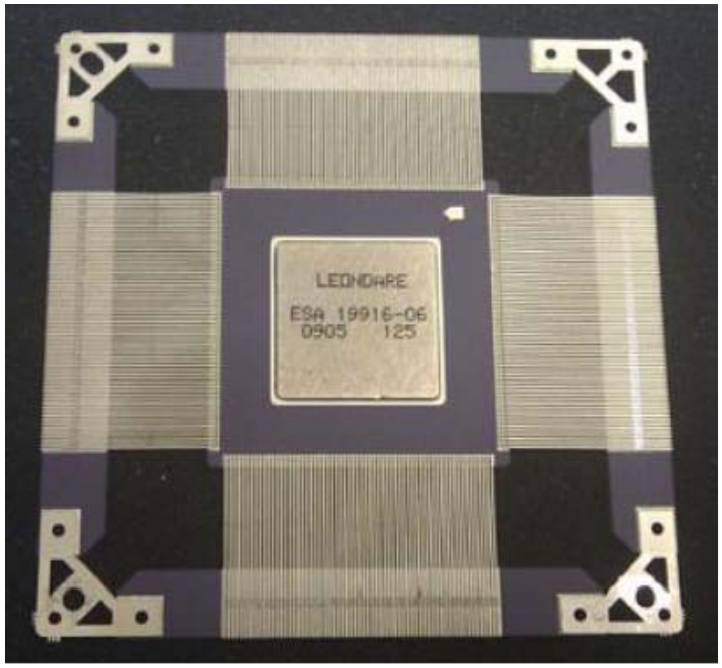
Kick-off:	February 2012
SRR:	March 2012
PDR:	June 2012
CDR:	October 2012
MPW:	October 2012
Die available:	January 2013
Packaged die:	February 2013
Tested part:	March 2013
Validated part:	April 2013

Companies involved

Main contractor:	Aeroflex Gaisler AB, Sweden
ASIC backend:	IMEC, Belgium
ASIC electrical testing:	Serma technologies, France
ASIC package:	Kyocera Fineceramics Ltd, UK
ASIC assembly:	HCM, France

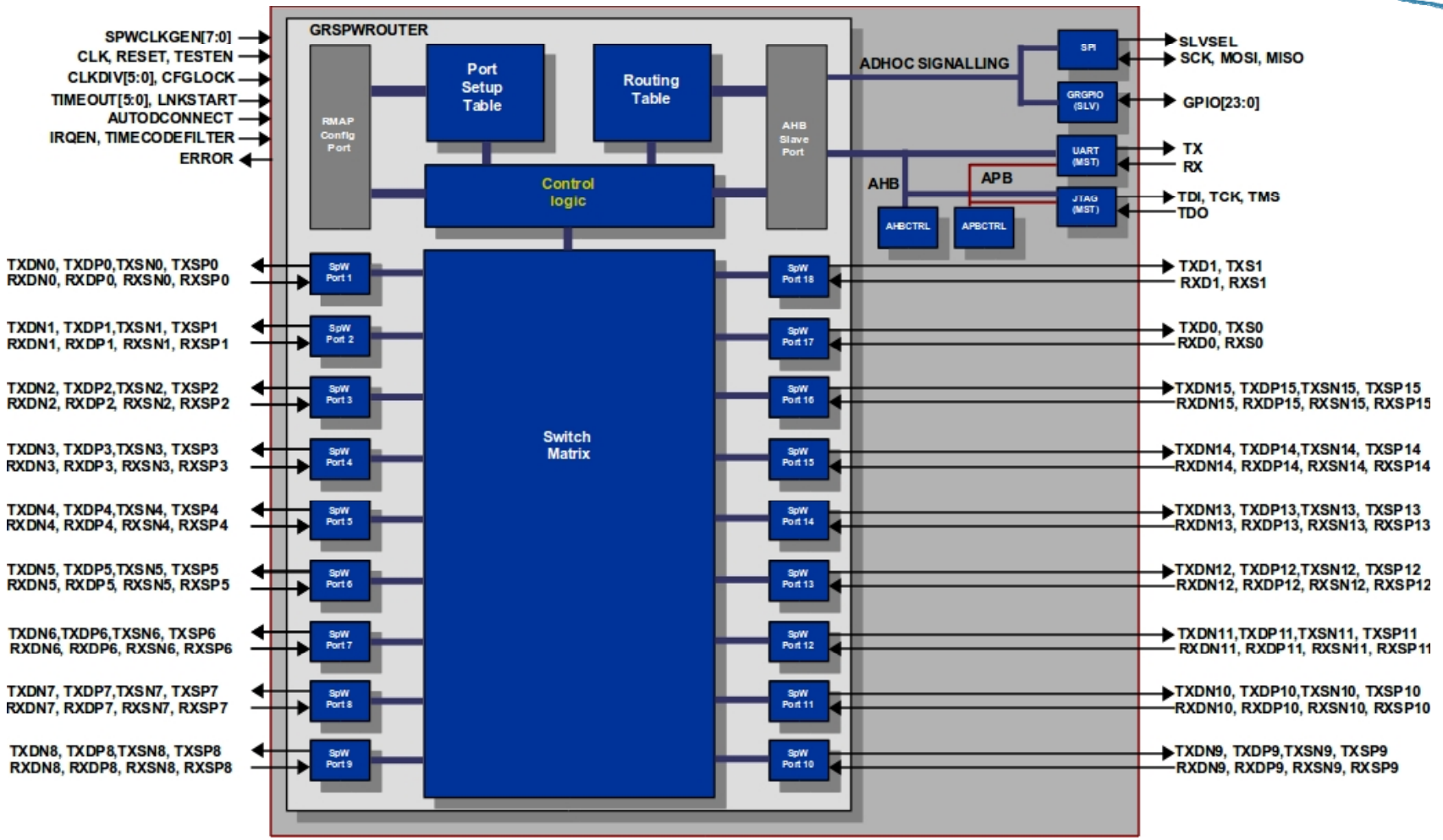
Technology and package

- DARE library on UMC 0.18 µm
- 256-pin CQFP
- Both are the same as for the LEONDARE project
- DARE library version is newer and several improvements have been made



AEROFLEX GAISLER

Architecture



Architecture (2)

- Based on existing SpaceWire router IP
  - Software drivers already available
  - Existing features will be software compatible in the new ASIC
- 16 SpW ports with on-chip LVDS
- 2 SpW ports with LVTTL signalling
- 64 character deep SpW FIFOs
- RMAP configuration port
- Timeouts
- Auto-scrubbing of routing table
- Packet and character counters for statistics
- Auxiliary time-code/interrupt-code interface on external signals

Architecture (3)

- Automatic clock gating of disabled ports for power saving
- External LVDS driver/repeater enable signals
- Interrupt signal for error indication to for example a processor
- An interrupt-code can optionally be generated when the interrupt signal is asserted
- SPI housekeeping interface accessible through the configuration port
- JTAG and UART auxiliary interfaces
  - Do not use RMAP
  - Simple read/write protocol with little overhead
  - Gives access to all status and configuration

New functionality in the SpW IP

- The Router ASIC shall be compliant to SpaceWire revision 2
- It shall also support SpaceWire-D
- SpaceWire revision 2
  - Support for interrupt distribution will be implemented
  - Several configurable options which control the interoperability with old devices and time-codes
  - FSM will be updated according to the minor changes accepted by the working group
- SpaceWire-D
  - Maximum packet length configurable per port and spill done if violated
  - Spilling if transfer active at time-tick

Prototype

- ASIC prototypes will preliminarily be ready in April 2013
- An accompanying prototype board will also be available supporting all features of the ASIC
- It will most probably be based on the existing RASTA-SPW-ROUTER CPCI FPGA board available from Aeroflex Gaisler