European LVDS driver development and ECSS evaluation and qualification

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18th SpW working group – SpW component development

ESTEC
25/04/2012

ECI phase 3 activities started 2012

Contracts

Awarded to

1. Aeroflex Gaisler AB
2. Arquimea Ingenieria S.L

Schedule

1. Phase 1 preliminary design: 6months
2. Phase 2 detailed design and test: 12 months
3. Phase 3 ESCC evaluation and qualification: 6-8 months

Objectives

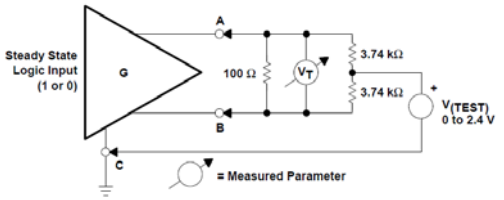
1. Provide ITAR free ESCC qualified radhard TIA/EIA 644a compliant LVDS components for the European market.
2. Ensure long term availability and a sustainable device support framework.
3. Make available LVDS parts suitable for most common applications such as SpaceWire, signal repeating or distribution.
4. Enhance common mode voltage range and ESD tolerance for the LVDS buffers.

Limitations of LVDS and suggested improvements

LVDS standards

Comparison of the most commonly used LVDS standards in terrestrial applications

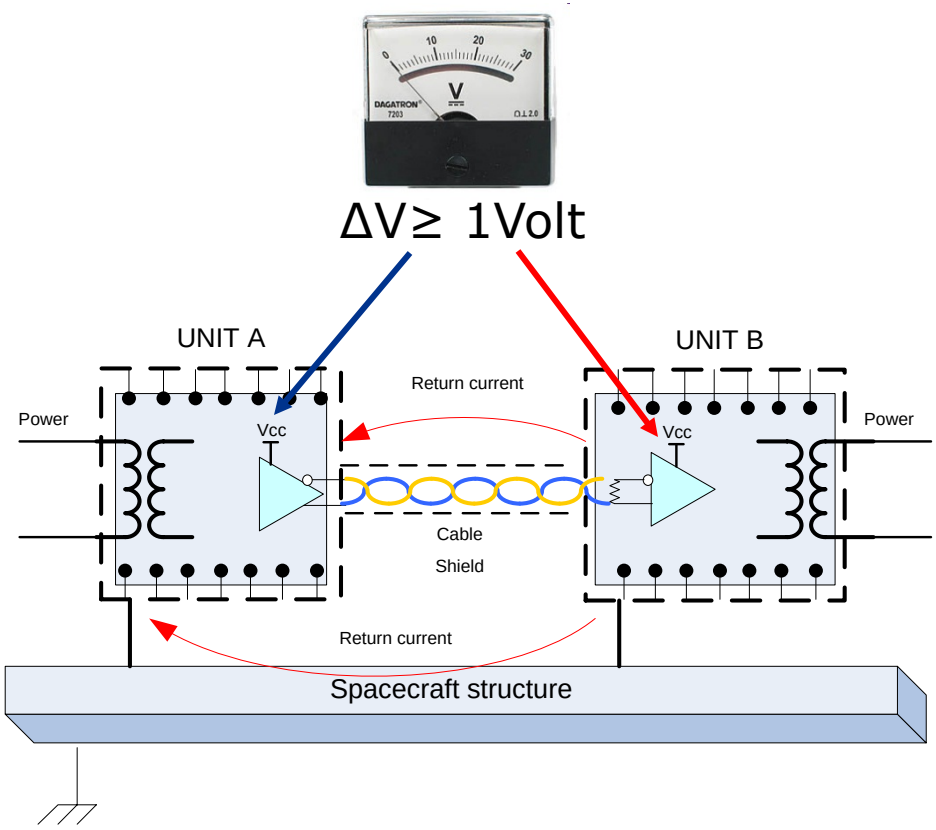
PARAMETER	TIA/EIA-644 (LVDS)	TIA/EIA-644-A (LVDS REV A)	TIA/EIA-899 (M-LVDS)	UNIT
DRIVER CHARACTERISTICS				
Offset voltage: Vos (max)	1375	1375	2100	mV
Offset voltage: Vos (min)	1125	1125	300	mV
Differential output voltage: Vod (max)	454 (100 Ω)	454 (100 Ω)	650 (50 Ω)	mV
Differential output voltage: Vod(min)	247 (100 Ω)	247 (100 Ω)	480 (50 Ω)	mV
Offset voltage variation: Vospp	150	150	150	mV
Short circuit current: Ios	12/24	12/24	43	mA
Differential voltage change: ΔVod	50	50	50	mV
Offset voltage change: ΔVos	50	50	50	mV
Transition time: tr/tf(min)	260	260	1000	ps
RECEIVER CHARACTERISTICS				
Ground potential difference: Vgpd	+/- 1	+/- 1	+/- 1	V
Input leakage current: Iin	20	20	20	µA
Differential input leakage current: Iid	NS	6	4	µA
Input voltage range: Vin	0 to 2.4	0 to 2.4	–1.4 to 3.8	V
Input threshold: Vith	100	100	50	mV
NS: Not specified				



TIA/EIA 644A Full load test circuit

Common Mode Noise and TIA/EIA 644A

Common Mode Noise i.e. voltage differences above 1V is a problem for most TIA/EIA 644 LVDS devices



Common mode noise is caused by:

- **"Conducted" noise:**

Significant impedance of return currents generates voltage difference.

- **Capacitive or inductive coupling:**

Signal lines too close to e.g power cables, switching of inductive loads,

- **EMI:**

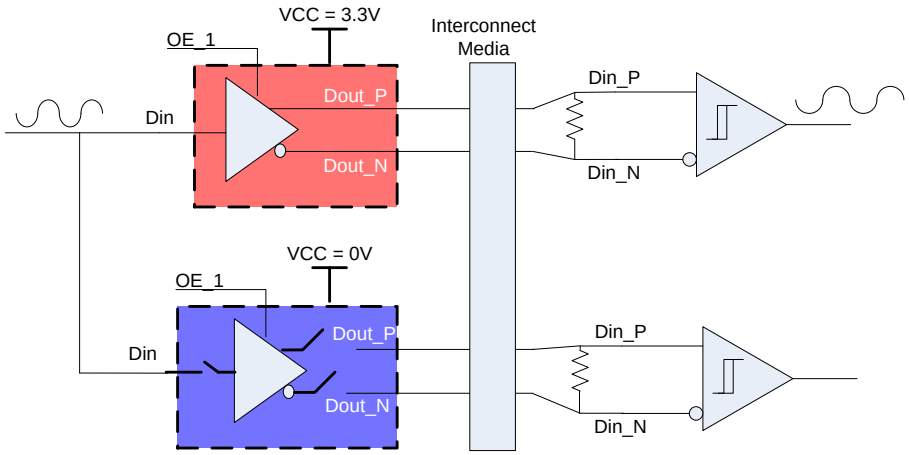
Coupling from adjacent signal lines

- **ESD due to spacecraft charging:**

Sudden release of energy caused by surface charging.

Cold Sparing and higher absolute max rating

Cold Sparing capability is useful in applications e.g. where LVDS buffers are connected together for redundancy purposes



Cold Sparing Buffer represents high impedance when not powered

Increased absolute max rating of a LVDS device to reduce risk of fault propagation

Typical max VCC rating for a **3.3V** device is typically around ~**4.0V**

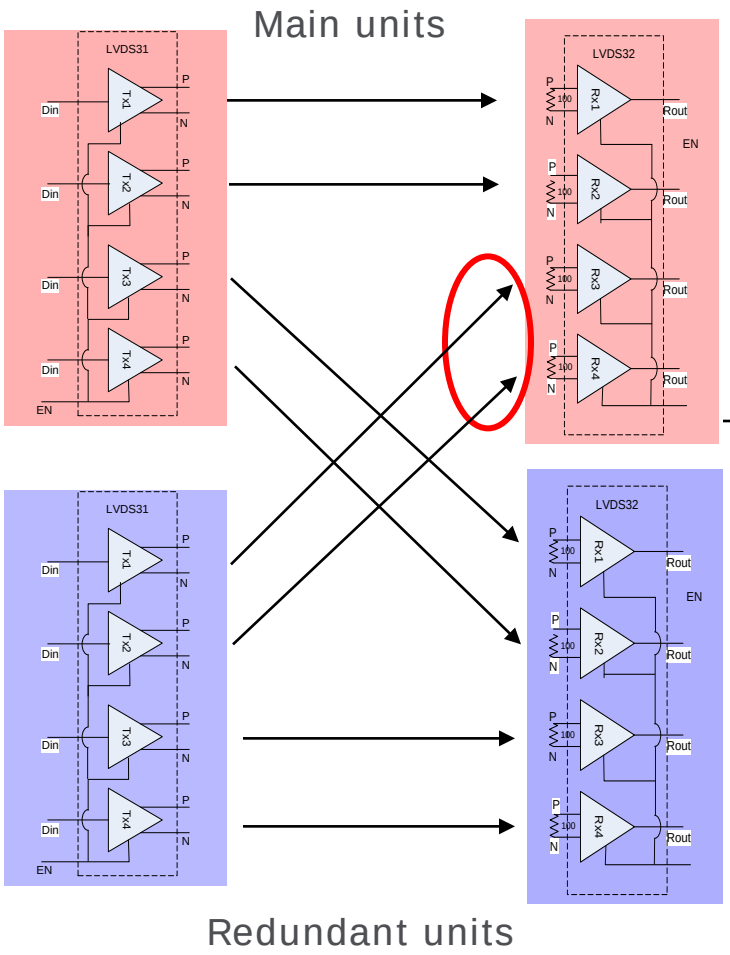
Target for the European LVDS drivers

Cold sparing capability

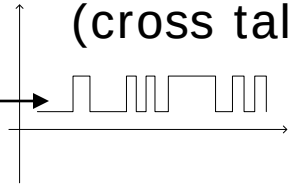
Absolute max rating VCC: -0.5 to 4.6V

High ESD tolerance: 8kV -15kV (HBM)

Failsafe operation of the LVDS receiver
- Creative engineering may cause problems



In this **non-recommended** cross strap (N&R links not via same device), the un-driven receiver inputs may pick up noise causing spurious transitions on output (cross talk)



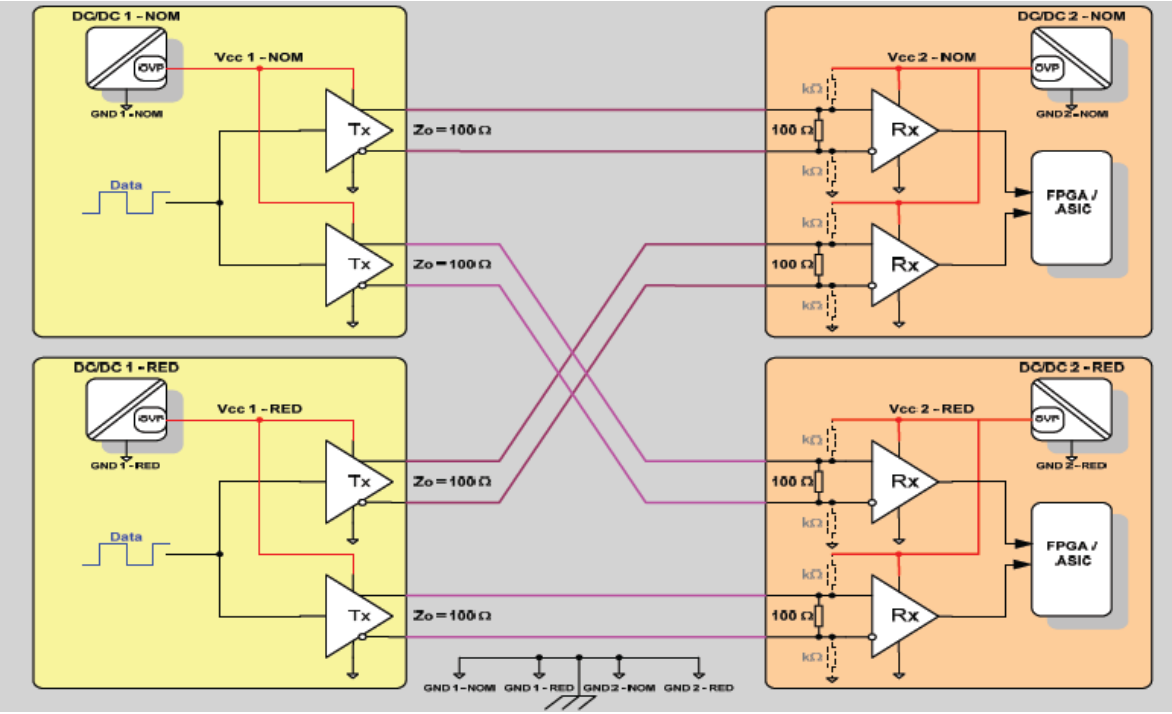
External failsafe network or failsafe circuit should always be used to avoid spurious switching

Target for the European LVDS drivers

Include internal failsafe circuit

Implementation issues

Fault voltage propagation is always an issue even in correct x strapping as in the figure below



** Figure from SpW link I/F, LVDS Power & x-strapping aspects S.Landström & W.Gasti, 2008

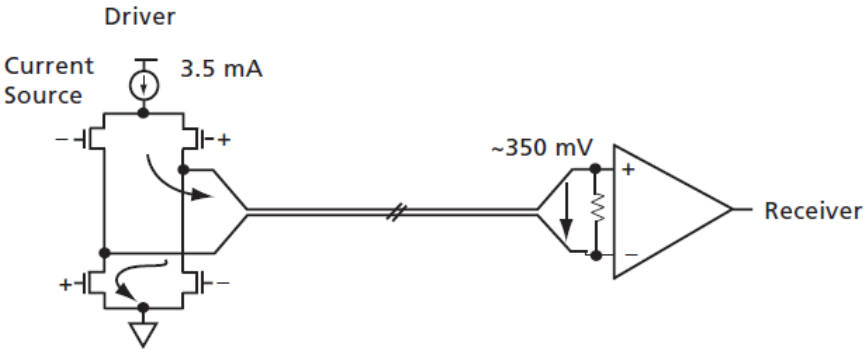
Power supply failure can in the **worst case** lead to voltages much higher than standard CMOS absolute max ratings.

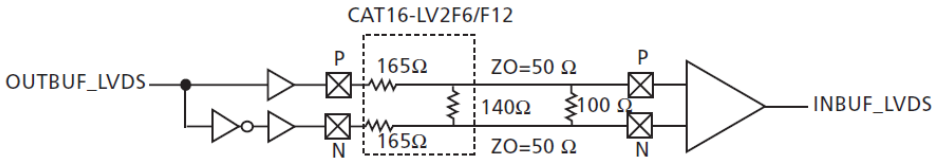
*** Note OVP must always be used.**

More robust LVDS devices can mitigate effect of over voltage propagation.

LVDS driver structures
Voltage and current mode drivers

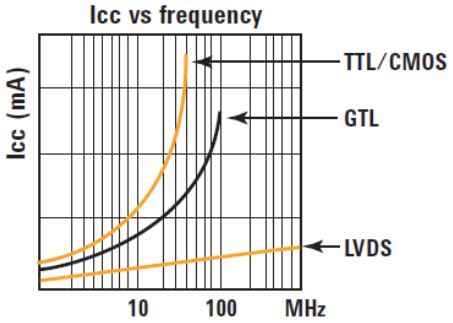
Some basic models





Current source based driver

- ✓ Most common implementation
- ✓ Achieves fastest performance
- ✓ Robust towards noise
- ✓ Power consumption is low (~10mW per output)



Voltage source based driver

- ✓ Sometimes called emulated LVDS transmitter
- ✓ Can fulfil the ANSI EIA/TIA-644a standard, by setting the correct source resistor network.
- ✓ Find these most often used in FPGAs without current mode LVDS drivers
- 😐 Lower performance than current source driver, but is ok for most applications up to 200Mbps
- 😐 More noisy and more power consuming than current source drivers and receivers.

LVDS driver structures

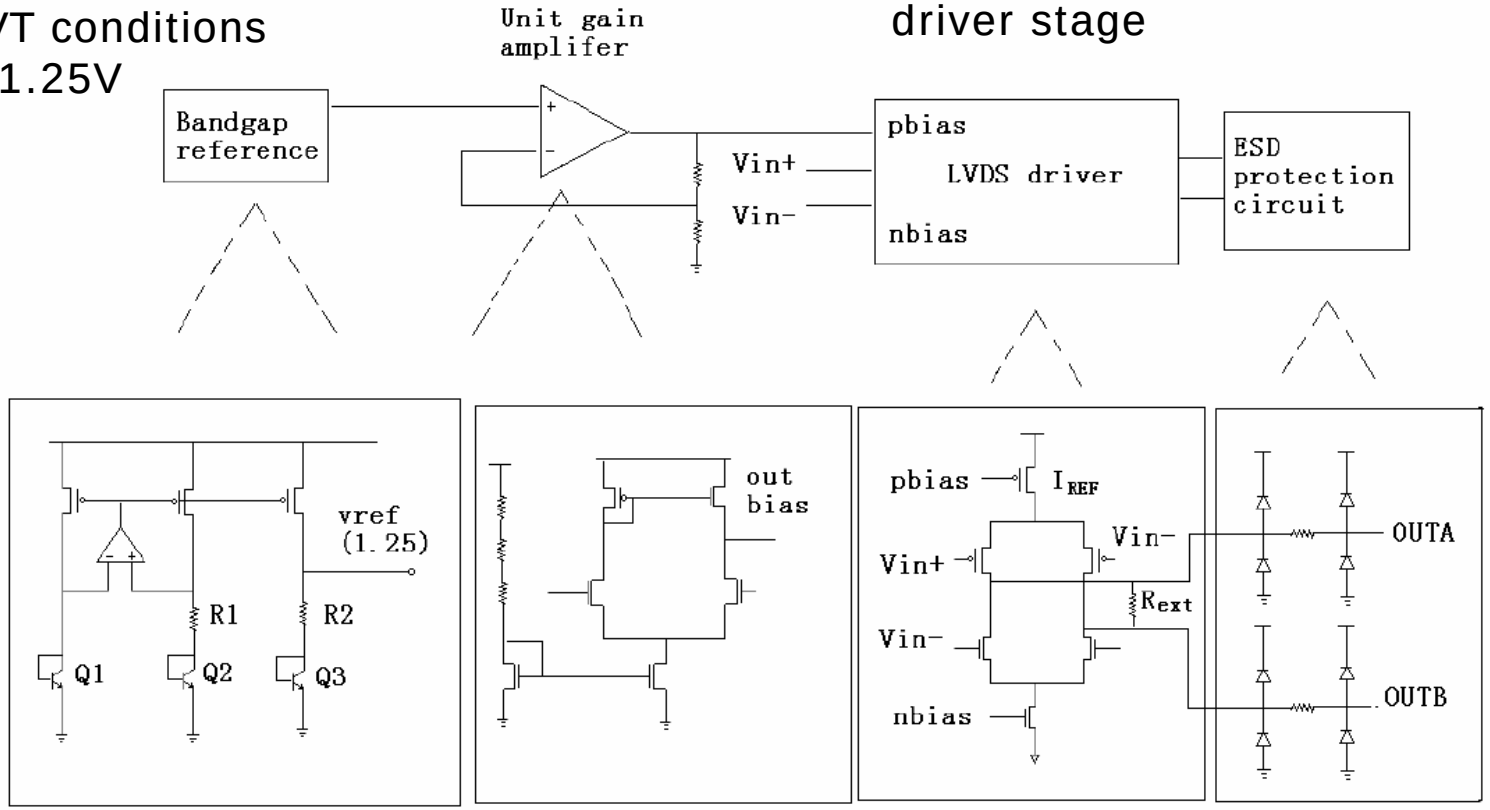
More advanced current mode models

Ensure constant bias voltage for all PVT conditions
* 1.25V

Constant common mode voltage stage

Differential driver stage

ESD structure



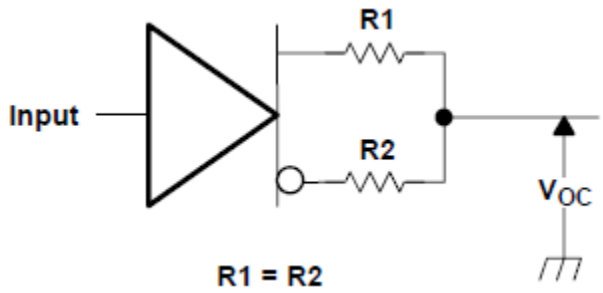
Important considerations for the LVDS driver

Symmetry of the complementary LVDS outputs

a. Imbalanced symmetry leads to noise emissions

b. Common mode components induced during switching imbalance are high in frequency and radiate readily

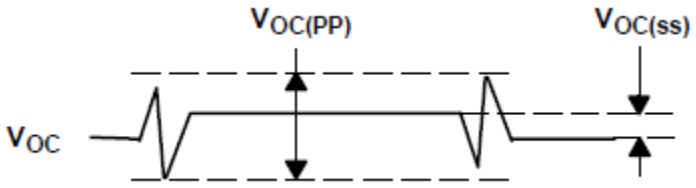
c. TIA/EIA-644a require Voc(PP)<150mV



Noise frequency Fundamentals

Voc(PP) >= 3/TUI Hz

Voc(ss) = 0.5/TUI Hz



What can we improve?

- Requirements for the LVDS devices

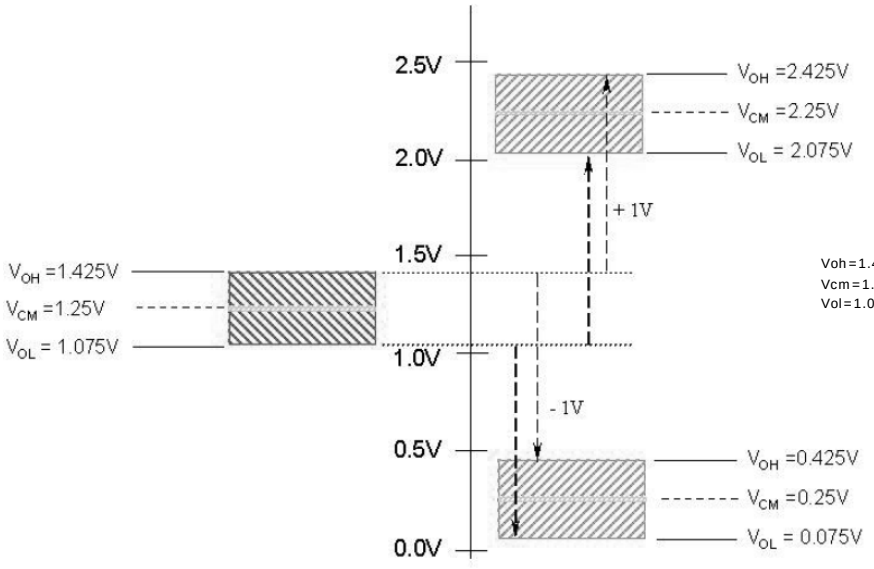
1. **Increased common mode tolerance on LVDS receiver**
    a. Requirement: -5V to +6V
    b. Some commercial device offer: -7V to +12V. (high speed performance not known)
2. **Improved higher absolute max rating**
    a. Requirement for logic inputs: -0.5 to+6V
    b. Requirement of supply max rating: -0.5V to +4.6V
3. **Increased ESD tolerance**

    a. 8kV – 15kV (HBM)
    b. Commercial device such as TI SN65LVDS33 ESD protection exceeds 15kV.
4. ***TID, SEU and SET thresholds***
    a. Devices with spec. for TID: <300krad(si)
    b. No SEL: > 80 MeV-cm^2/mg
    c. No SET: > 80 MeV-cm^2/mg

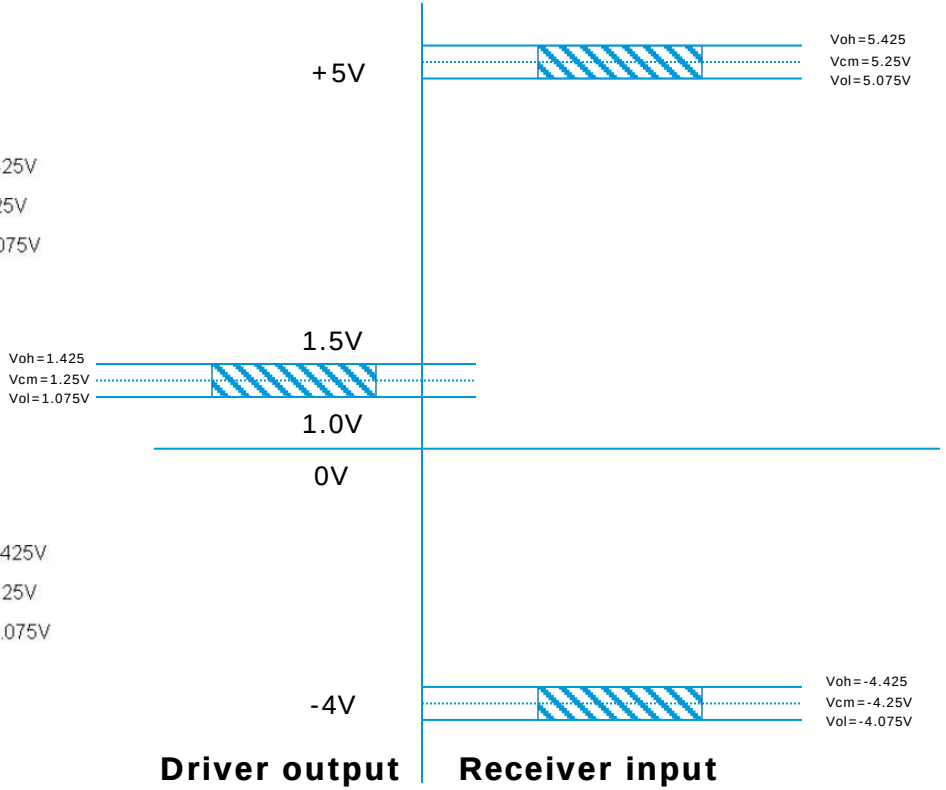
TIA-644a common noise range

Improved LVDS receiver common range

Standard EIA/TIA 644a device



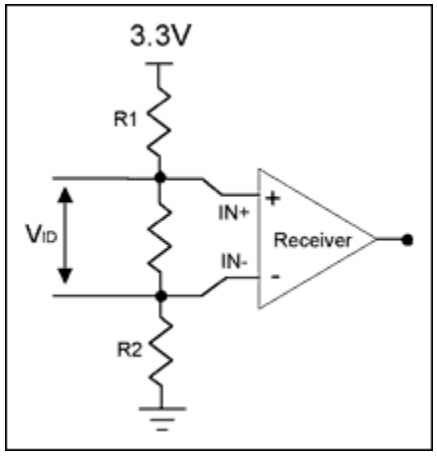
improved EIA/TIA 644a device



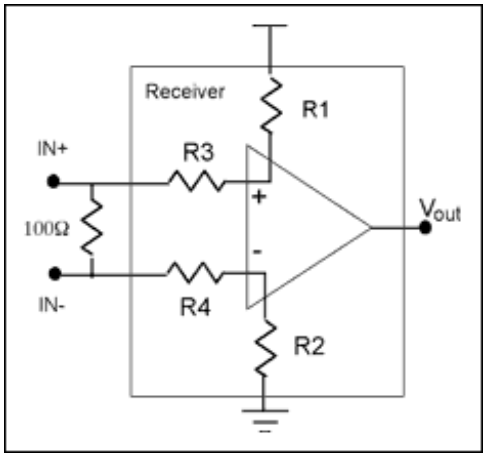
LVDS failsafe

The LVDS receiver's output should have a stable output under the following conditions

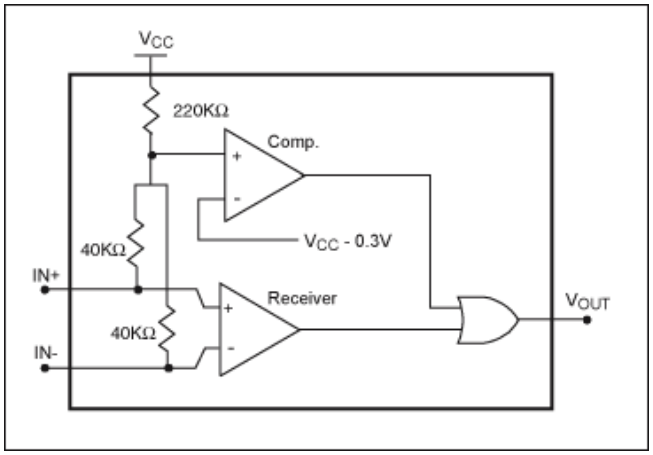
1. **Open inputs:** unused input pins should not lead to an oscillating output.
2. **Floating inputs:** if the LVDS driver is in tri-state, powered off or link broken, the receiver output must have a stable logic high-input.
3. **Shorted inputs:** Receiver output must be logic-high.



External bias network



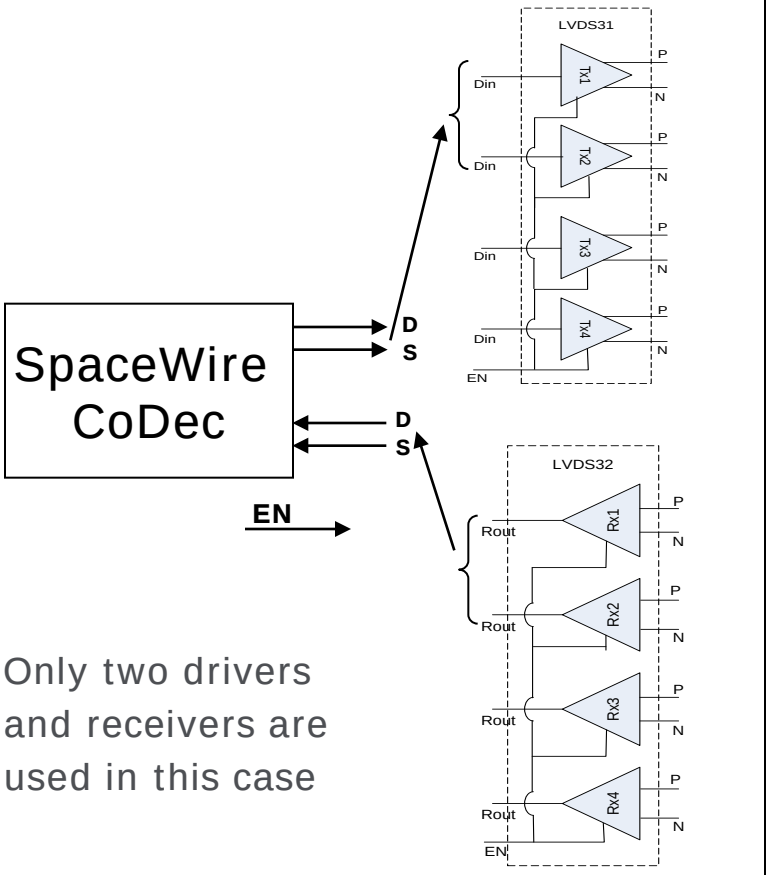
Internal bias network



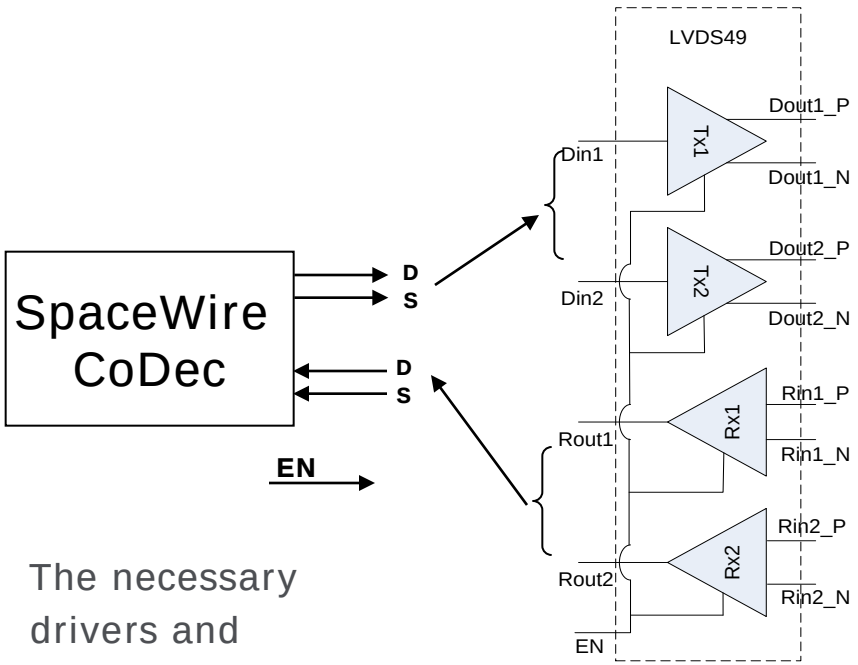
Active failsafe circuit

What additional functions are needed?
LVDS transceiver for SpaceWire

The available LVDS components for space does not always allow optimal solutions….



Only two drivers and receivers are used in this case



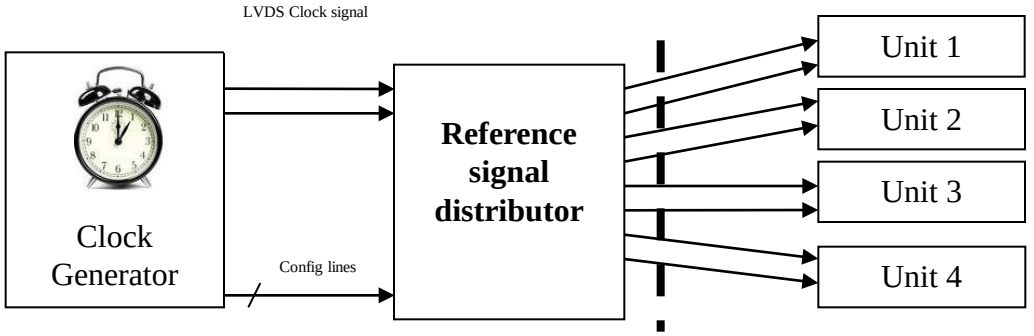
The necessary drivers and receivers in one package.

What additional functions are needed?
Reference signal distribution

– Not many Space Components on the marked fulfil this function for EIA/TIA 644 LVDS

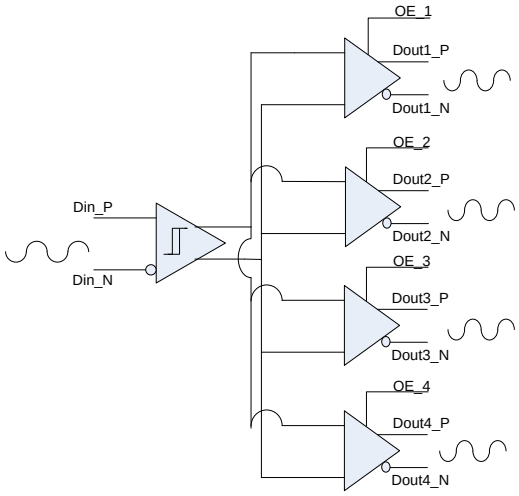
– Low jitter and skew are key requirements

– Adequate fault tolerance is required



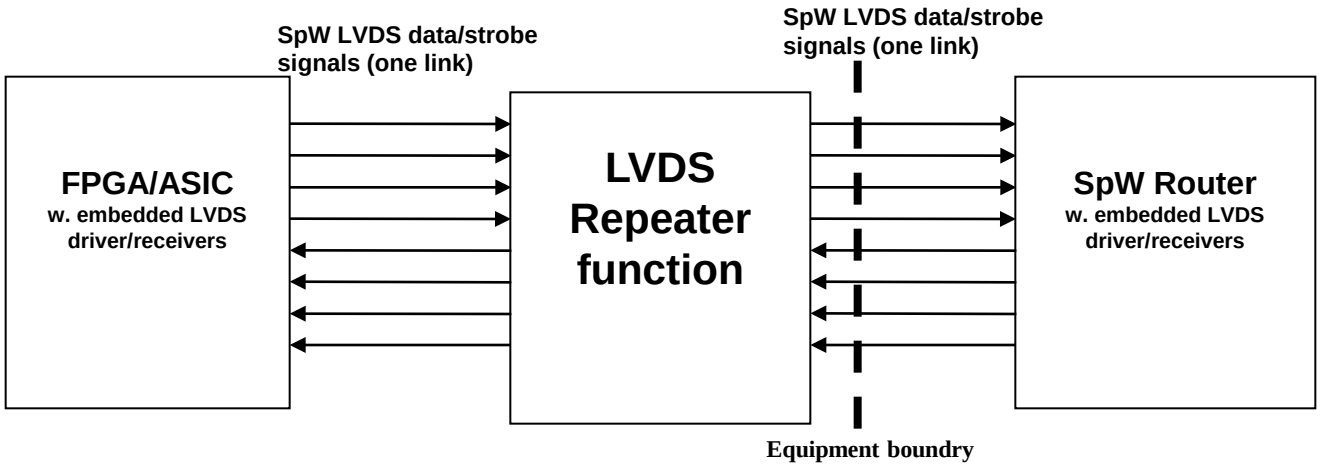
Function is ideal for;

- backplane and interconnect applications
- clock/data distribution
- Signal switching



What additional functions are needed?

LVDS Signal repeating



Some ASIC or FPGA might have ESD sensitive LVDS buffers

➡ **Protection of costly ASIC/FPGA devices**

Some space FPGAs do not LVDS conform to ANSI/TIA/EIA 644

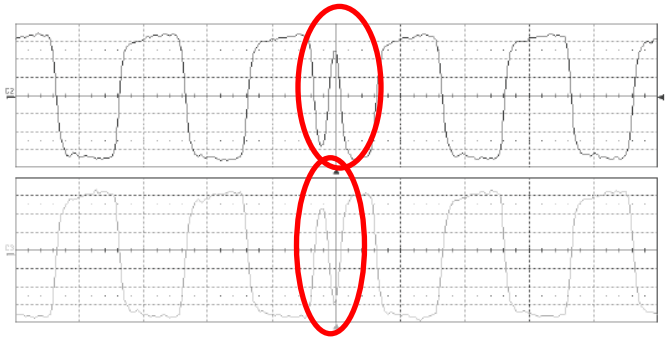
➡ **Convert non compliant LVDS to ANSI EIA/TIA 644**

Signal losses of high speed LVDS signals can be adverse

➡ **Ensure high speed signal over longer transmission paths**

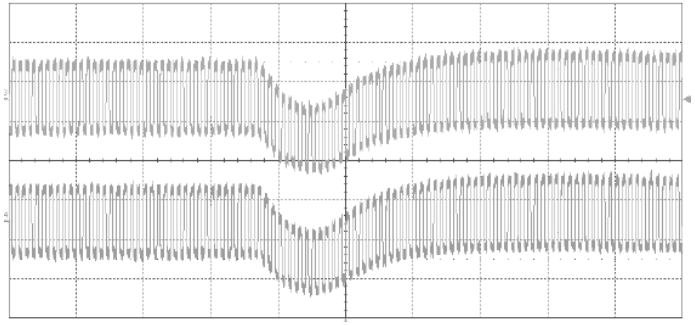
Possible issues

1. Patents LVDS circuit enhancements
    a. A survey is necessary
2. Single event transient effects at levels below 80Mev*mg/cm^2



SET - Split polarity

SET – Reverse polarity



SET – Common mode loss

To catch SETs as depicted a pulse width detection method was used.

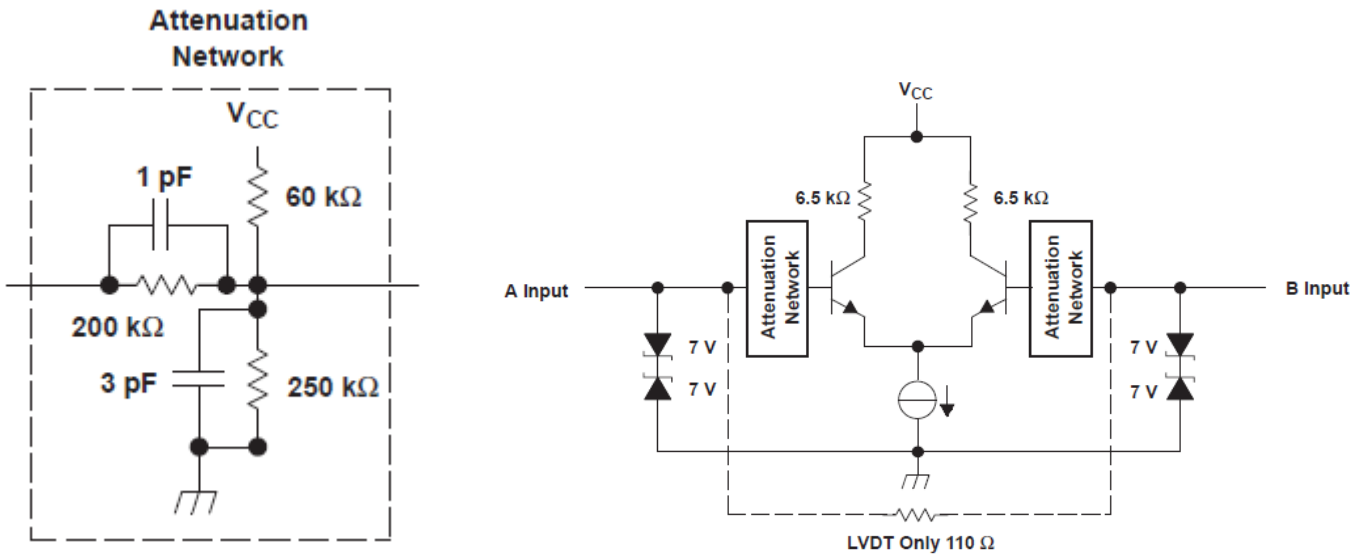
** Results reported in IEEE paper; Single Event Sensitivity of High-Speed Differential Signaling Devices to Heavy Ions and Protons, R.Koga et al.

Thank you for your attention

Backup slides

TIA-644a common noise range
Improved LVDS receiver common range

An example from Texas Instruments which offer improved common mode range receivers



LVDS standards

LVDS Standard	Standard Characteristics	Comments
ANSI/TIA/EIA-644-1995	3.5mA drive, max data rate of 655 Mbps and theoretical max of 1.923 Gbps based on a loss-less media. Fail-safe operation of the receiver under fault conditions is discussed Baseline point-to-point, other configurations issues as multi-receiver operation.	ANSI/TIA/EIA-TIA version is the most generic and it is intended to multiple applications
IEEE 1596.3 Scalable Coherent Interface-SCI	is an application specific standard “SCI”.Originally electrical specifications were based on ECL technology. Addresses only high data rate aspects, not low power concerns. Specific encoding for packet switching. Could be used in single-ended mode over short distances (4 wires)	Features similar: driver output levels, receivers threshold and data rate Differs in load conditions
ANSI/TIA/EIA-899–M LVDS	10mA drive, extends from point-to-point applications to multi-point and multi-drop applications, M-LVDS (& BLVDS) products are capable of data rates in excess of 3 Gbps.	MLVDS (Multipoint-LVDS) features only similar voltage swing but higher drive current. Suited for multi-drop applications.
B-LVDS National Semiconductor	10mA drive current. Very similar to TIA/EIA-899 M-LVDS	BLVDS is actually not a formal standard.
G-LVDS proprietary Standard	Does not specify any transmitter drive current Places the driver output voltage offset closer to ground potential.. Point-to-point.	Ground referenced LVDS. Allows very low power chips.

Requirements for new LVDS devices

1. Adhere to the **ANSI TIA/EIA 644A** standard

2. Support larger **common mode voltage** tolerance (e.g. SN65LVDS33)

3. **Higher maximum rating,**
    a. **Supply i.e. -0.5V - +4V**
    b. **LVTTL inputs i.e. -1V – +6V**
    c. **LVDS inputs i.e. -5V - +6V**
4. **Cold sparing**
    a. **Facilitate redundant system architectures**
    b. **low leakage current e.g. +/- <= 20uA**

5. **Integrated fail-safe circuit**

Requirements for new LVDS devices

7. **Radiation tolerance**
    a. **latch-up threshold > 80 Mev-cm²/mg**
    b. **Total dose > 300Krad**
8. Support **high speed** ASIC LVDS signals >= 200MHz
    ! Up to **300MHz** and beyond for ASIC LVDS buffers/receivers
9. **Facilitate SpaceWire implementations** i.e. have an optimal number of drivers and receivers in one package
10. **Buffer and distribute** low jitter clock signals over LVDS
11. **Repeater function for** LVDS signals
    1. Facilitate distribution of longer distances
    2. Facilitate ASIC **LVDS driver / receiver protection**
12. Availability of **commercial grade equivalent components**