European LVDS Driver Development and ESCC Evaluation and Qualification

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Quick introduction

- ESA Contract (ECI phase 3)
- 24 month development in three phases:
  - Definition and preliminary design
  - Design, prototype manufacture, test
  - ECSS qualification
- Development and ESCC Qualification of 2 LVDS ICs:
  - Dual Transceiver, 16 pin (type: National Semi. DS90LV049Q)
  - 4x4 Cross-Point Switch, 40 pin (type: Texas Instrument SN65LVDS125a)
- Based on technologies and companies with space heritage
  - Rad Hard CMOS
  - Hermetic sealed ceramic flat package
  - ESCC assembly and test
Consortium

▼ Aeroflex Gaiser
   - Requirement Definition
   - Package development
   - IC Assembly
   - System Validation
   - Evaluation board development and manufacturing
   - Radiation Testing
   - Product Documentation
   - ESCC Evaluation and Qualification
   - Commercialization of the product

▼ IMEC
   - IC Design and Verification
   - Management of Wafer production

▼ Hirex Engineering
   - Functional and Electrical validation testing
   - ESCC Evaluation testing and Screening testing
   - ESCC Qualification testing
Project team

- Project Manager
  - Sandi Habinc

- Contract Manager
  - Per Danielsson

- Component Engineering
  - Fredrik Sturesson

- Hardware Engineering
  - Marko Isomäki

- Product Assurance
  - Fredrik Sturesson

- Hirex
  - Technical Manager
    - Jean-Francois Pascal

- IMEC
  - Project Manager
    - Jan Wouters

  - Hirex
    - Quality Manager
      - Yannick Soler

  - IMEC
    - Manufacturing Manager
      - Paul Malisse

  - IMEC
    - Design Manager
      - Geert Thys
Key features

- TIA/EIA-644 compliant LVDS inputs and outputs
- 3.3V single supply
- 3.3V LVTTL compatible input / output
- Up to 400 Mbps switching rates
- Tri-state output control

- Robust design, ESD, voltage tolerance, failsafe, coldsparing
- Radiation hard
Robustness (1/2)

▶ ESD robustness
  – 8 kV HBM ESD Level

▶ Overvoltage tolerant (transients)
  – Supply: -0.5V / 4.6V
  – LVTTL: -1V / +6V
  – LVDS: -5V / 6V

Low risk of failure propagation at overvoltage, powered and un-powered.
Robustness (2/2)

▼ Receiver Extended Common Mode Input
  – -4V / +5V

▼ Receiver with Active Failsafe Operation
  – High state at floating or shortened inputs

▼ Cold Spare outputs
  – For cold spare redundancy in multi-point systems

▼ 5V tolerant TTL inputs
Radiation

▼ TID hard
   > 300 krad(si)

▼ SEL immune
   > 110 MeV-cm2/mg

▼ SEU/SET immune
   > 80 MeV-cm2/mg

by proven Rad Hard CMOS technology
Library extension for DARE 180 nm

- Receiver Extended Common Mode Input
- Receiver Failsafe Operation
- Cold Spare Functionality
- 8 kV HBM ESD Level
- Single Supply Capability
- Removal of External Resistor Requirement
The LVDS IC devices

▼ Dual Transceiver LVDS IC (pin compatible to DS90LV049Q) features the following pin types and counts (16 pins in total):

- LVDS receiver pairs (+/-) 2 (2 pins each)
- LVDS transmitter pairs (+/-) 2 (2 pins each)
- LVTTL receiver output 2
- LVTTL transmitter input 2
- LVTTL enable (positive/negative) 2
- Supply 2

▼ The 4x4 Cross-point Switch (pin compatible to SNLVDS125A) features the following pin types and counts (38 pins in total):

- LVDS receiver pairs (+/-) 4 (2 pins each)
- LVDS transmitter pairs (+/-) 4 (2 pins each)
- LVTTL selectors 8
- LVTTL enables 4
- Supply 10
4x4 Cross-Point Switch (1/2)

▼ **Functionality and pin compatibility:**
- TI SN65LVDS125A

▼ **Ceramic flat package (baseline):**
- 40 leads bottom brazed
- 1.27 mm pitch
- 26.7 mm x 9.0 mm x 2.5 mm
4x4 Cross-Point Switch (2/2)

Configuration Examples:
- Selection with S10-S41
Dual LVDS Transceiver

▼ Functionality and pin compatibility:
  – NSC DS90LV049Q
  – Ideal for Space Wire: “one channel, one package”

▼ Ceramic flat package (baseline):
  – 16 leads bottom brazed
  – 1.27 mm pitch
  – 10.5 mm x 7.5 mm x 2.2 mm
Feedback: Dual Transceiver

By removing one of the enable pins this pin can be used as a mode pin:

- Default enable value: Dual Transceiver
- Not the default enable value: 2x2 Cross-point Switch

服役 Use the two LVTTL inputs Din1 and Din2 as selectors
服役 Use the two LVVTL output pins Rout1 and Rout2 for debug
Feedback: 4x4 Cross-point Switch

<table>
<thead>
<tr>
<th>SNLVDS125A</th>
<th>UT54LVDM288</th>
<th>UT54LVDM328</th>
<th>DS90LV049Q &amp; UT54LVDM055</th>
<th>UT54LVDS031</th>
<th>UT54LVDS032</th>
<th>Custom</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single 4x4 crosspoint</td>
<td>Quad 2x2 crosspoint</td>
<td>Octal repeater</td>
<td>Dual Rx &amp; Tx</td>
<td>Quad Tx</td>
<td>Quad Rx</td>
<td>Redundant Rx &amp; Tx</td>
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<tr>
<td>Signal / Mode</td>
<td>Single</td>
<td>Dual</td>
<td>Quad</td>
<td>Dual</td>
<td>Quad</td>
<td>Quad</td>
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<tr>
<td>LVDS TX</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>8</td>
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<tr>
<td>LVDS RX</td>
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<td>8</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>8</td>
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<tr>
<td>LVTTL DATA IN</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>LVTTL DATA OUT</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>ENABLE</td>
<td>4</td>
<td>4</td>
<td>4 (not 1)</td>
<td>2</td>
<td>4</td>
<td>4 (not 1+1)</td>
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<tr>
<td>SELECT</td>
<td>8</td>
<td>4</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
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<tr>
<td>GND</td>
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<td>6</td>
<td>4</td>
<td>4</td>
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<tr>
<td>VCC</td>
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<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
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SN65LVDS125A

ESCC LVDS 4x4 Cross-Point Switch

4x4 MUX

SN65LVDS125A
Schedule

▼ August 2012
   - Specification / datasheet

▼ August 2013
   - Prototypes available
   - Prototype boards available

▼ April 2014
   - ESCC qualification och ESCC QPL
Aeroflex Gaisler and space components

- **GR712RC, Dual Core LEON3FT processor**
  - 240 pin CQFP
  - Prototypes
  - MIL-STD-883 space flow
  - Prototypes
  - MIL-STD-883 space flow

- **SpaceWire Router**
  - 256 pin CQFP
  - Prototypes
  - ESCC 9000

- **LVDS components**
  - 16 pin FP & 40 pin FP
  - Prototyper
  - ESCC qualification
Contact information

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▼ Board information:
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▼ Software and tools information:
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