32-bit microprocessor with SpaceWire routing switch for space applications

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Outline

- introduction of SRISA RAS
- current space products
- description of the 32-bit uP with SW router
- conclusions
SRISA RAS in facts

- Was founded in 1986
- More than 700 scientists
- Located in Moscow
- www.niisi.ras.ru
SRISA main fields of research

- theoretical problems of the programming automation and data security
- HPC theoretical base
- system software: the RTOS, compilers, debuggers, …
- microelectronics
  - R&D of high performance chips for HPC (uP, DSP, RapidIO switch, …)
  - R&D of rad-tolerant and fault-tolerant CPUs and interface circuits for space applications
SRISA’s Research Fab

- Up to 0.25 um, 5 LM
- CMOS, CMOS SOI
- No volume production
- Located in Moscow
space products: MCM BT83_micro

- 32-bit microprocessor
- 2xMIL1553B
- 4x128KByte SRAM
- PCI, RS232, GPIO, …
- 0.5 um CMOS SOI
- 33 MHz
- TID >200krad
- SEL immune
space products: K32-TMR

- 32-bit FT-microprocessor
- 0.35 um CMOS SOI
- 66 MHz
- on-chip TMR
- TID >200krad
- SEL immune
- SEU*, cm²/bit <2*10⁻¹²
- SEFI, cm²/chip <5*10⁻⁷

* - parity check disable
Current Space Applications

- SUBMICRON have developed computers for Russian space ships (SOUZ-TMA and PROGRESS) and satellites (RESURS-P) on the base of SRISA’s chips.
- Several new on-board computers are being developed.
32-bit uP ‘ORBITA’ block diagram
5-port SW routing switch

* with RMAP support
ORBITA main features

- >100 MHz MIPS32-like microprocessor
- 0.25 um CMOS SOI
- TID >200krad
- SEL immune
- Full set of software: OS2000 RTOS, gcc compiler, ...
Current status

- FPGA prototype passed almost all tests of STUR-Dundee conformance tester
- First engineering samples are expected by the end of 2012 (CPGA602 package)
SpaceWire conformance testing stand
SpaceWire conformance testing stand (2/2)
### SpaceWire testing results

#### Test 1: Empty Packet (EOP)
- **Success:** Run Test
- **Result:** Empty Packet (EOP)
- **Maximum test duration:** 10
- **Packet bytes:**

#### Test 2: Send Packet With EEP
- **Success:** Run Test
- **Result:** Empty Packet Loop-back (EEP)
- **Maximum test duration:**
- **Packet bytes:**

#### Test 3: UUT is data loop-back
- **Success:** Run Test
- **Result:** UUT is data loop-back
- **Header bytes:** 0x00
- **Packet size:** 4

#### Test 4: UUT is data sink
- **Success:** Run Test
- **Result:** UUT is data sink
- **Header bytes:** 0x00
- **Packet bytes:** 0x65 0x0d 0x17 0x00 0x11 0x01

#### Test 5: UUT is data source
- **Success:** Run Test
- **Result:** UUT is data source
- **Maximum number of packets:** 10
- **Maximum test duration:**

#### Test 6: Investigate UUT timcode support
- **Success:** Run Test
- **Result:** Investigate UUT timcode support
- **Timecode to send:** 42

#### Test 7: Timecode/NCHAR confusion
- **Success:** Run Test
- **Result:** Timecode/NCHAR confusion
- **Timecode to send:** 42

#### Test 8: UUT ignores invalid timcodes
- **Success:** Run Test
- **Result:** UUT ignores invalid timcodes
- **Timecode to send:**

#### Test 9: Measure timcode frequency
- **Success:** Run Test
- **Result:** Measure timcode frequency
- **Test duration (seconds):** 10
Conclusions

- SRISA RAS is able to develop, manufacture and test RT and FT Systems-on-Chip, and we are open for cooperation.
- It’s rather difficult to develop SoC with SpaceWire nodes, when SW standard is not totally defined.
- Now, a new interface SpaceFibre for high-speed communication is being developed.
- May be, it is time to look once more at existing well-defined interfaces for speed >400 Mb/s? (Subset of RapidIO??)
Thank you!