High Speed Links perspective in future payload

International SpaceWire Working Group Meeting #18
24-26 April 2012, ESTEC, Noordwijk, The Netherlands

Session 1: System requirements (Convenor D. Jameux, ESA/ESTEC)

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All the space you need

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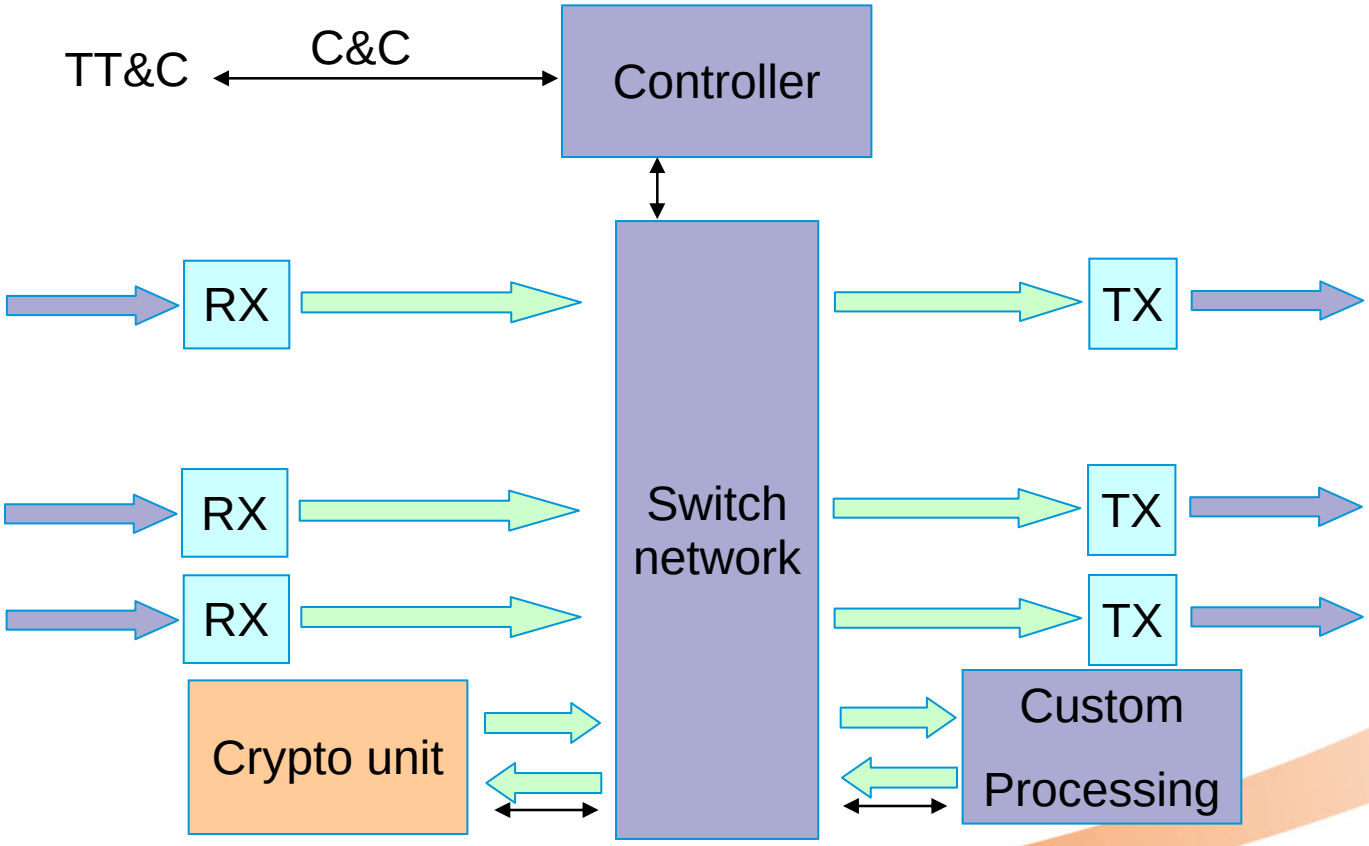
Outline

- Needs by application category
- Reference architecture
- Link usage
- Link requirements

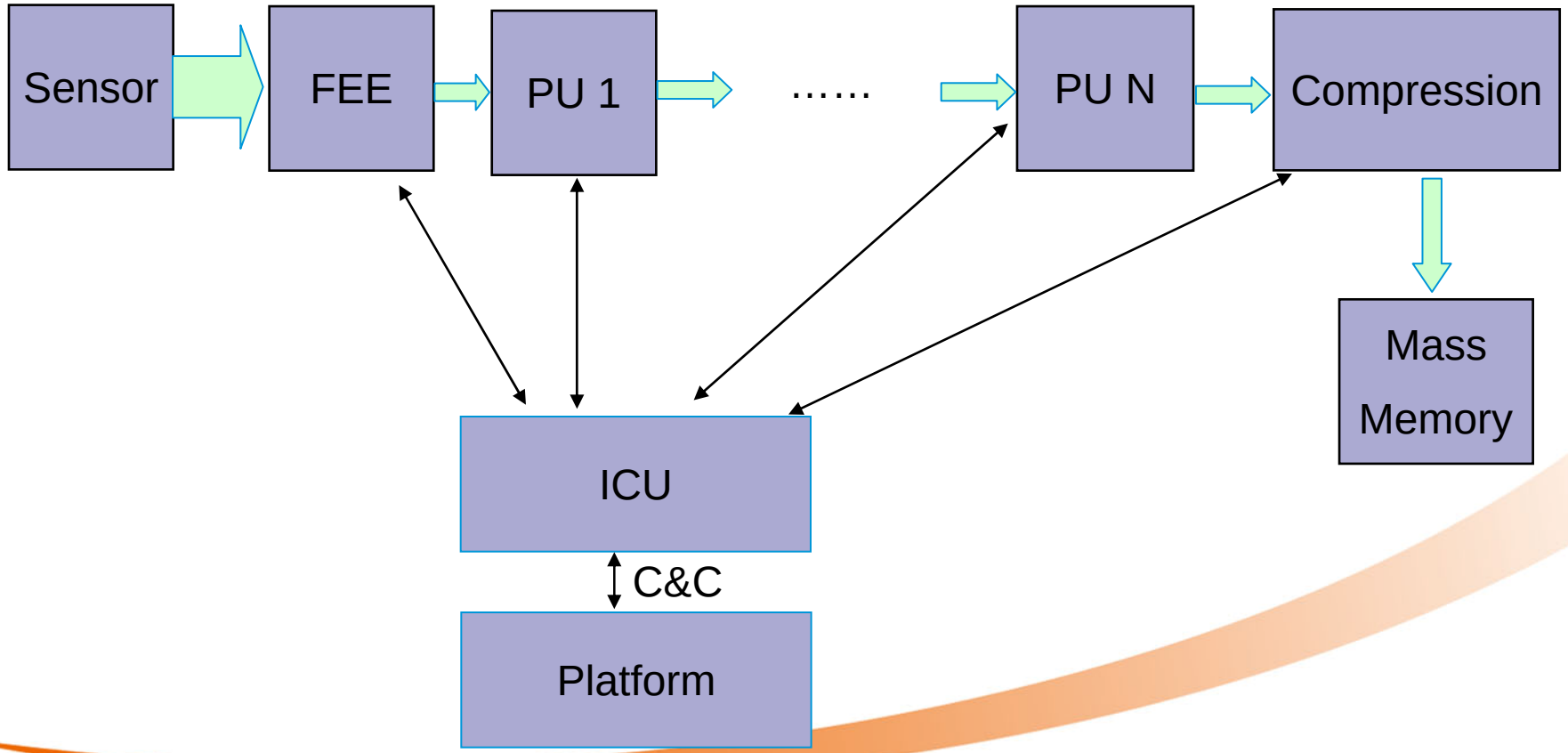
Need for very high speed link

Application categories		IO Speed Gb/s
1	Image Processing – Earth Observations – Optical	Variable
2	Image Processing – Earth Observations / Astro. – NIR - IR.	Variable
3	Image Processing – Astronomical – Optical Star based.	1 - 100
4	Image Processing – Astronomical – Optical Wide field.	1 – 100
5	Image Processing – Robotic Navigation	<0,2
6	Radar SAR – signal processing	0.2 - 1
7	Radar SAR – On-board image processing & feature extraction	> 100
8	Telecom/SAR (Multi) Beam forming and Steerability.	> 100
9	Telecoms DSP – Transparent	> 100
10	Telecoms DSP – Regenerative	> 100
11	Soft Radio – reconfigurable payload data communication interface.	0.2 - 1
12	Standard Compression	0.2 – 1
13	Payload Crypto	0.2 – 1
14	Radiometry – Spectral analysis e.g. WBS	0.2 – 1
15	Specials	Variable

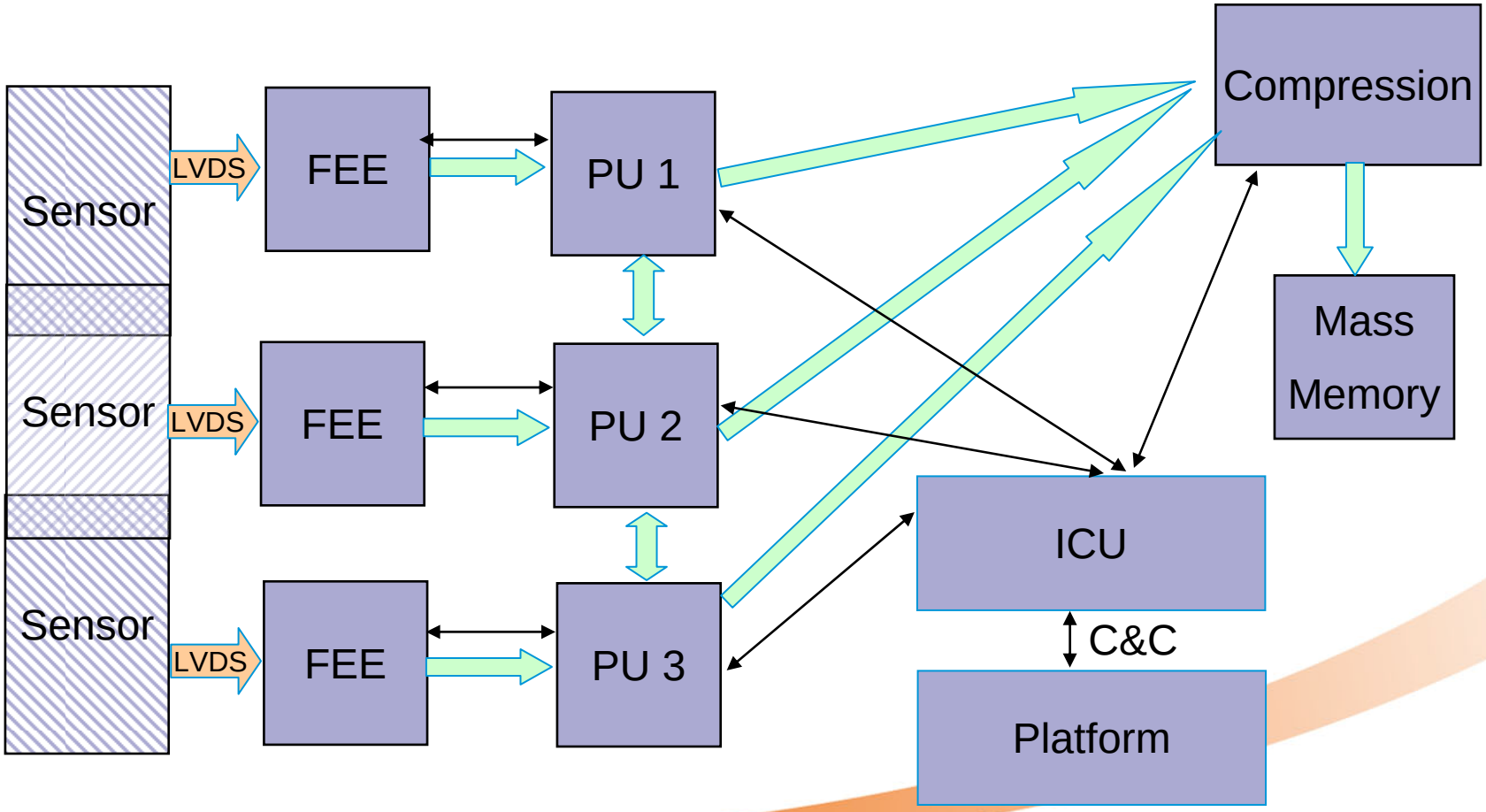
Telecom payload reference architecture



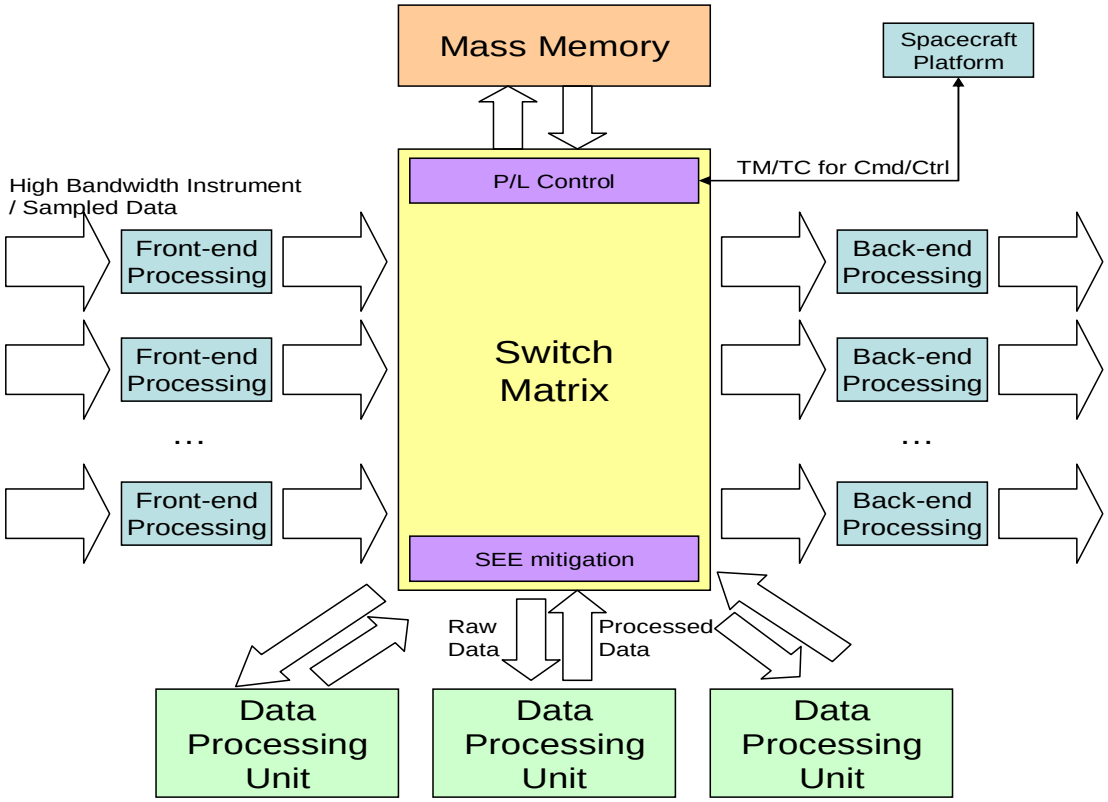
Heavy processing



Parallel processing with data overlapping



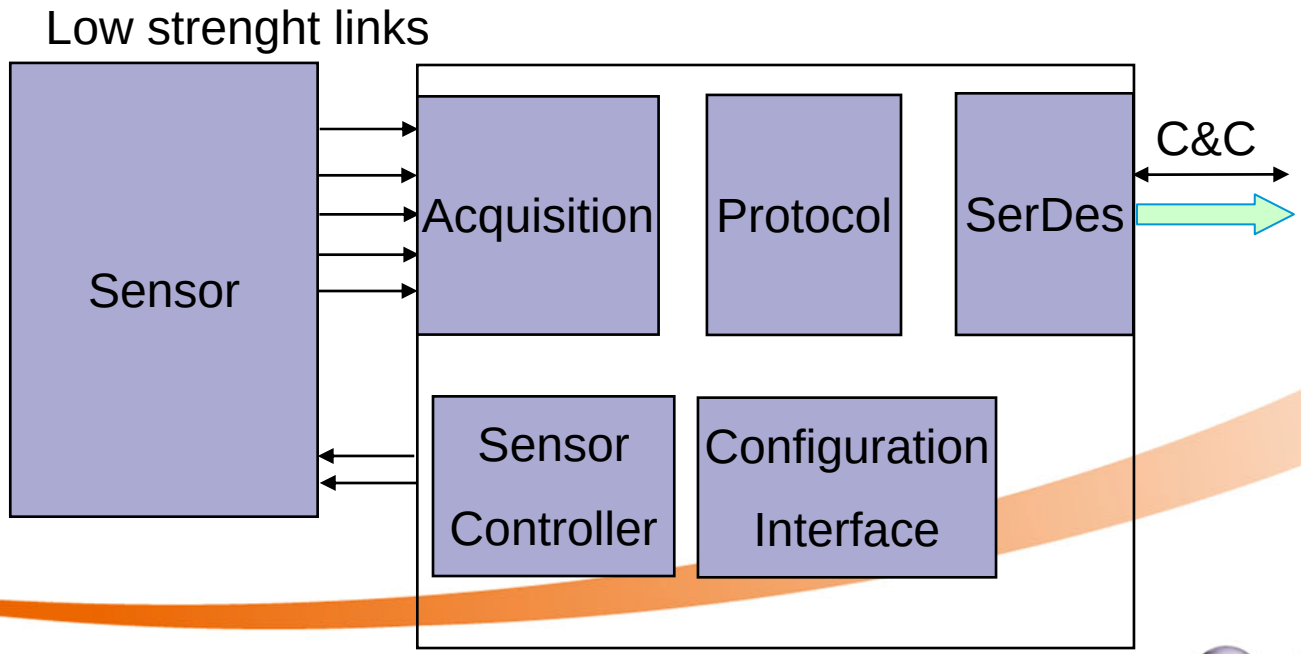
High Performance Science architecture



Link usage

Data concentration

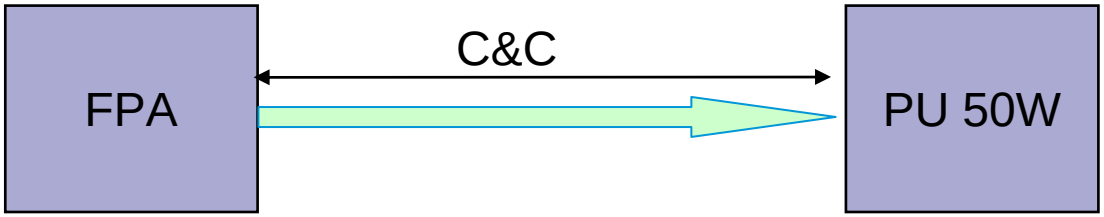
- Multiple sensor outputs gathering
- Trade off at protocol level with the number of required VC and port



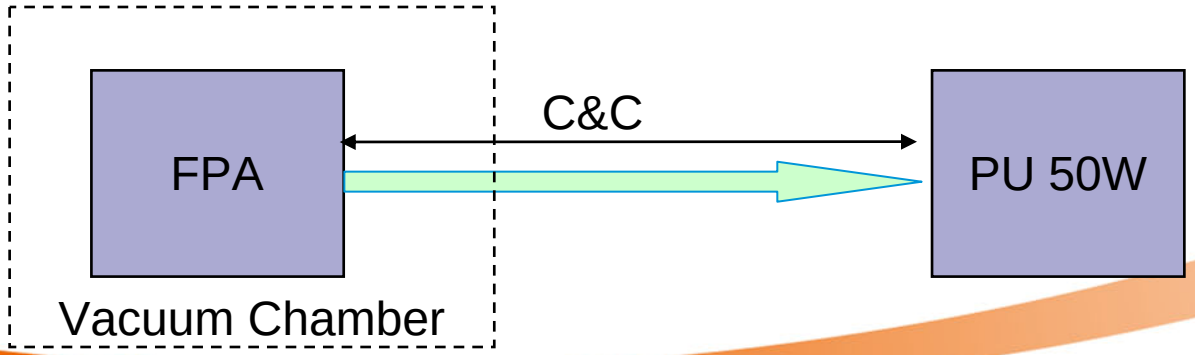
Link usage

Data transmission

- Long distance (several meters) for thermal or mechanical issue



- For testing

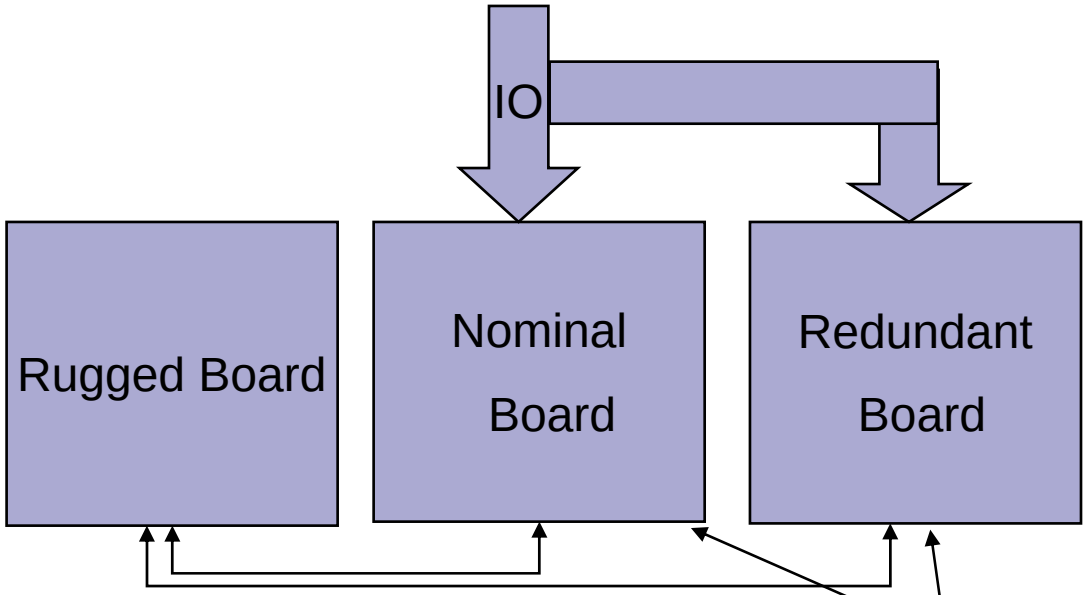


Link requirement : Raw data transmission

- Small connector
- Light weighted
- Point to point traffic (stream)
- Simple protocol (no need for flow control)
  - Minimal overhead
- Scalable (multi lane aggregation)
- Asymmetric (data >> control)
  - Sometimes unidirectional only

Link usage

- Inter processor
  - Backplane functionality with redundancy



- Data (memory mapped)
- Interrupt (TBC)
- Time Distribution
- DMA enabled

Board/slot power control

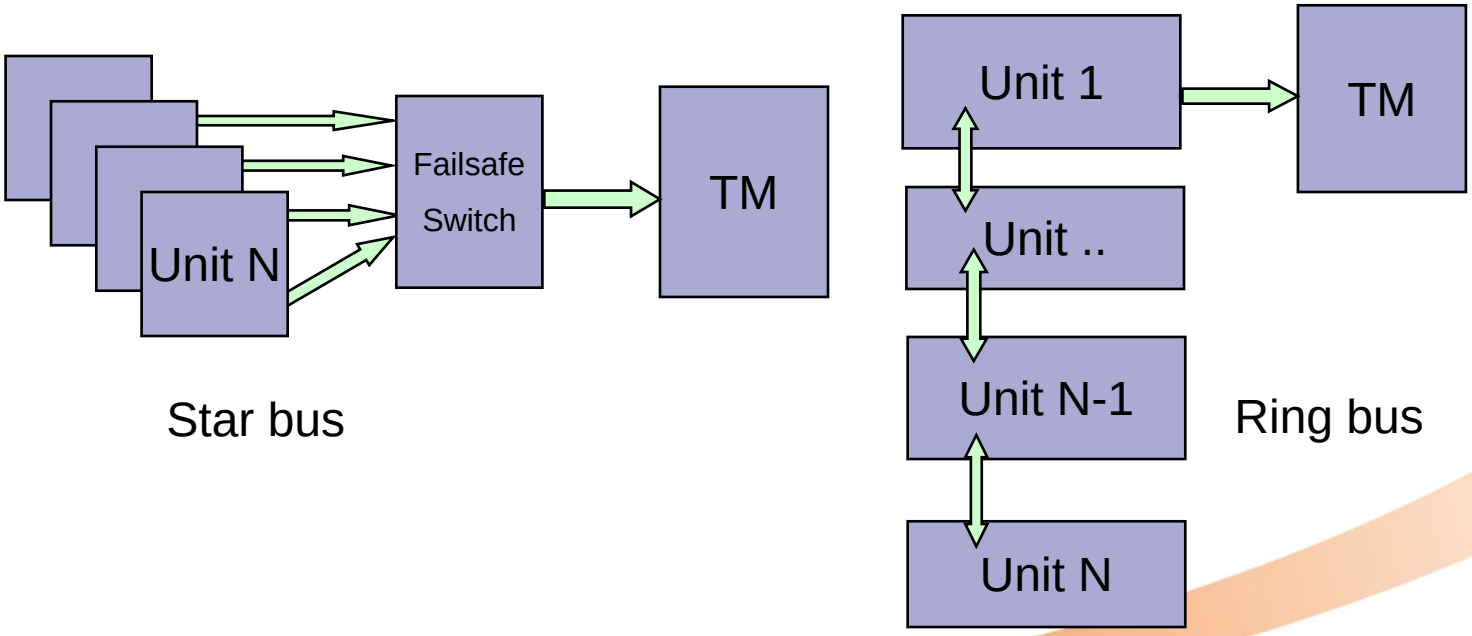
Link requirement : interprocessor communication

- Memory mapped traffic
- Interrupt capable (to be confirmed)
  - This need is linked with the IMA approach
- Board level
  - (backplane)
- System level
  - (distribution of the processing among several unit for thermal issue or mass repartition)
- Reliable

Link usage

Data aggregation

- Several processing unit towards a single Mass Memory or TM unit



Link usage

- Payload Control & Command
  - If a bidirectional data link exists it could be used for C&C
    - Internal to the payload
    - Between the payload and the platform
  - C&C requirements between platform and instrument
    - Up to 8 Hz refreshing rate
    - < 100 Kbits of data per second
  - Protocol candidate : Spacewire-D , TTethernet , AFDX

Key points

- Redundancy
- Connectivity
  - Signals should be defined connector should stay indicative except for evaluation and ground system.
- Configurability
  - Symmetry
  - Reliability
  - Services
- Interoperability
  - Usage with multi

Key Points

- Robustness
  - The SerDes fault model are known : single bit or up to thousand bits. How the fault is propagated/handled by the protocol/system ?
- Power consumption
  - A link is a huge power consumer
- Embeddable
  - The protocol stack and the SerDes could be integrated in a System On Chip, ideally in the sensor.

Switches

- Increase the system bandwidth compare to bus
- Failsafe architecture is expensive
- Standard component to be developed
  - Common effort and specification since it is the most re-usable part

IP commercialisation

- Low cost for evaluation and R&D purpose (GPL ?)
- Strong granularity with numerous options
  - E.G : Serdes, Retry ,Virtual Channelling, Memory mapped transfert,streaming, number of lane etc..

System implementation

- IMA Time & Space Partitioning
  - Bandwidth guaranteed
  - Hardware « guardians » at switch level
  - Remove asynchronism in the system (reactivity)

=> In theory no need for interruption or high priority message

Topology

- Mesh
  - Local switch
  - Redundancy issue
- Star
  - Centralized failsafe switch
  - Harness concentration
  - Standardized connectors are an issue

EGSE and Advance study tools

- Custom protocol are expensive
  - Tools need to be developped
  - No external support from a wide user community
  - No experimentation board available at low cost

Way forward

- Interworking between different electrical interface
  - CML vs VML
- Interworking with COTS
  - P4080
  - DSP

Thank you for your attention !

Questions ?