SpaceWire Backplane Application Requirements

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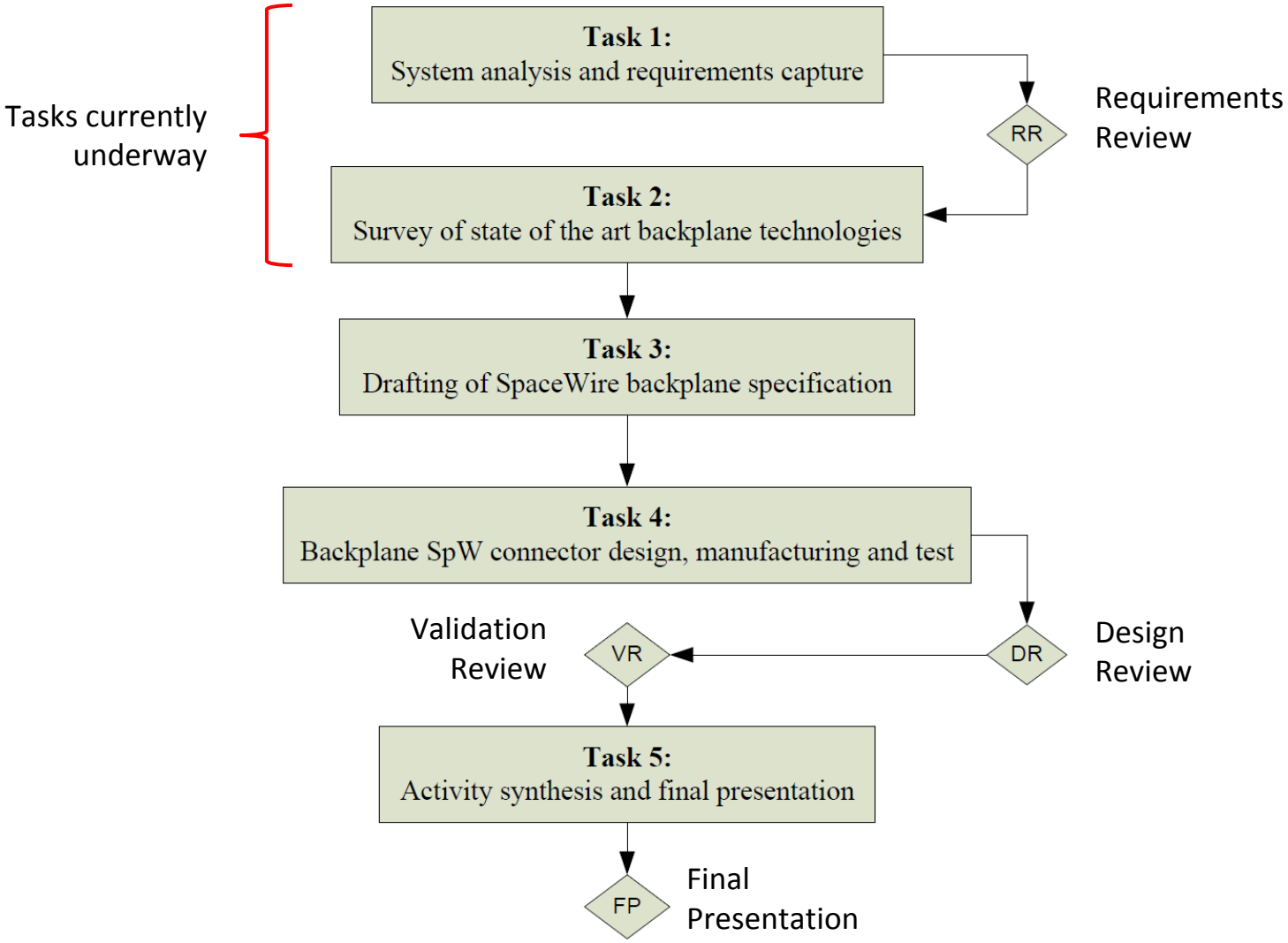
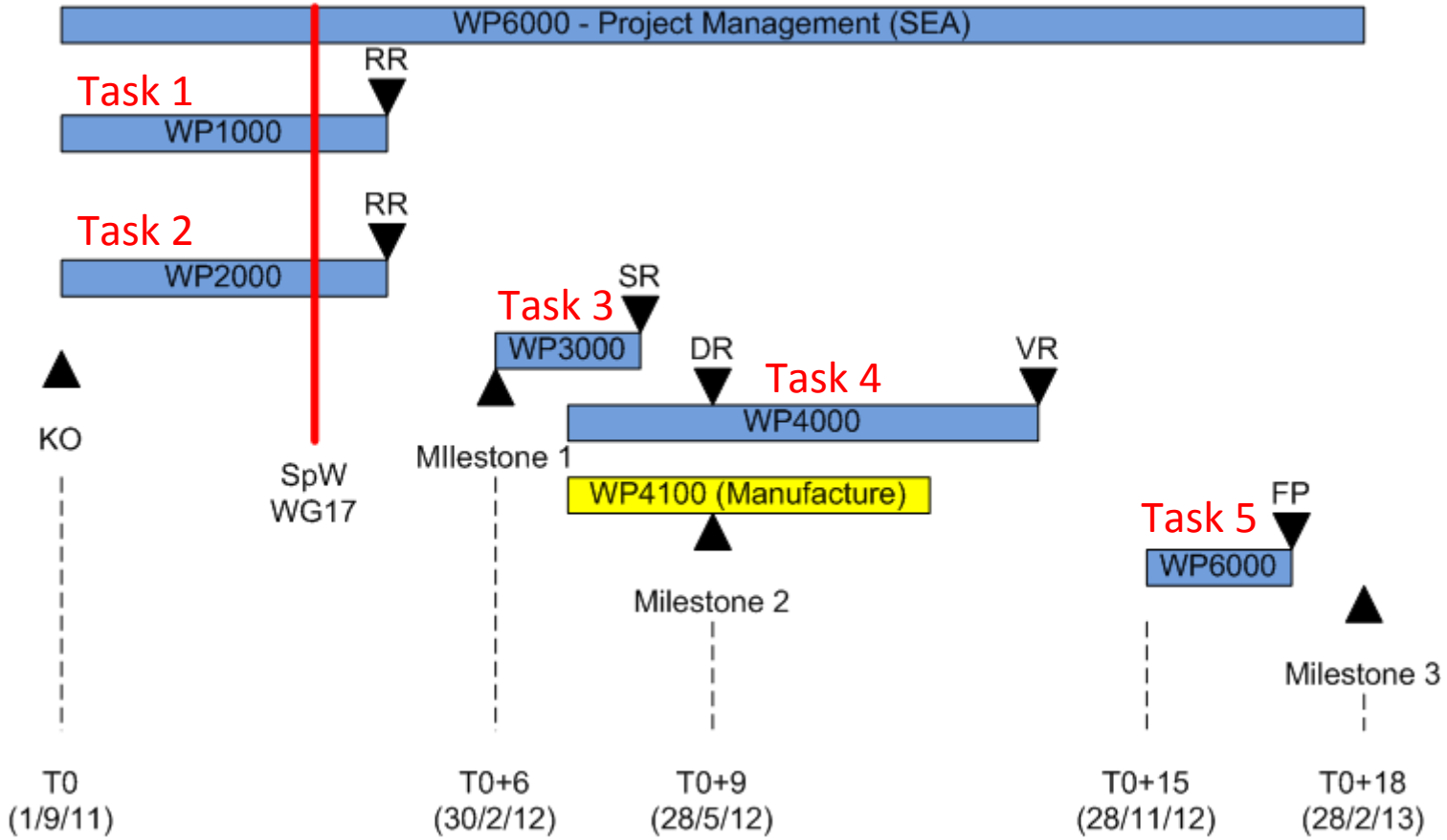
Summary

- The work presented is part of the ESA funded SpaceWire Backplane activity reference TEC-EPD/2010.88
- The activity tasks comprise:
  - Task 1: System analysis and requirements capture
    - Functional and performance requirements
    - Connector layout, dimensions, pinout etc
    - Constraints e.g. Slot count, fault tolerance
    - Compatibility with future space qualification to ECSS standards
    - Document outputs are: Analysis Report & Requirements Specification
  - Task 2: Survey of state of the art backplane technologies
  - Task 3: Drafting of SpW backplane specification (ECSS format)
  - Task 4: Backplane SpW connector design, manufacture and test
  - Task 5: Activity synthesis and final presentation

Work Logic



Schedule



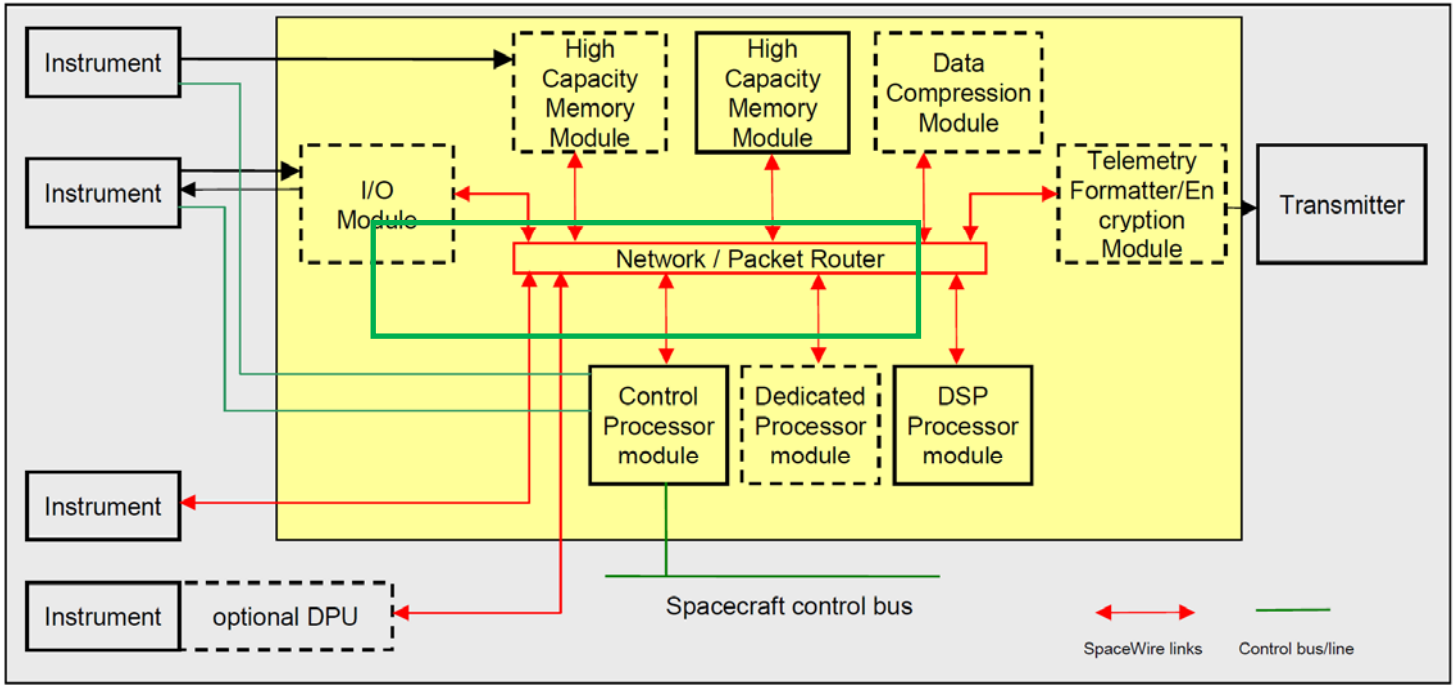
Task 1 Description

- Identify applications for SpaceWire Backplane
- Analyse these applications
  - SpW architecture (network and power)
  - Number of modules
  - Physical attributes (Form factor, connector location etc)
  - Connector characteristics (number of SpW ports and discrete signals)
  - Mechanical robustness (Stiffness of board)
  - Thermal management (Power dissipation)
  - Fault tolerance
  - Redundancy
- Requirements consolidation
- Requirements review – involving SpW WG

Applications for SpW Backplane

- Any Spacecraft unit that contains a number of modules which:
  - Need to communicate with data rate in the range 10Mbps to 2Gbps
  - Contain functions that are suitable for re-use in future spacecraft
- For example:
  - Spacecraft Management units
  - Data handling units
  - Platform control units
  - Instrument control units
  - Mass memory units
- Perhaps SpW Backplane not as applicable to:
  - Low rate Remote Interface Units (RIUs)
  - Instrument and sensor front-end applications

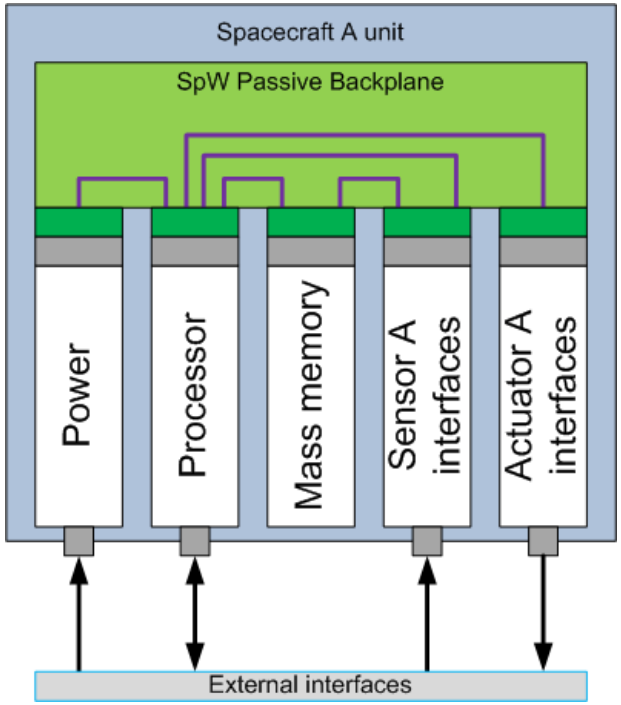
Data handling application for SpW Backplane



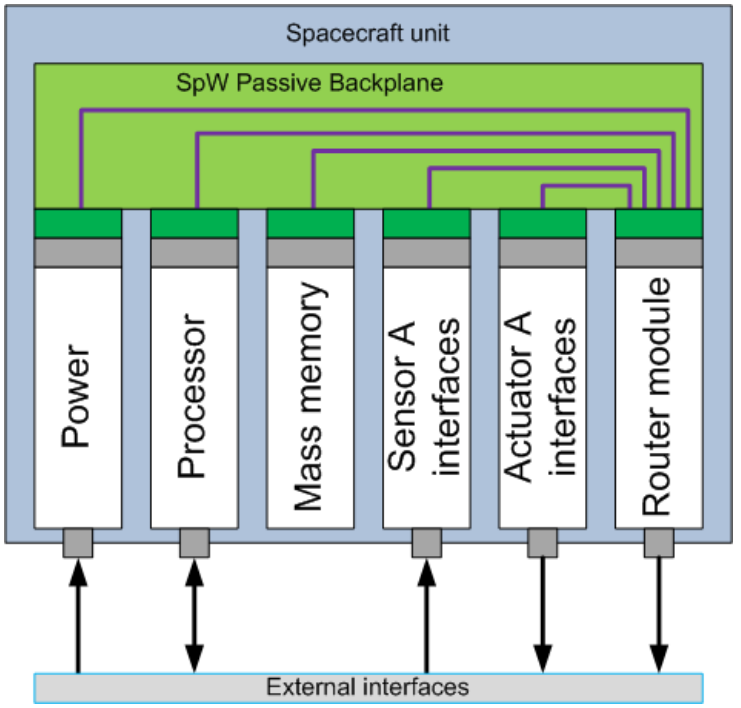
- 8 modules in non-redundant “unit” above, but we may have more I/O modules
- Typical spacecraft non-redundant unit has 3 to 8 modules
- MARC architecture combines prime and redundant on one backplane so twice the number may need to be accommodated

SpW “Passive” Backplane architectures

- Ad-hoc:
  - Routers are on the modules
  - Modules have 1 to N ports



- Centralised routing
  - Routers located in one module
  - Modules have 1 port
  - Router module has “N” ports



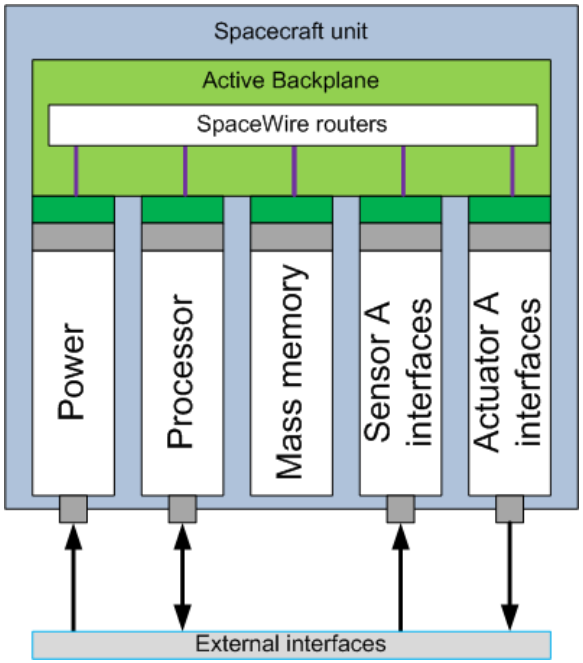
SpW “Active” Backplane Architectures

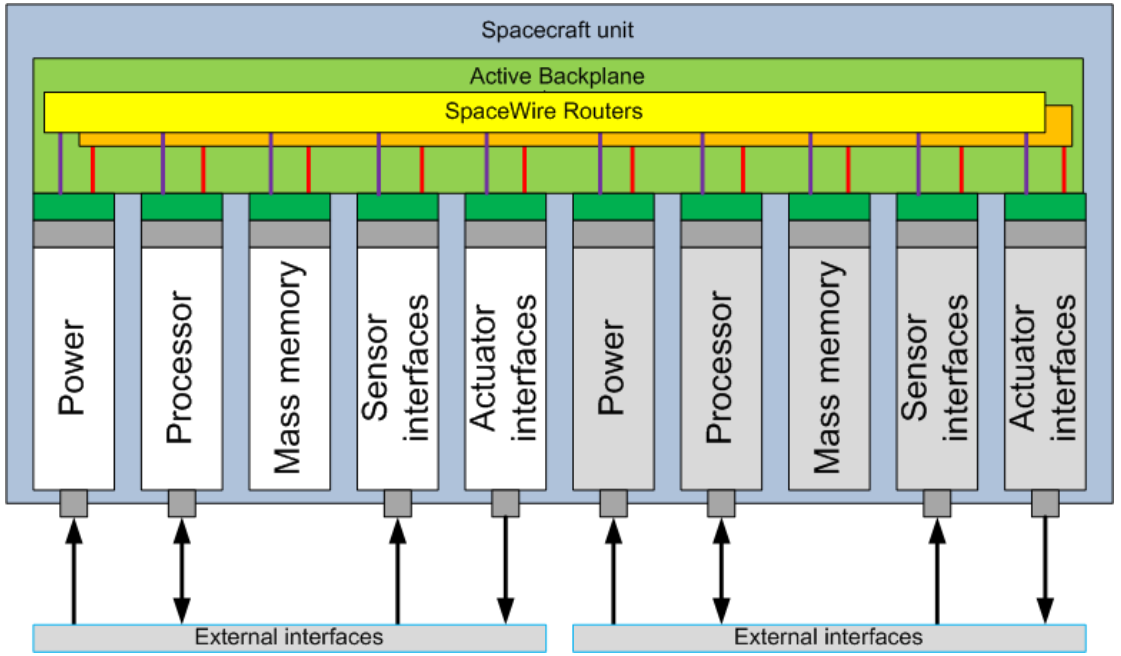
Basic Active Backplane

- Routers are on the backplane
- Modules have 1 backplane port

Redundant Active Backplane

- Routers are on the backplane
- Modules have 2 backplane ports

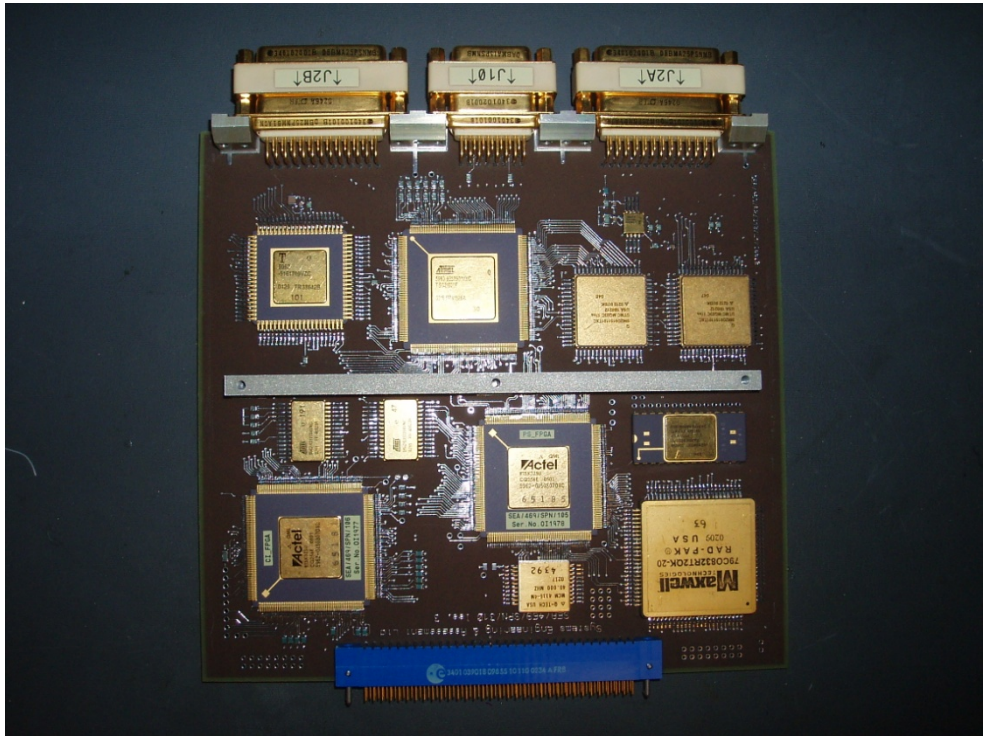




Physical attributes – compatibility issues

- Board size: large or small?
  - Adopt existing standard eg Eurocard, PCI express, microTCA?
  - Existing spacecraft board sizes are driven by device level packaging:
    - 352 pin quad flat packs
    - BGA technology as used for miniature terrestrial applications not generally used
    - Backplane connector
    - Unit external interface count and connectors
- Connector card guide specification, allowing for thermal conduction paths for TBD watts
- Board location (e.g. Simple slot, Bircher, Camloc or Wedgeloc)
- Front panel and associated mechanical interfaces

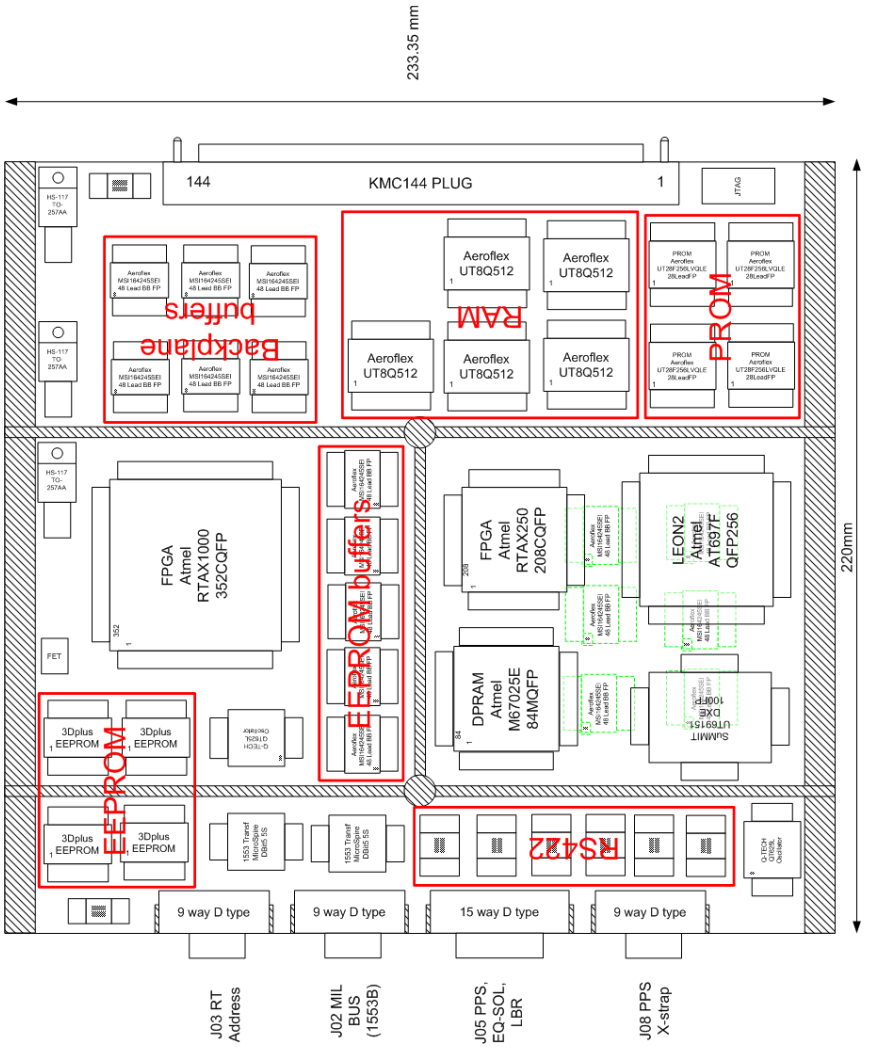
PCB board size (1)



184mm x 170mm Flight PCB

- Board sizes less than 160mm x 160mm generally not used for common packaged parts due to:
  - Restricted area for components
  - Large area occupied by connectors

PCB board size (2)

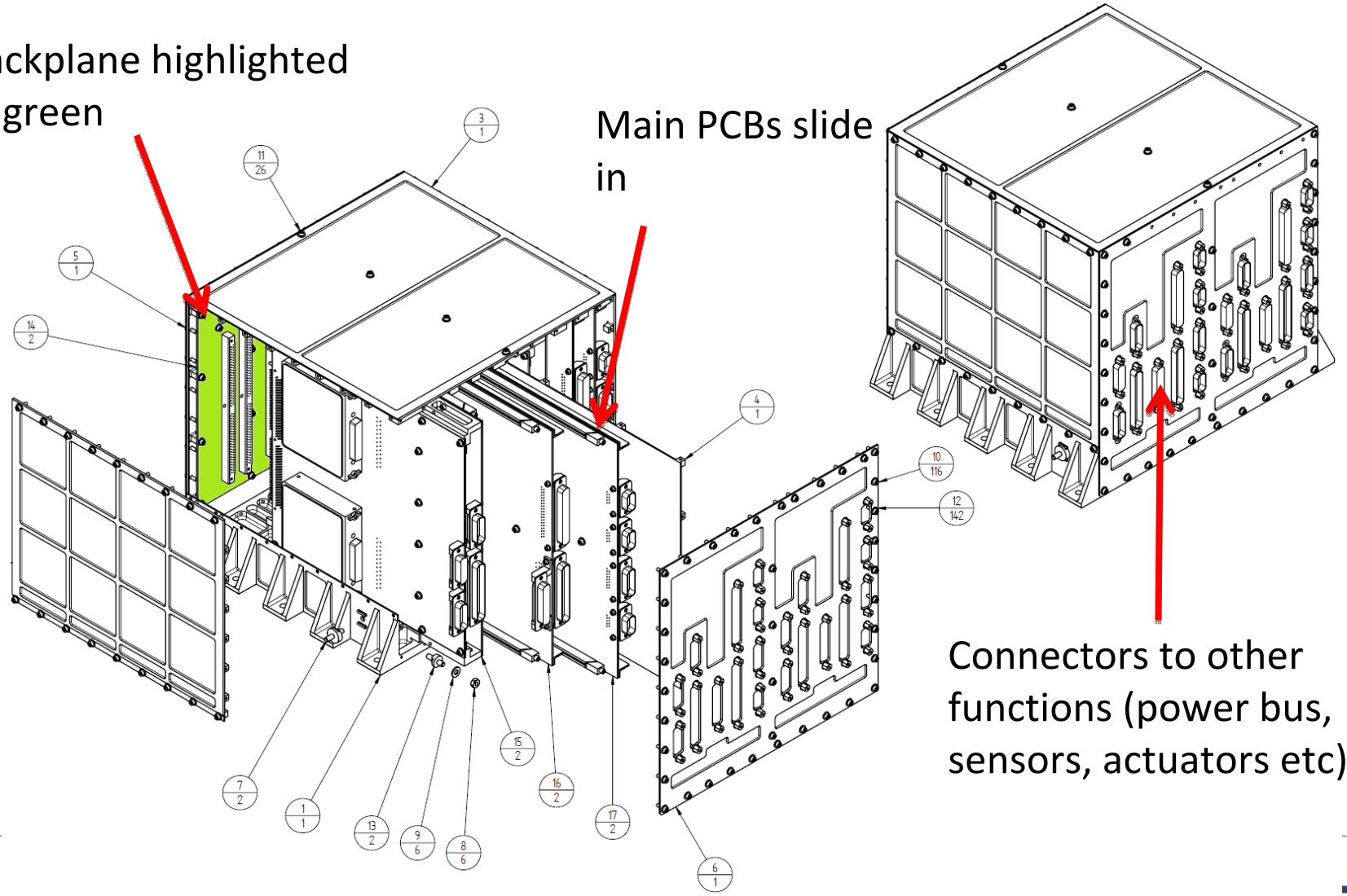


- Extended double Eurocard size is a terrestrial standard board size:
  - 233mm x 220mm
- Other common Eurocard sizes:
  - Single: 100mm x 160mm
  - Double: 233mm x 160mm

Physical attributes (unit level example)

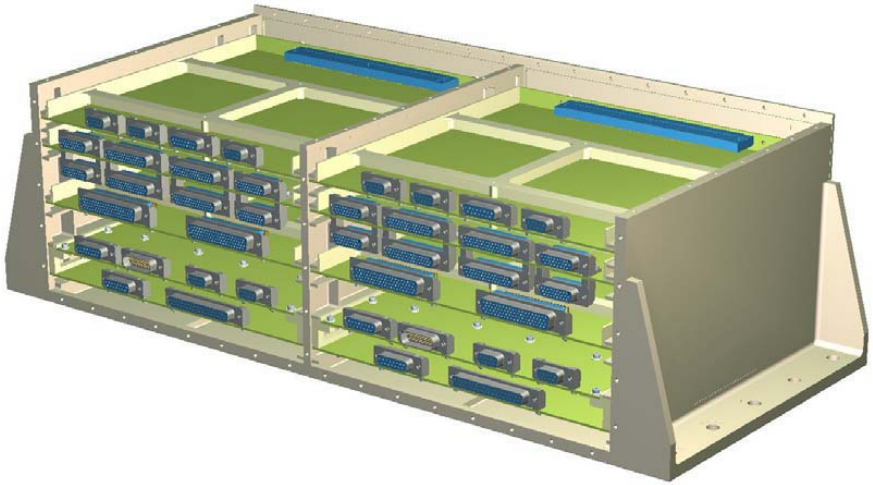
Backplane highlighted in green

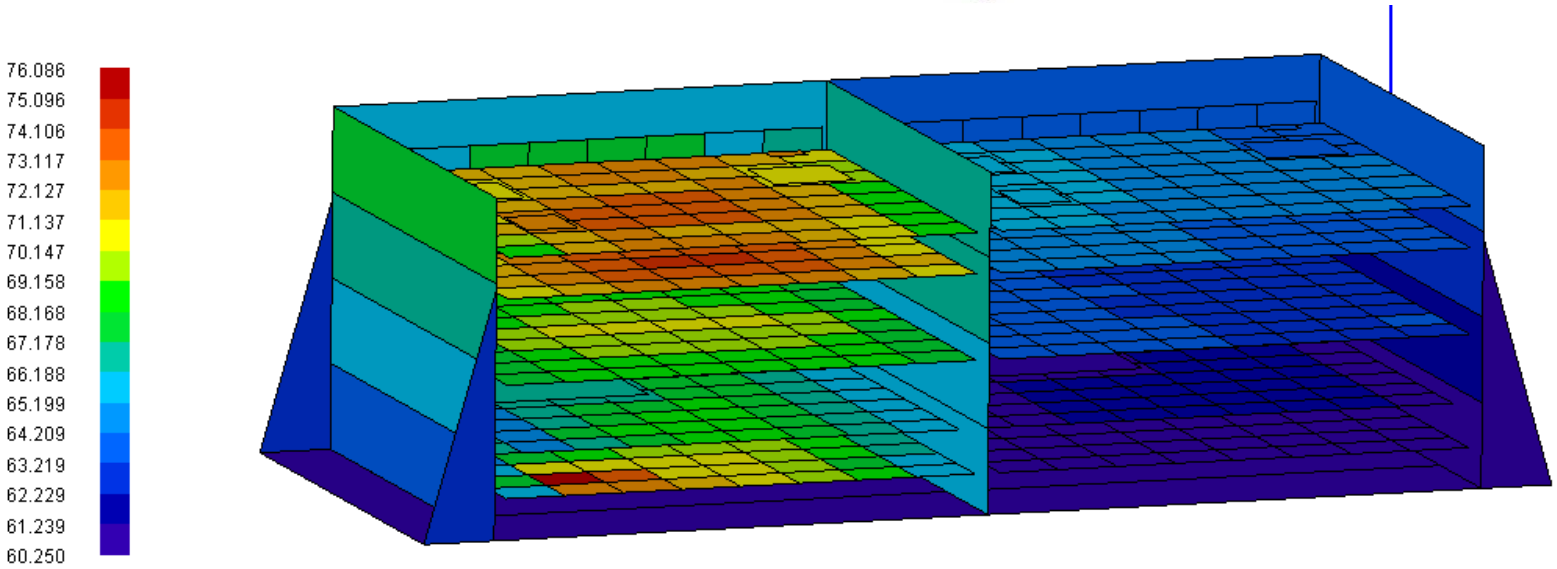
Main PCBs slide in



Connectors to other functions (power bus, sensors, actuators etc)

Horizontal card stack not precluded

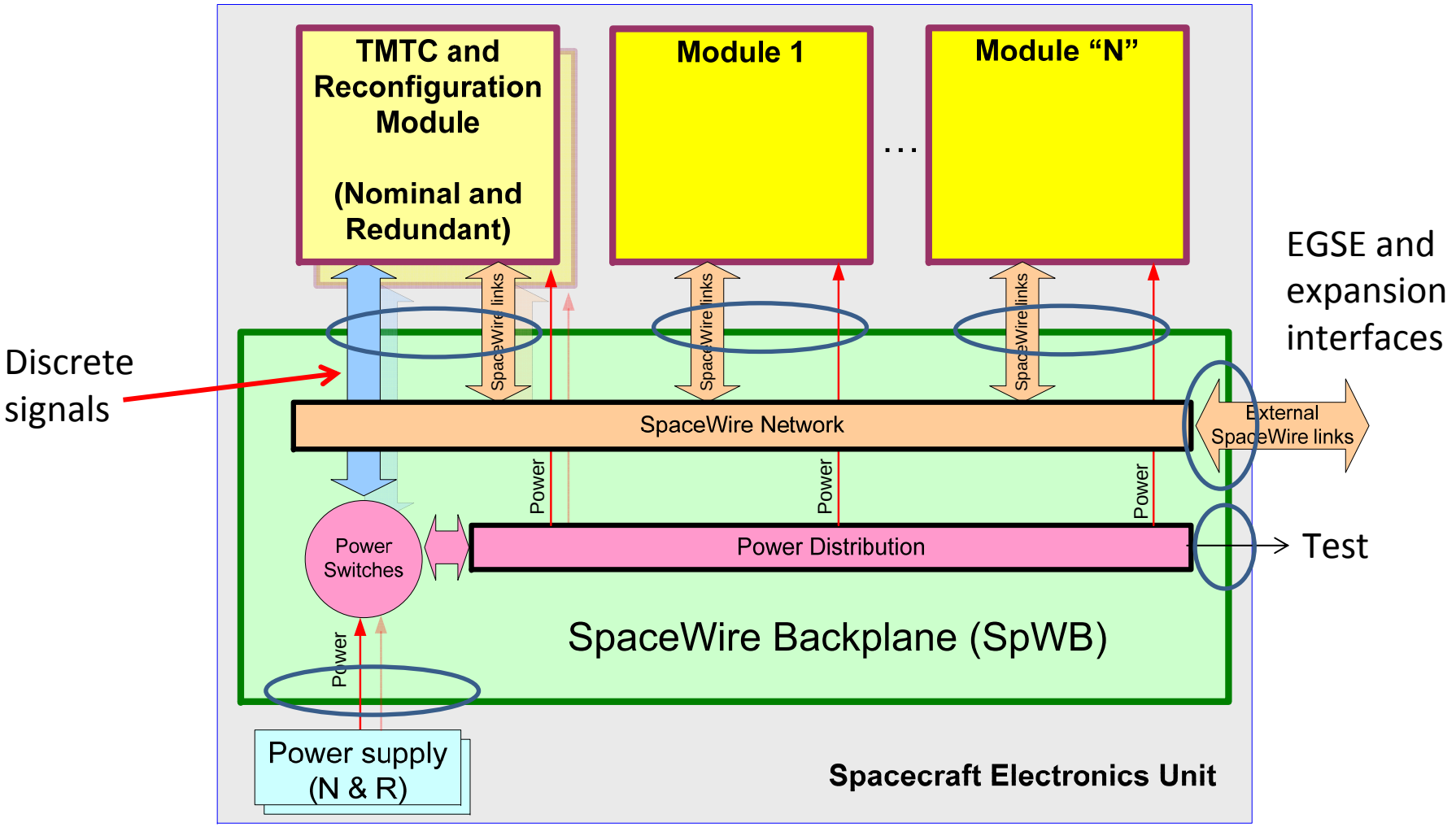




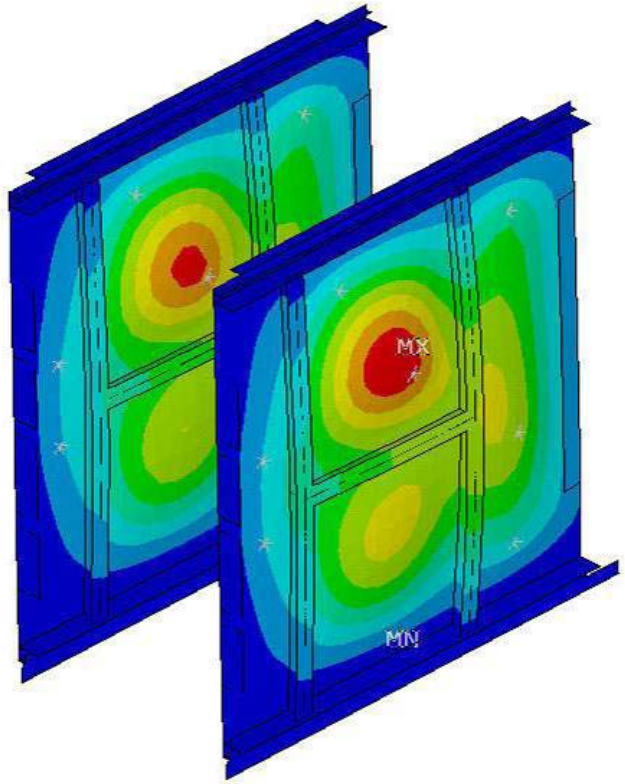
Connector characteristics

- SpW signalling rate compatible (up to 400 Mbps)
- SpFi Cu capable? (minimum 2Gbps, up to 5Gbps for FR4 PCB)
- Minimum of 2 SpW ports (4 SpFi Cu ports):
  - 8 impedance controlled (100 Ohm) differential pairs required
- Power:
  - Minimum of 2 pins, normally are paralleled up with many more grounds than +\- power rails
  - +28V and +5V minimum capability
  - At least 4 Amp rating (20 Watts at 5V)
- Signal lines:
  - Ideally avoided but... this is sometimes not practical
  - Typically single ended, clocks, synchronisation, on/off, FDIR etc.
  - 20 to 40 pins adequate?

Backplane connector interfaces - example



PCB stiffeners



232mm x 220mm PCB with
“H” stiffener

- PCBs with unsupported spans of >100mm generally require stiffeners
- The stiffening required is dependant on the component masses (user controlled)
- Stiffeners are inconvenient when large components need to be placed!
- Stiffener shown is also a thermal conduction path to the edge of the board

Fault tolerance and redundancy

- Should this be defined by the backplane specification?
  - Backplane specification appears to be driving the unit design!
- Yes, we must:
  - Prevent failure propagation from a module into the Backplane and other modules, this is a shared responsibility between Backplane and Module and hence responsibilities must be defined
  - Allow for redundancy (and allocate nominal and redundant ports)
  - Consider failure scenarios in backplane and module:
    - Failed SpW port
    - Failed power supply
    - Failed discrete signals

Task 1 – recap... and a request for your inputs!

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