SpaceWire Backplanes
– ESA ITT AO/1-6692/11/NL/LvH

17th SpaceWire Working Group, ESTEC
15/12/2011

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The need for a SpWBP specification

User needs for a SpW backplane specification:

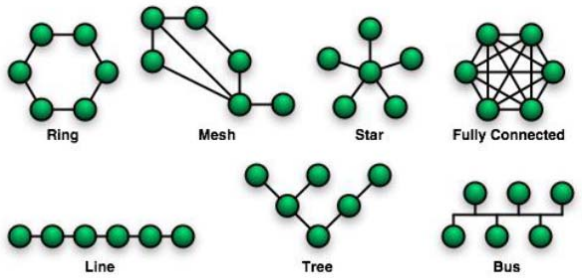
1. Reduce NRE development costs for avionics systems.
2. Satisfy use of both SpaceWire and next generation HSSL.
3. Highly reliable and scalable architecture.
4. Standardised way of implementation

Meeting these needs may be achieved by:

1. Prototyping and agree on a common denominator for the SpaceWire backplane.
2. Fund activities to aid prototyping and development of standardisation proposals.
3. Formalise a SpW Backplane standard within the ECSS framework.

SpW backplane ideas presented at earlier SpW WG

1. **SpW Backplane Specification, SEA / A.Senior,** Draft 1 B presented at 14th WG
2. **SpW Backplane connectors, routing topology and pin assignment,** Osaka University / M. Nomachi, presented at 14th WG
3. **Generic Avionic Backplane using Quadrixal Insert Connectors,** Alex Kisin, MEI Inc. & Glenn Rakow, NASA/GSFC
4. **Modular Architecture for Robust Computation (MARC),** ESA funded activity led by SEA Ltd (UK)
5. **Evaluation for the prototype SpWBP and Investigation of Standard topology for SpWBP**, Mitsubishi Electric, MELCO, Osaka University, JAXA ISAS

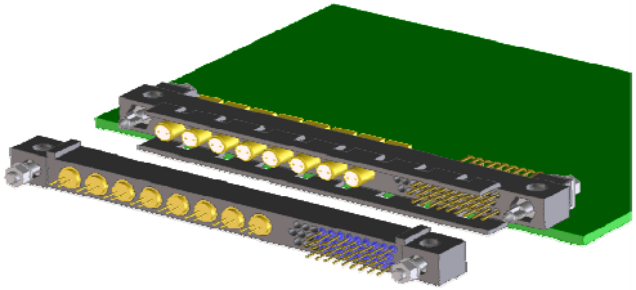


Key objectives

1. Trade off different backplane architectures and technologies to produce a SpaceWire backplane specification for **ECSS standardisation**.
2. The SpW-Backplane specification shall
    a. define a **variable/expandable number of slot/boards** for the backplane.
    b. define a number **SpaceWire interconnections and high speed serial links to co-exist on the backplane**.
    c. specify **fault tolerant power distribution**
    d. use an **appropriate number of SpW links, HSSL and discrete I/O per module**
    e. host general I/Os
    f. use a **standard backplane connector with clear path to a space qualified version**
    g. ensure good signal integrity for high speed signals up to **2.5Gbit/s and beyond**.

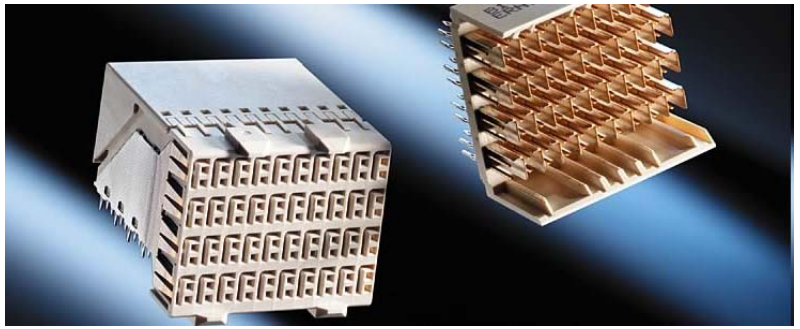
Key objectives

Identification of an matched impedance backplane connector suitable for space applications



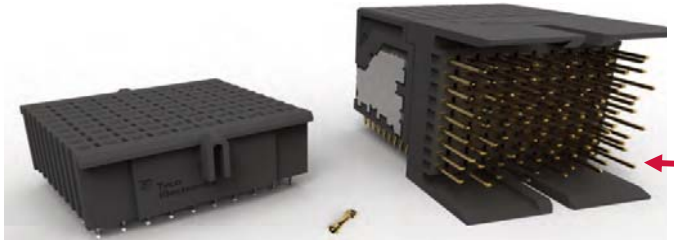
Hypertac HPH-SpW connectors

ERmet ZD®



Hard Metric Family- IEC 61076-4-101

Fortis ZD



Ruggedized

☺ Very high signal density

☺ Impedance matched differential pairs

☹ Space Qualified

Adopt Concepts from Existing Terrestrial Standards?
"Older" standards

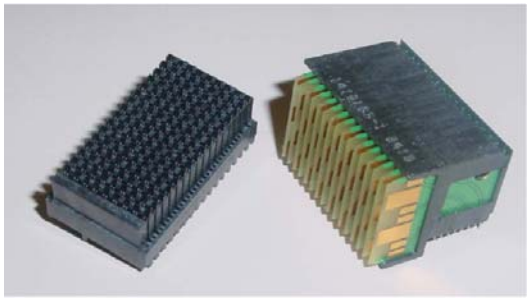
1. **PICMG 2.18 RapidIO**
    a. Defines redundant, switched, high-speed point-to-point connectivity among some or all slots using Serial RapidIO and coexisting with 64 bit CompactPCI H.110 and optionally PICMG 2.16
2. **PICMG 2.20 Serial MESH**
    a. Define a point-to-point serial interconnect intended to add high-speed cell based data transport to the PICMG 2.x platforms.

Adopt Concepts from Existing Terrestrial Standards?
"Newer" standards

1. **PICMG AdvancedTCA 3.0 R3.0**
    a. The PICMG 3.0 "core" specification will specify board, backplane and shelf mechanicals, power distribution and the connectivity required for system management.
2. **PICMG AdvancedTCA 3.4 PCI Express**
    a. Define how PCI Express and PCI Express Advanced Switching transport is mapped onto PICMG 3.0
3. **PICMG AdvancedTCA 3.5 RapidIO**
    a. Define how Serial RapidIO transport is mapped onto PICMG 3.0
4. **PICMG EXP.0 R1.0**
    a. Define the connector, electrical, and mechanical requirements of 3U/6U System Boards, Peripheral Boards, Switch Boards, and Backplanes using PCI Express as peripheral interconnect with CompactPCI interoperability features.

Adopt Concepts from Existing Terrestrial Standards?
"Newer" OPEN standards

1. **ANSI VITA 46.0 (VPx) and 46.3 PCIexpress over VPX**
    a. PCIe on VPX Fabric connector
2. **ANSI VITA 65 – OpenVPX (VITA)**
    a. Approved in June 2010
    b. Specifies a minimum set of backplane configurations
    c. Gives clear information about data rate, routing topology and fabric topology that has to be used on the backplane.



MultiGig RT-2 7-row connector

ECSS SpW Backplane draft specification
contents

Clauses suggested to be included

a. Connectors and signal configuration
   - SpW pins, user pins, reserved pins etc.

b. Module and backplane physical dimensions (form factor).

c. Power distribution

d. Routing topology
   - **Should not impose a strict passive or active backplane.**

e. Design rules in line with other ECSS quality assurance standards.

f. Test criteria
   - Mechanical and electrical


ECSS-Standard-ST-Number
ECSS Standard Issue Date

EUROPEAN COOPERATION
ECSS
FOR SPACE STANDARDIZATION

Space engineering, product assurance, management

SpaceWire backplane specification

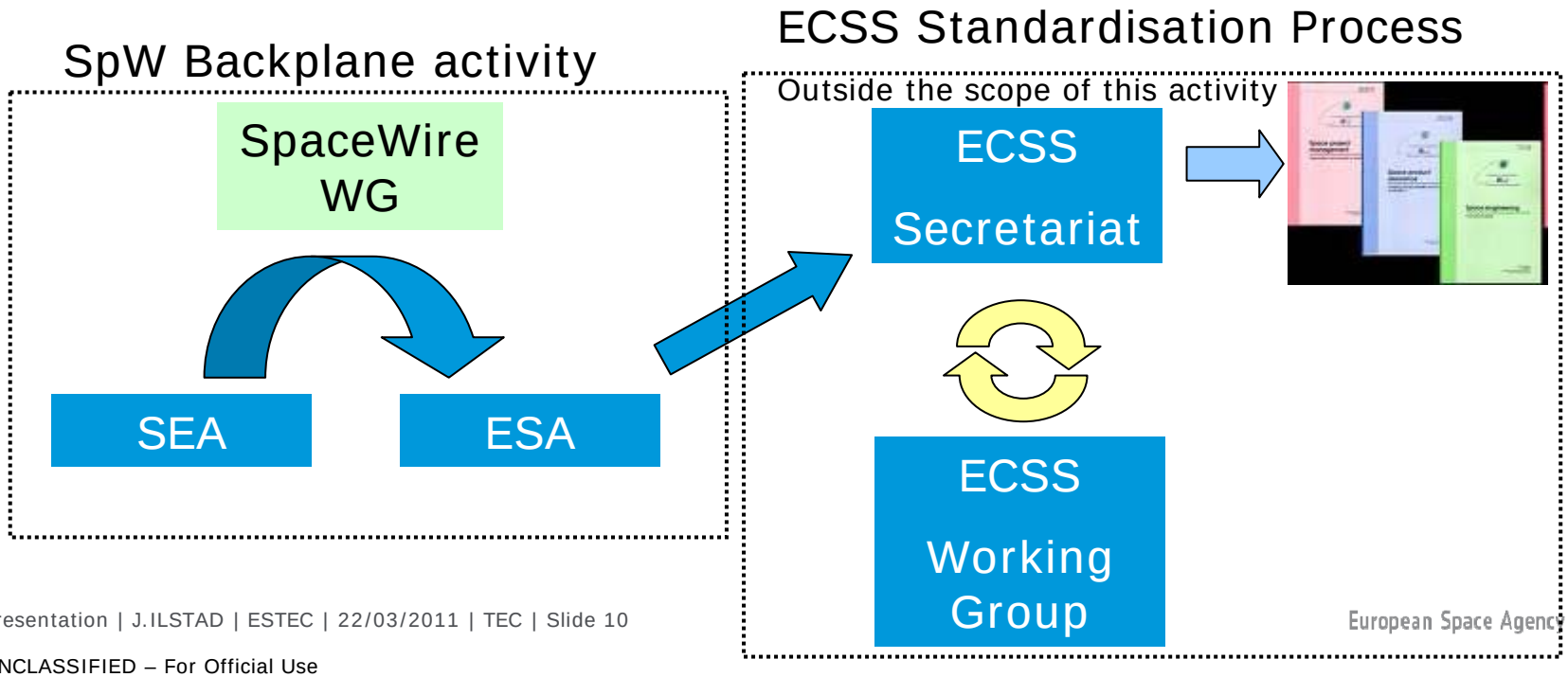
This document is a preliminary proposed ECSS draft standard to be drafted during a study before circulated for review and comments.

It is therefore subject to change without notice and may not be referred to as an ECSS Standard until published as such.

ECSS Secretariat
ESA-ESTEC
Requirements & Standards Division
Noordwijk, The Netherlands

ECSS SpW Backplane draft specification
review process

1. First draft of specification to be reviewed by members of the SpW WG
2. Time frame is foreseen between two WG meetings
3. Inputs from SpW WG should raise the maturity level
4. Goal is to define a draft specification which shall be used as baseline for a ECSS standard.



Test Connector and Test Board manufacturing

Parameters to be verified:

Impedance for single ended and differential lines

Cross-Talk

Propagation Delay / Skew

S-parameter

Eye Diagram

Current status

Contract awarded to SEA Ltd

- Hypertac Ltd subcontractor for connector prototypes

The project is divided in 5 main tasks

1. System analysis and requirements capture
2. Survey of state of the art
3. Drafting of SpWBP ECSS specification
4. SpWBP connector design, manufacturing and test
5. Activity synthesis and final presentation

Current Status

Activity kick-off: September 2011

Task 1 & 2 in progress, to be completed mid Q1 2012.

More information to be given in the following presentation by SEA

Thank you!