


SpaceWire Backplanes: Feedback from a User

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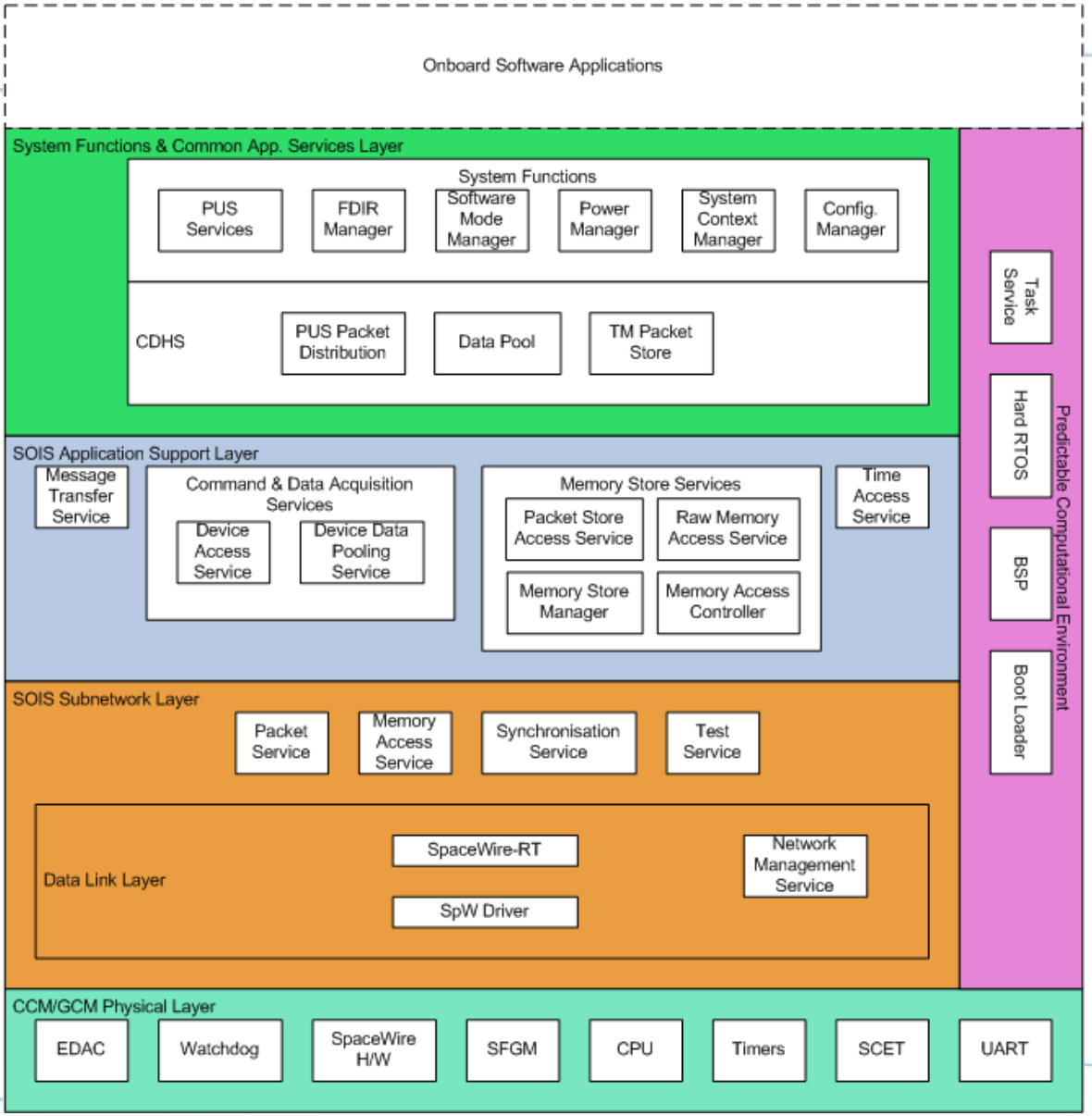
GenFAS for MARC

- Generic Fault-tolerant Architecture using SOIS
- SOIS-compliant complete onboard-software execution platform
  - I/O
  - Standardised data handling (PUS-based)
  - System and context management
  - FDIR
- Implements all SOIS QoS classes
  - Timeslotted RMAP, PS and SpaceWire-RT
- Connected to bespoke EGSE tool
  - Debugging, system control, module emulation etc.

GenFAS Architecture



scisys

SpaceWire Technologies in GenFAS

- SOIS-Compliance
- Channel-oriented
- Time-slotted
- Packet Service
- Memory Access Service (RMAP)
- SpaceWire-RT
- Segmentation
- Acknowledgements and retries (reliability)
- Time handling
- Limited SpaceWire-PnP (SpW-10X compatibility)

- Uses SpW-10X, UoD RMAP IP Core

Using the MARC Backplane

- Topology was logical
- Failover modes were easy to design
- Active backplane easy to work with
  - Functioned independently of modules
- Common RMAP address space permitted basic network discovery

- Debugging was more tricky
- Wrote a packet sniffer
- Need an extender card for a link analyser
- Debugging should be considered as part of backplane specification

Other Comments

- Configuration and power controller is a single point of failure
  - Is also time-code master and master SCET with similar problems
  - Not clear what architecture is the best to replace this
- Signals giving module “location” were not that useful
  - Only used on processor modules and could have been worked around
  - Are these a waste of pins?