



SpaceWire Backplanes: Feedback from a User

Peter Mendham

24 March 2011

GenFAS for MARC

- > Generic Fault-tolerant Architecture using SOIS
- SOIS-compliant complete onboard-software execution platform
 - > I/O
 - > Standardised data handling (PUS-based)
 - > System and context management
 - > FDIR
- > Implements all SOIS QoS classes
 - > Timeslotted RMAP, PS and SpaceWire-RT
- > Connected to bespoke EGSE tool
 - > Debugging, system control, module emulation etc.



GenFAS Architecture

Onboard Software Applications System Functions & Common App. Services Layer System Functions Software System PUS FDIR Power Config. Mode Context Manager Services Manager Manager Manager Manager Task Service PUS Packet TM Packet CDHS Data Pool Distribution Store Hard RTOS Predictable SOIS Application Support Layer Message Time Command & Data Acquisition Memory Store Services Transfer Access Services Computationa Service Packet Store Service Raw Memory Device Device Data Access Service Access Service Pooling Access BSP Service Service Memory Store Memory Access Manager Controller Ш ronment Boot Loader SOIS Subnetwork Layer Memory Packet Synchronisation Test Access Service Service Service Service Network SpaceWire-RT Management Data Link Layer Service SpW Driver CCM/GCM Physical Layer SpaceWire SFGM CPU SCET UART EDAC Watchdog Timers H/W

3 SpaceWire Backplanes

SpaceWire Technologies in GenFAS

- > SOIS-Compliance
- > Channel-oriented
- > Time-slotted
- > Packet Service
- > Memory Access Service (RMAP)
- > SpaceWire-RT
- > Segmentation
- > Acknowledgements and retries (reliability)
- > Time handling
- > Limited SpaceWire-PnP (SpW-10X compatibility)
- > Uses SpW-10X, UoD RMAP IP Core

Using the MARC Backplane

- > Topology was logical
- > Failover modes were easy to design
- > Active backplane easy to work with
 - > Functioned independently of modules
- > Common RMAP address space permitted basic network discovery
- > Debugging was more tricky
- > Wrote a packet sniffer
- > Need an extender card for a link analyser
- Debugging should be considered as part of backplane specification

Other Comments

- Configuration and power controller is a single point of failure
 - > Is also time-code master and master SCET with similar problems
 - > Not clear what architecture is the best to replace this
- > Signals giving module "location" were not that useful
 - > Only used on processor modules and could have been worked around
 - > Are these a waste of pins?

