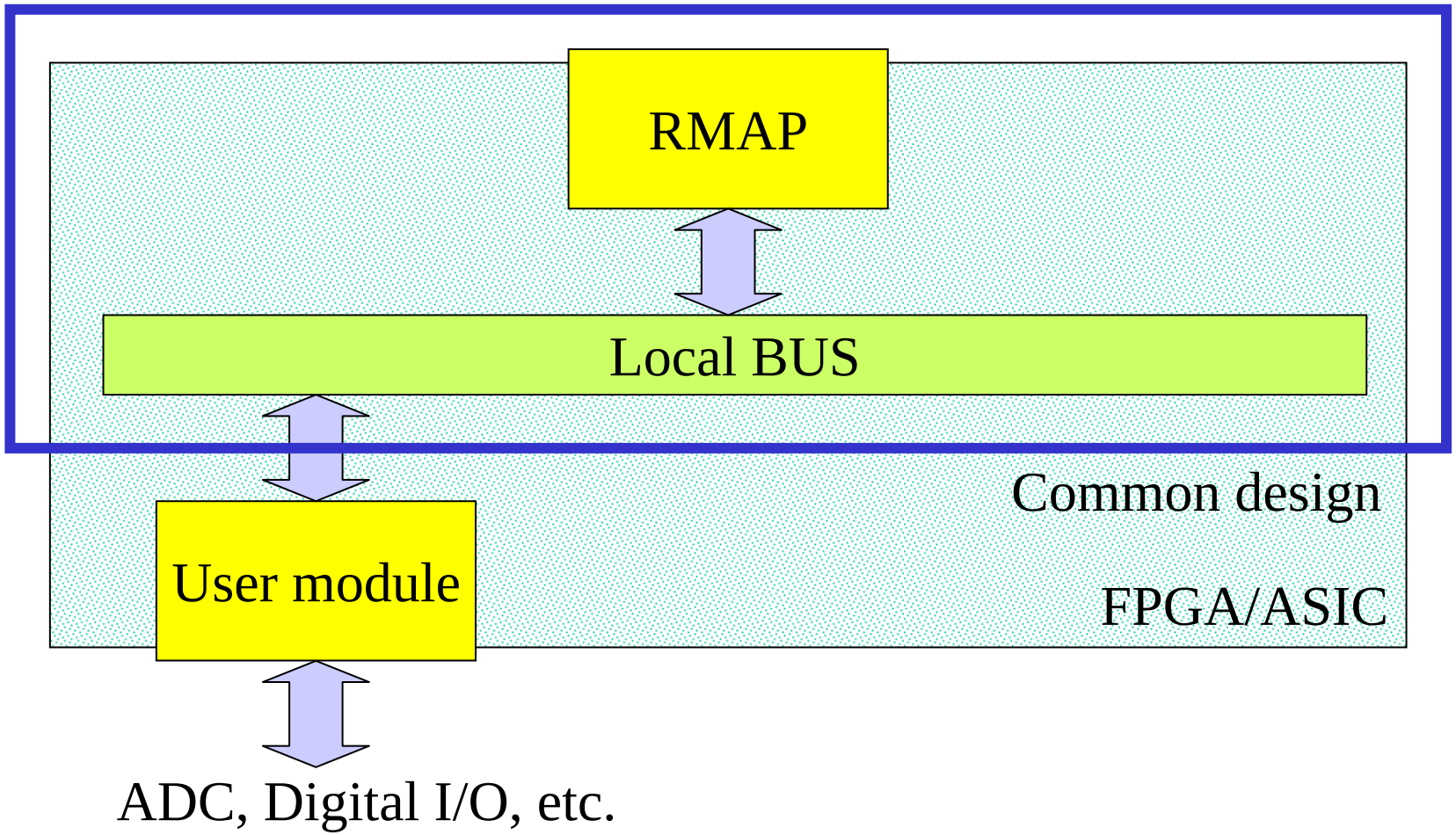
Prototyping with SpW in Japan

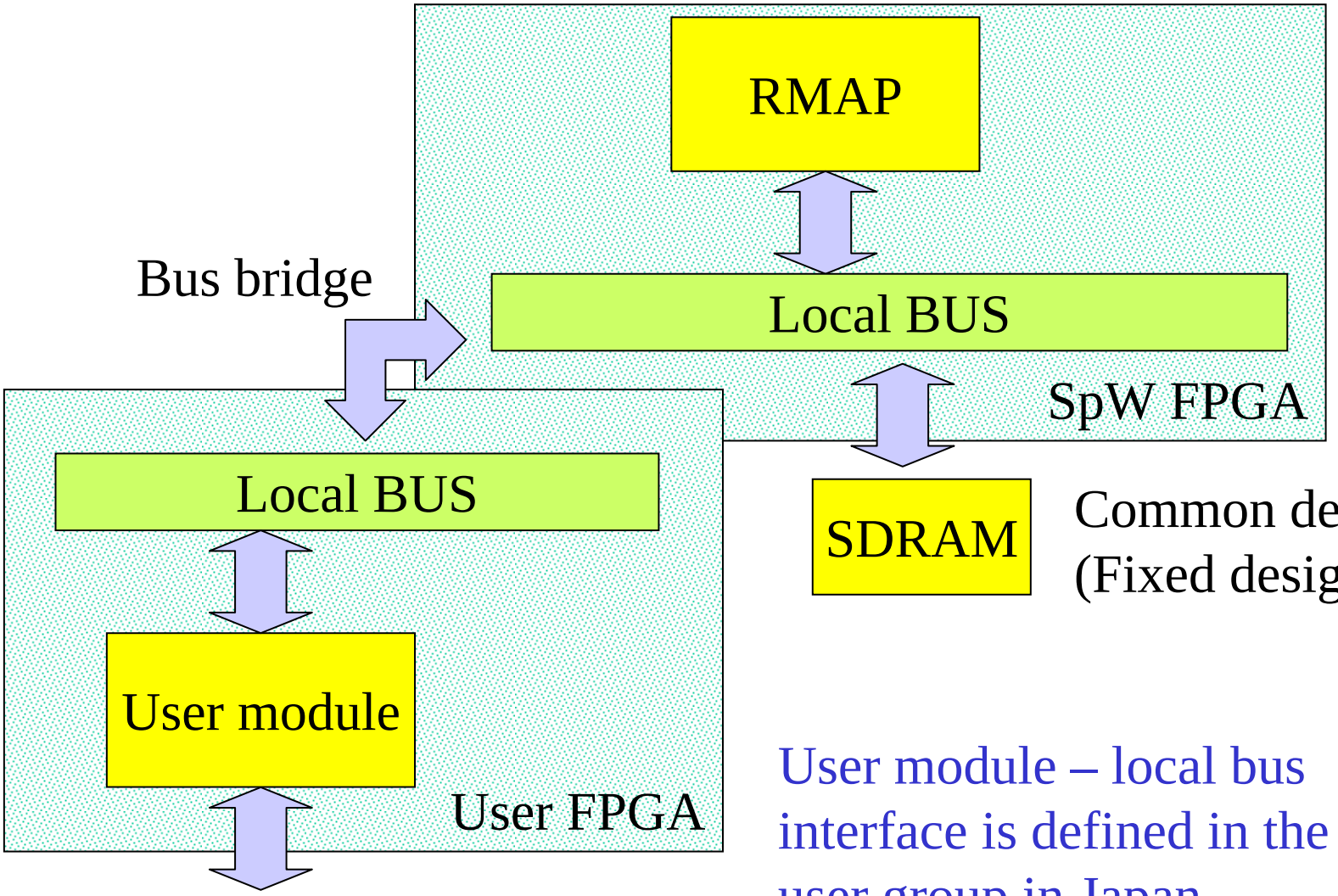
Osaka University/JAXA

M. Nomachi

Front-end module

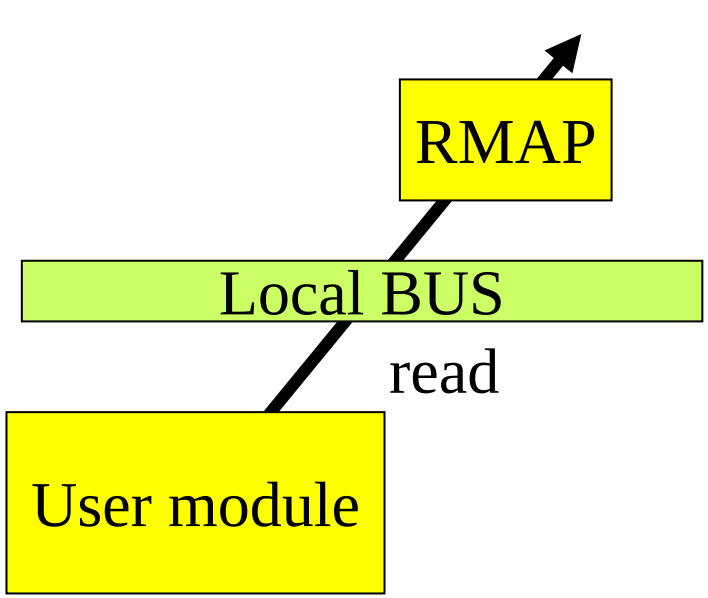


Front-end module prototype

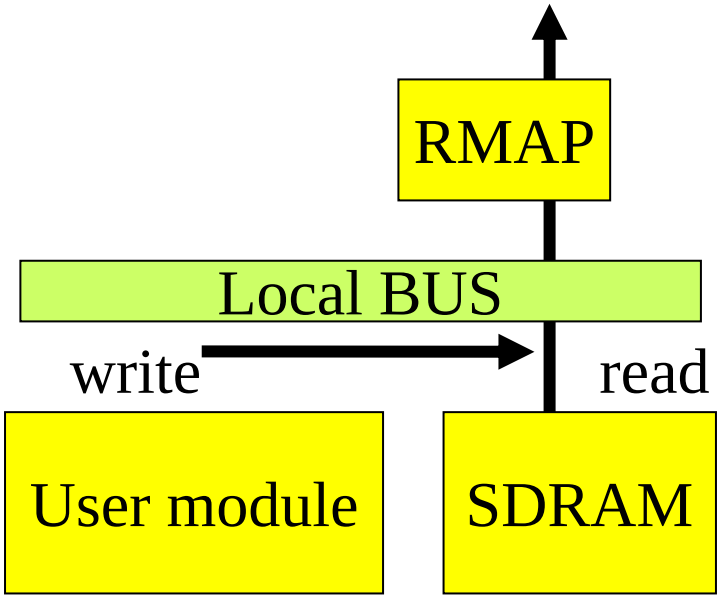


User module – local bus interface is defined in the user group in Japan.
Bus bridge is also defined.

Data collection



Simple BUS



Collect data fragments

BUS with arbitration is defined

SpW ADC/DAC BOARD

SHIMAFUJI

ADC/DAC Board specified for Space Wire

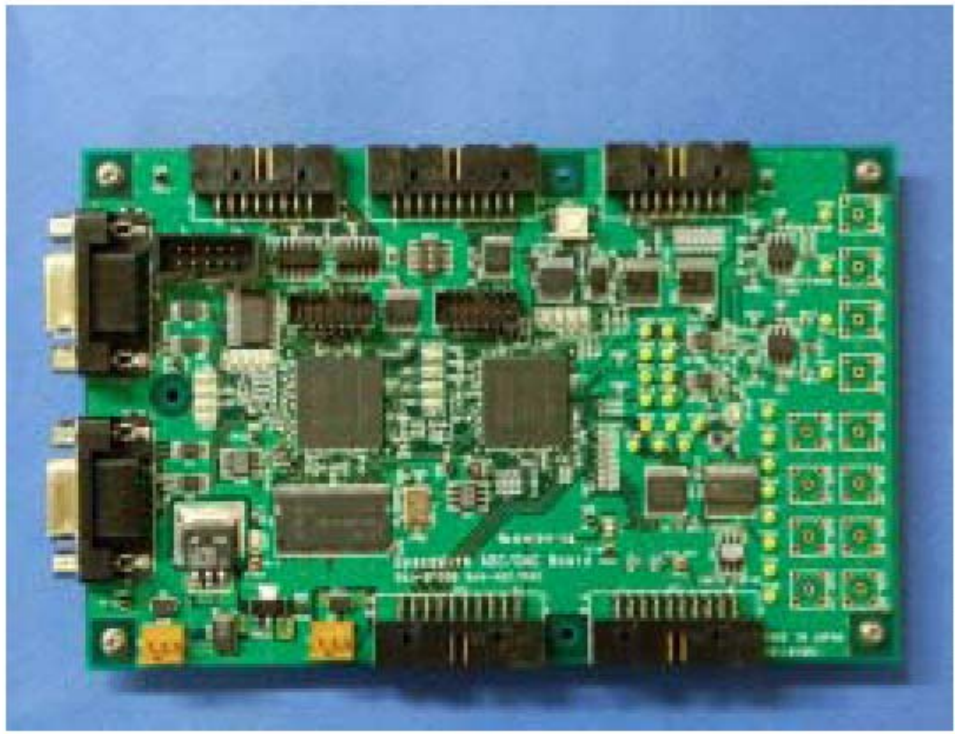
Connected to SpaceCube

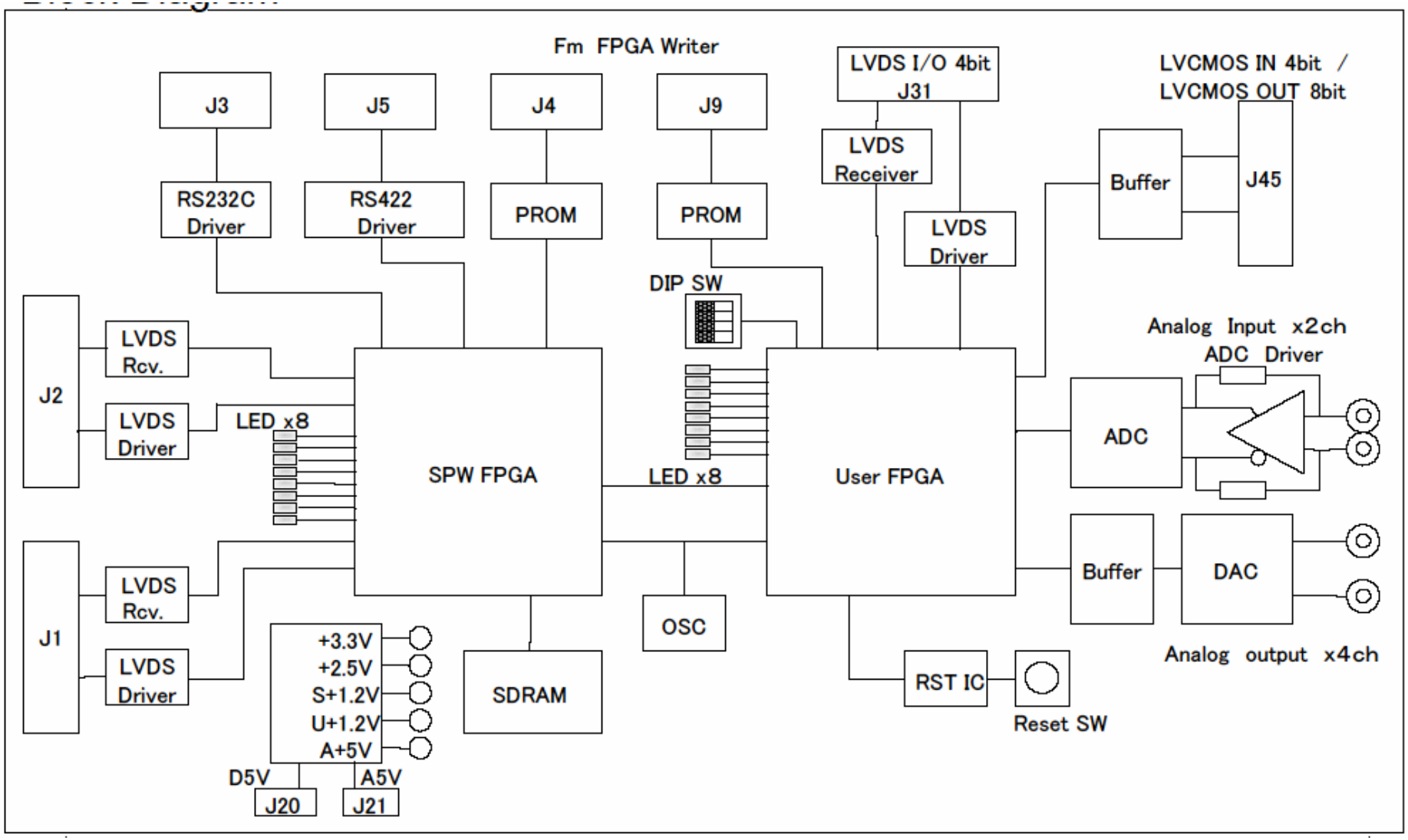
Includes user FPGA and SDRAM and as external I/O , LVDS input/output , LVCMOS input/output , serial I/F , AD converter and DA converter.

Joint development with JAXA（Japan Aerospace Exploration Agency)

Specification Table

ITEMS	SPECIFICATIONS
SpW I/F	2ch installed in FPGA
External I/F	Pararrel : LVCMOS IN 4bit OUT 8bit LVDS IN 4bit OUT 4bit Serial : RS232C 1ch RS422 1ch ADC : AD7688BRM Input : 2ch , Resolution : 16bit Sample Rate : 500 KSPS DAC : AD5544 ARS Resolution : 16bit, Error : ±1LSB Output voltage/Current range : 0～4.0V/2.5～1.5mA
Others	SDRAM : x8bit 16MB User logic : FPGA




Fm FPGA Writer
J3
J5
J4
J9
LVDS I/O 4bit
J31
LVCMOS IN 4bit /
LVCMOS OUT 8bit
RS232C
Driver
RS422
Driver
PROM
PROM
LVDS
Receiver
LVDS
Driver
Buffer
J45
DIP SW
J2
LVDS
Rcv.
LVDS
Driver
LED x8
SPW FPGA
LED x8
User FPGA
Analog Input x2ch
ADC Driver
ADC
J1
LVDS
Rcv.
LVDS
Driver
+3.3V
+2.5V
S+1.2V
U+1.2V
A+5V
D5V
A5V
J20
J21
SDRAM
OSC
Buffer
DAC
Analog output x4ch
RST IC
Reset SW

SpW Digital I/O BOARD

SHIMAFUJI

Digital I/O Board specified for Space Wire

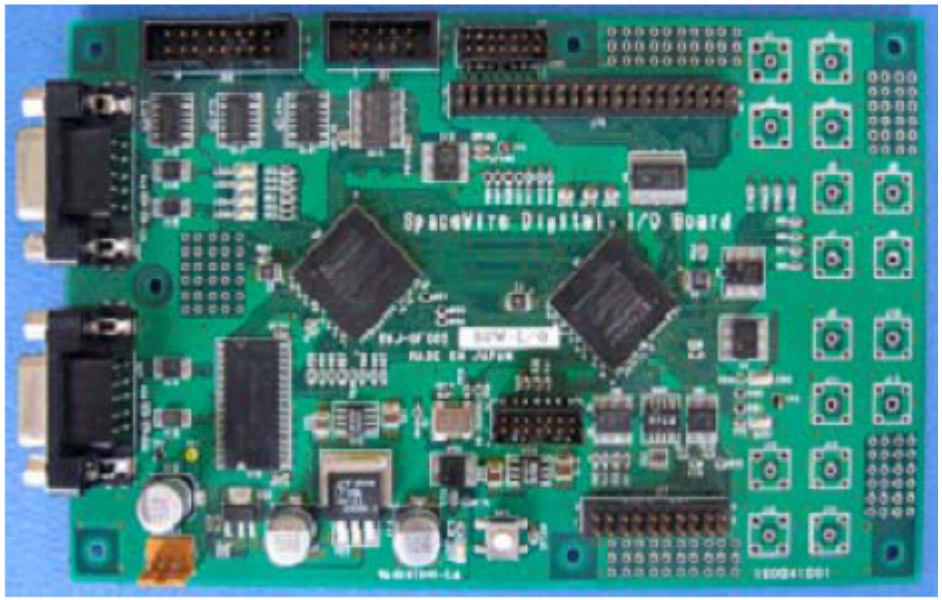
Connected to Space Cube

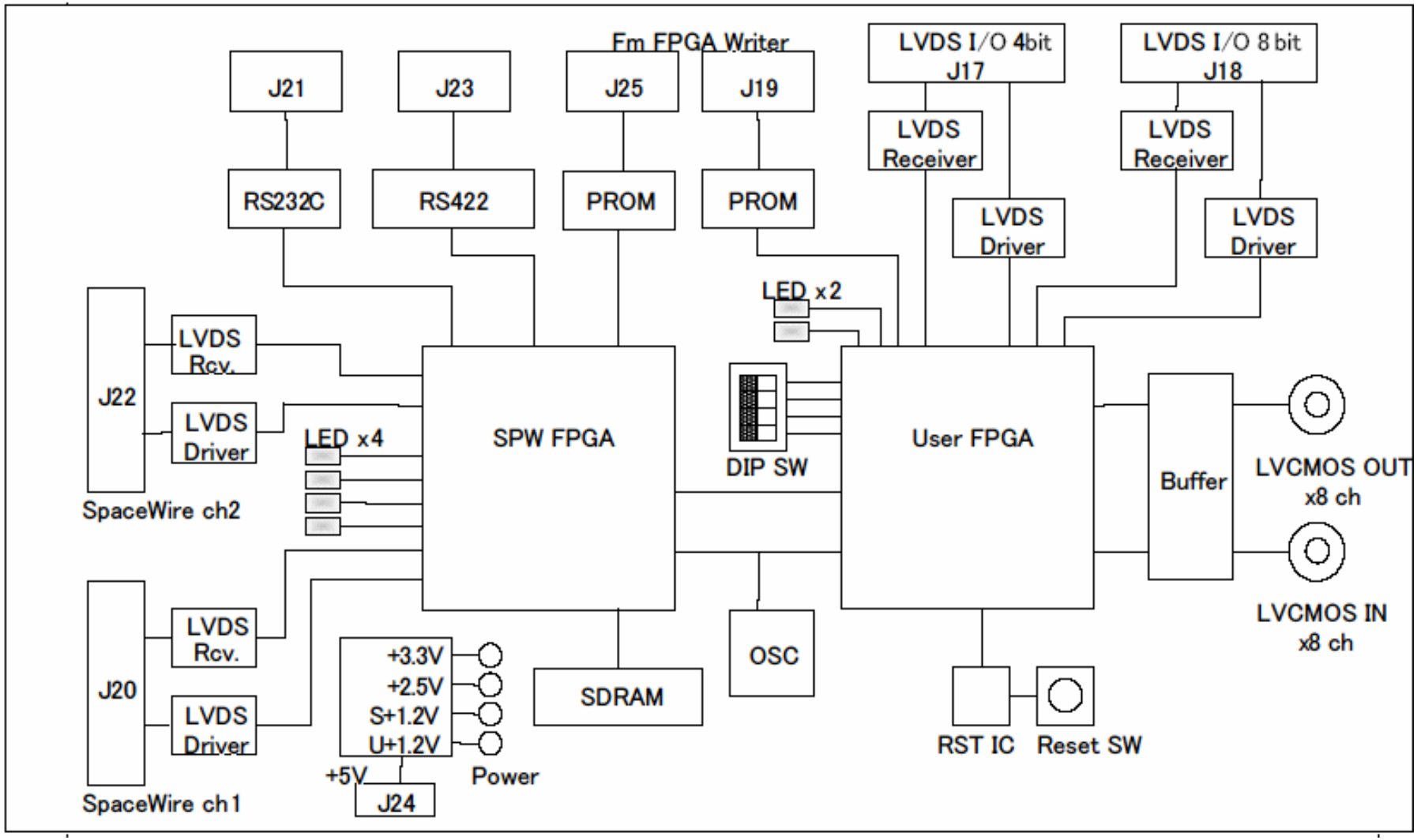
Includes user FPGA and SDRAM and as external I/O , LVDS input/output , LVCMOS input/output and serial I/F

Joint Development with JAXA (Japan Aerospace Exploration Agency)

Specification Table

ITEMS	SPECIFICATIONS
SpW I/F	2ch are installed in the FPGA
External I/F	Pararrel: LVCMOS IN 8bit LVCMOS OUT 8bit LVDS IN 12bit LVDS OUT 12bit Serial: RS232C 1ch RS422 1ch
Others	SDRAM: 16Mbyte User logic: FPGA




Fm FPGA Writer
J21
J23
J25
J19
LVDS I/O 4bit
J17
LVDS I/O 8 bit
J18
LVDS
Receiver
LVDS
Receiver
RS232C
RS422
PROM
PROM
LVDS
Driver
LVDS
Driver
LED x2
J22
LVDS
Rcv.
LVDS
Driver
LED x4
SPW FPGA
DIP SW
User FPGA
Buffer
LVCMOS OUT
x8 ch
SpaceWire ch2
LVCMOS IN
x8 ch
J20
LVDS
Rcv.
LVDS
Driver
+3.3V
+2.5V
S+1.2V
U+1.2V
+5V
J24
Power
SDRAM
OSC
RST IC
Reset SW
SpaceWire ch1

FADC BOARD High Reso.

SHIMAFUJI

Flash ADC Board specified for Space Wire

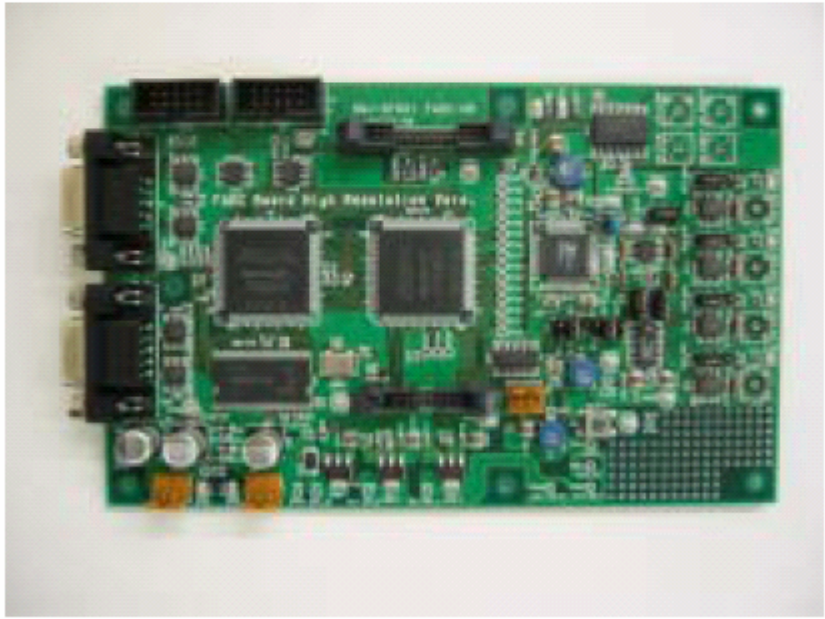
Connected to Space Cube

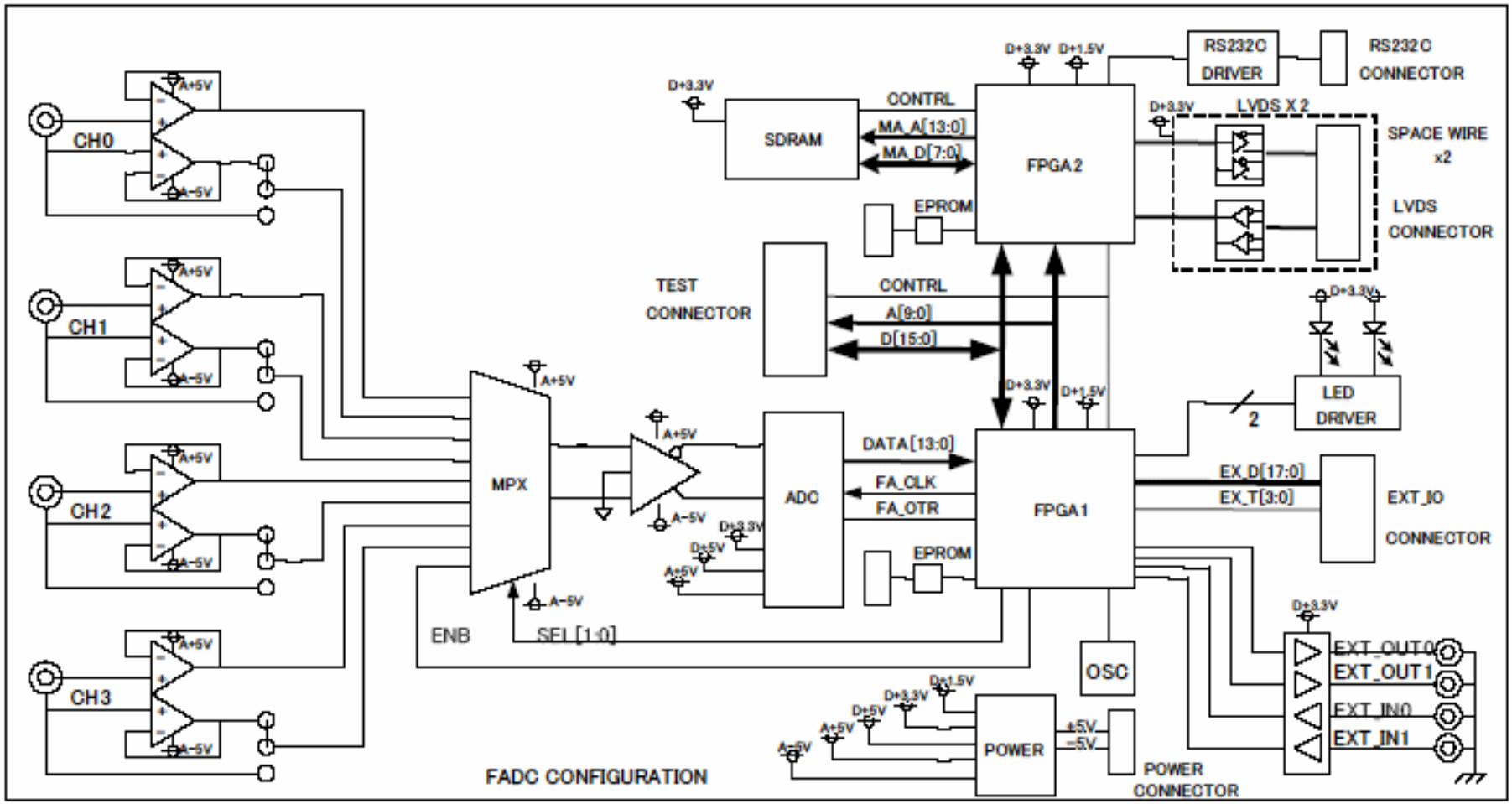
Analog input x 4ch、external I/O 26 bit

Joint development with JAXA（Japan Aerospace Exploration Agency）

Specification Table

ITEMS	SPECIFICATIONS
Space Wire	Installed in FPGA
Analog Input	ADC:AD9240AS Resolution:14bit Conversion speed:100ns
External I/O	Directly connected to FPGA:22bit (IN/OUT) Output via buffer:2bit Input via buffer:2bit
Monitor Function	Connectors for testing：Address×10bit Data×16bit Serial：RS232C（Only Transmission data）




CH0
CH1
CH2
CH3
A+5V
A-5V
MPX
ENB
SEL[1:0]
ADC
DATA[13:0]
FA_CLK
FA_OTR
SDRAM
CONTRL
MA_A[13:0]
MA_D[7:0]
EPROM
FPGA2
FPGA1
TEST
CONNECTOR
CONTRL
A[9:0]
D[15:0]
D+3.3V
D+1.5V
RS232C
DRIVER
RS232C
CONNECTOR
LVDS X 2
SPACE WIRE
x2
LVDS
CONNECTOR
LED
DRIVER
2
EX_D[17:0]
EX_T[3:0]
EXT_IO
CONNECTOR
EXT_OUT0
EXT_OUT1
EXT_IN0
EXT_IN1
OSC
POWER
+5V
-5V
POWER
CONNECTOR
FADC CONFIGURATION

VATA-FADC Attachment

SHIMAFUJI

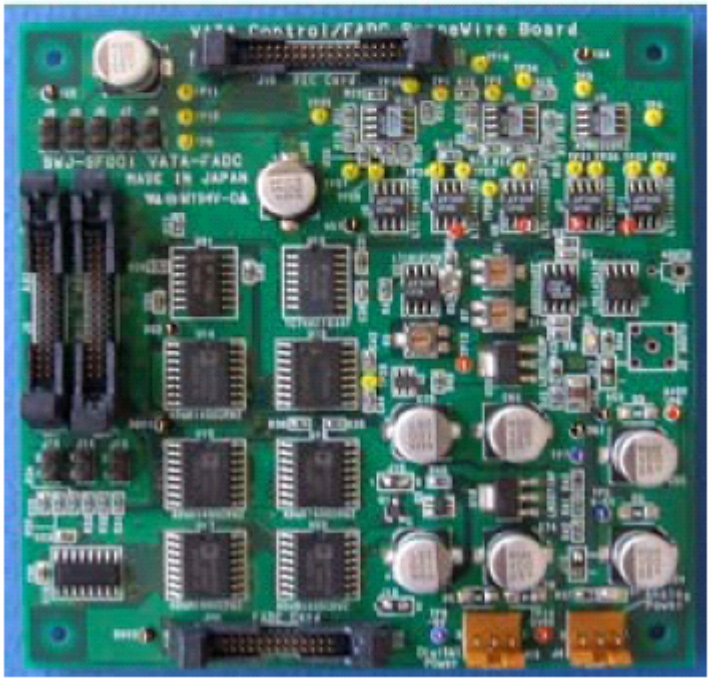
Used with connection to FADC Board High Reso.

Analog outputx6ch, Analog inputx1ch and external I/O 12 bit

Joint development with JAXA (Japan Aerospace Exploration Agency)

Specification Table

ITEMS	SPECIFICATIONS
Analog Output	Triple wires' serial DAC : LTC1446IS8 Resolution : 12bit DNL errors at Maximum : 0.5 LSB Conversion : 80ns 8bit pararrel DAC : CA33338AMZ DNL error at maximum : 1.0LSB Conversion speed : 20ns
External I/O	LVDS output : 4bit Isolation output : 7bit Input : 1bit



SpW Sampling ADC BOARD

SHIMAFUJI

Sampling ADC Board specified for Space Wire

Connected to Space Cube

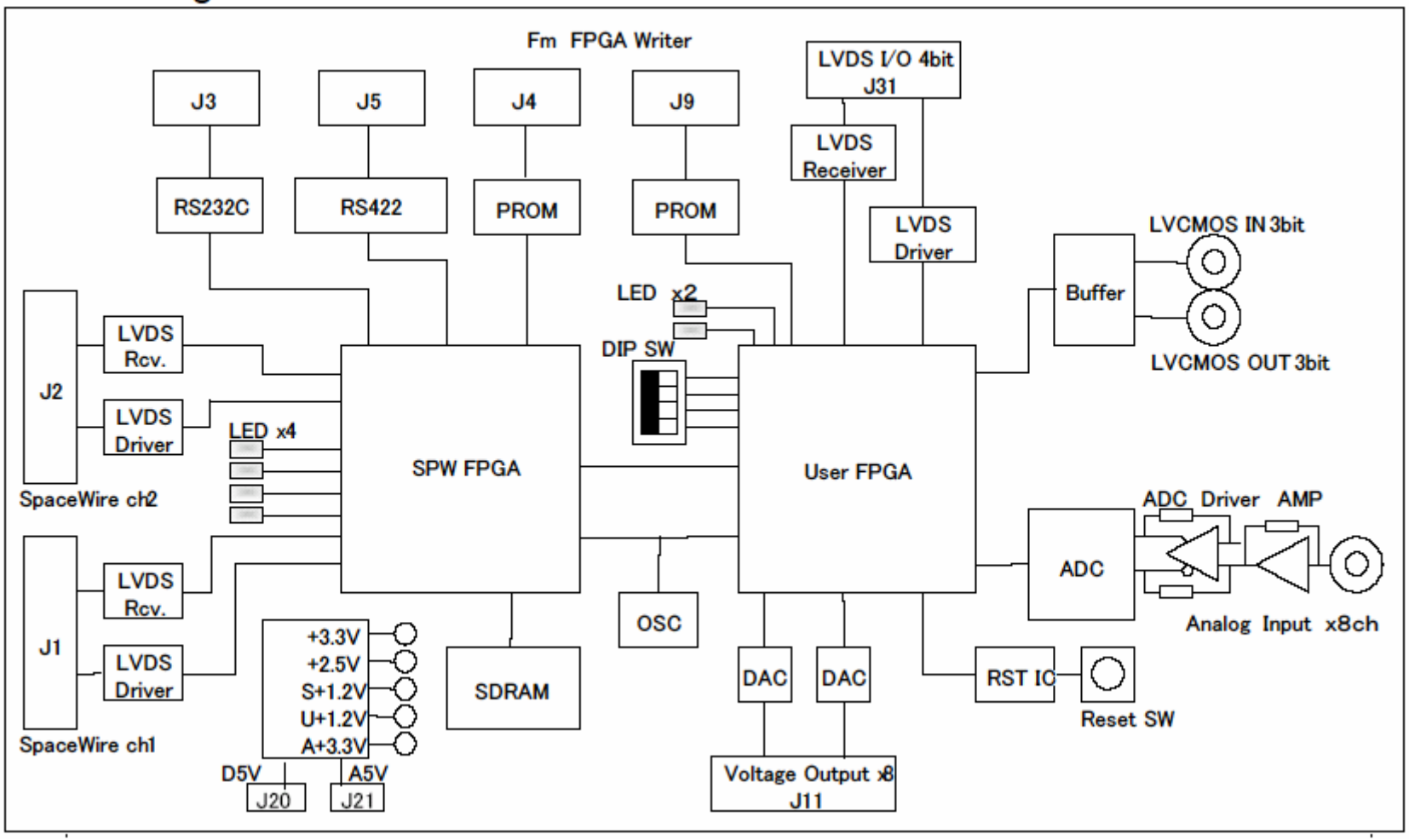
Includes user FPGA and SDRAM and as external I/O , LVDS input/output , LVCMOS input/output , serial I/F and AD Converter

Joint Development with JAXA(Japan Aerospace Exploration Agency)

Specification Table

ITEMS	SPECIFICATIONS
SpW I/F	2ch are installed in the FPGA
External I/F	Pararrel : LVCMOS IN/OUT 3bit LVDS IN/OUT 4bitt Serial : RS232C 1ch RS422 1ch ADC : ADS5721IPFP Input : 8ch, Resolution : 12bit Sample Rate : 50MSPS DAC : AD5324ARM Resolution : 12bit, Error : ±4LSB OutputVoltage range : 2.5～5.5v/200μA
Others	SDRAM : 16Mbyte User logic : FPGA

Block Diagram

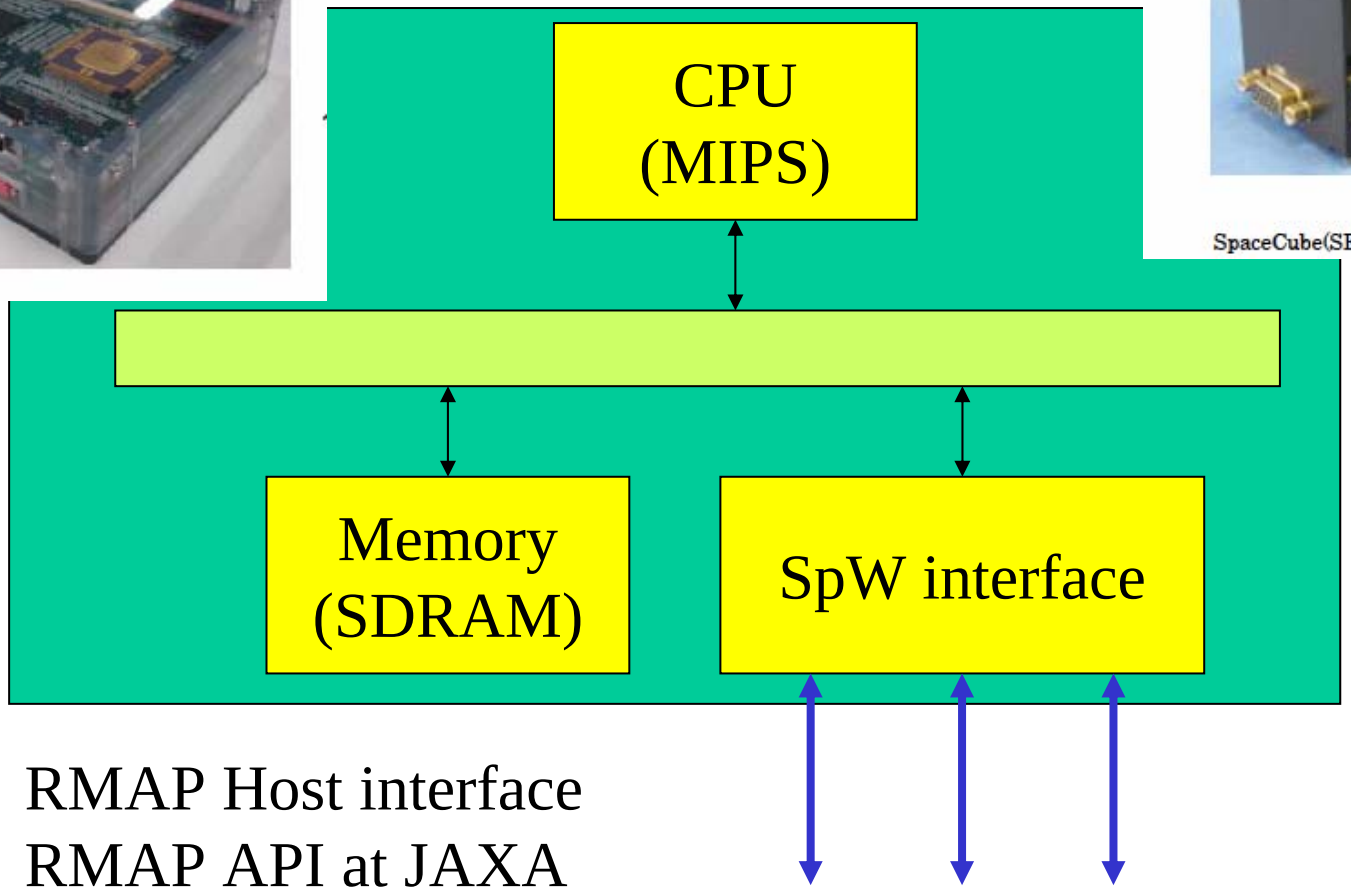


SHIMAFUJI Electric Inc. 〒144-0051 KC Bldg. 5F, 8-1-15, Nishikamata, Ota-ku,Tokyo, Japan

TEL：03-3733-8308 FAX：03-3733-8318 E-mail：info@shimafuji.co.jp URL：http://www.shimafuji.co.jp/

RMAP master
(Space Cube and Space Cube II)

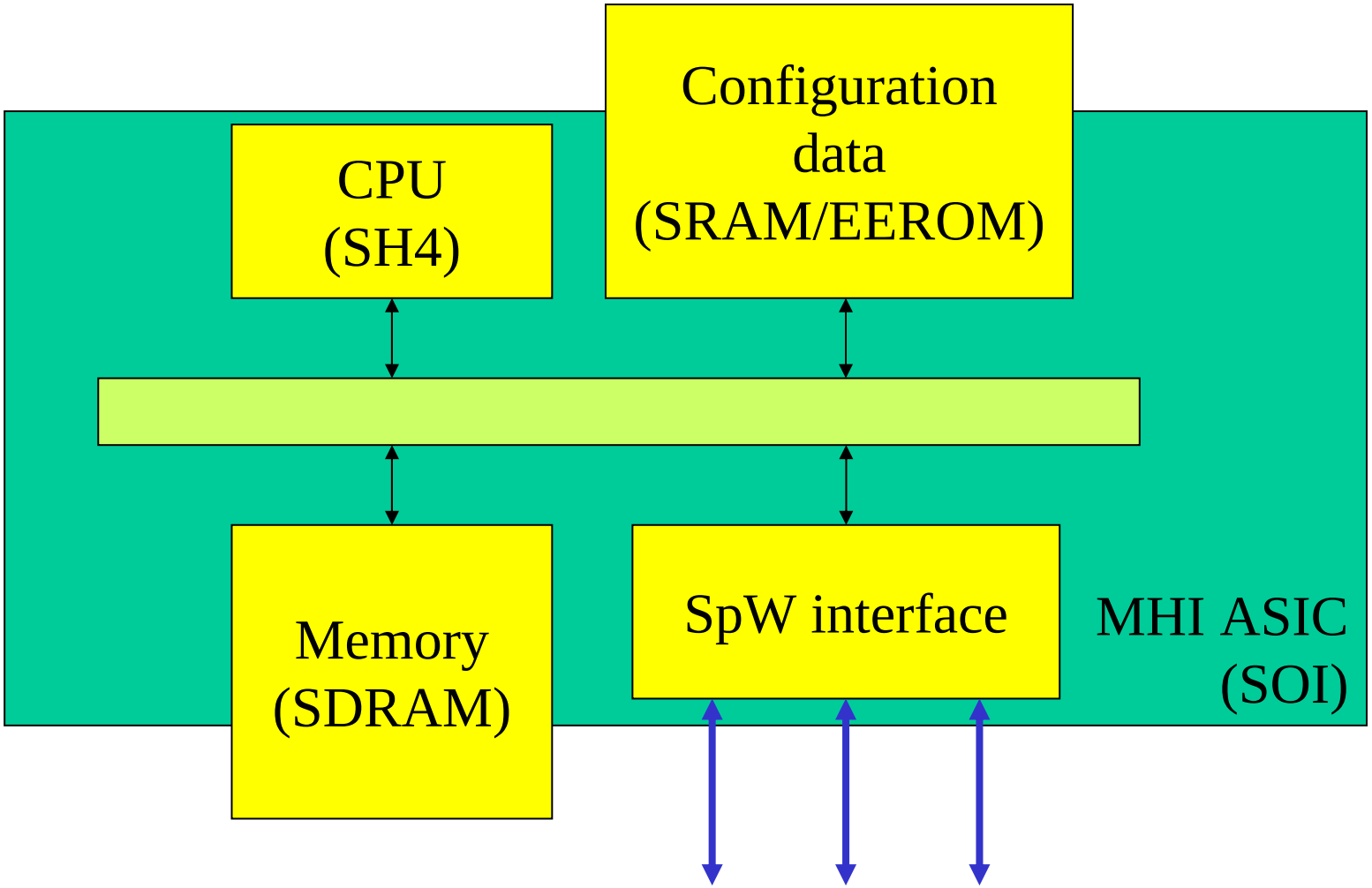
SpaceCube(SEMC5701B)



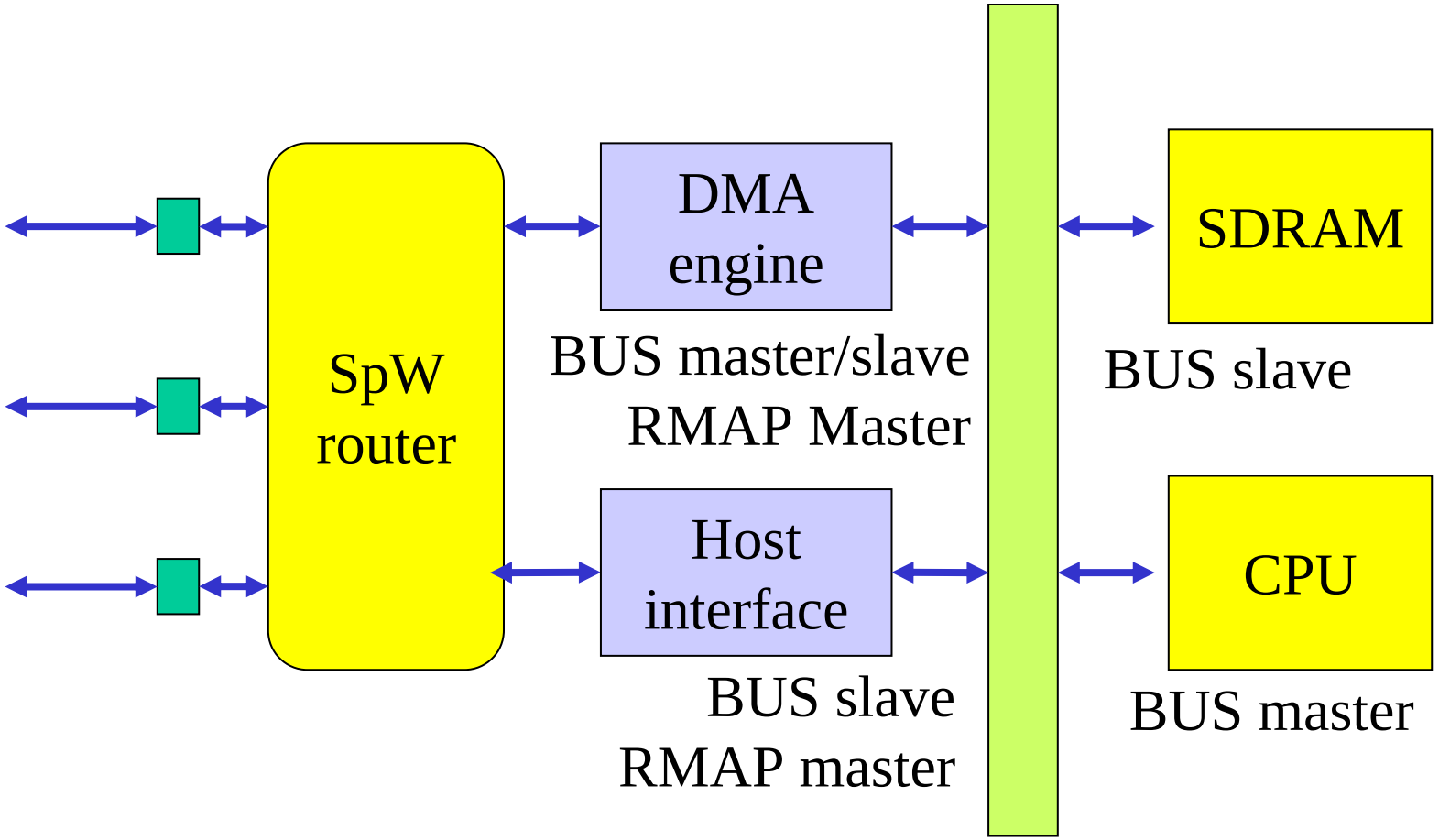
RMAP Host interface
RMAP API at JAXA

Do we have standard?

RMAP master
(Data processing Unit)



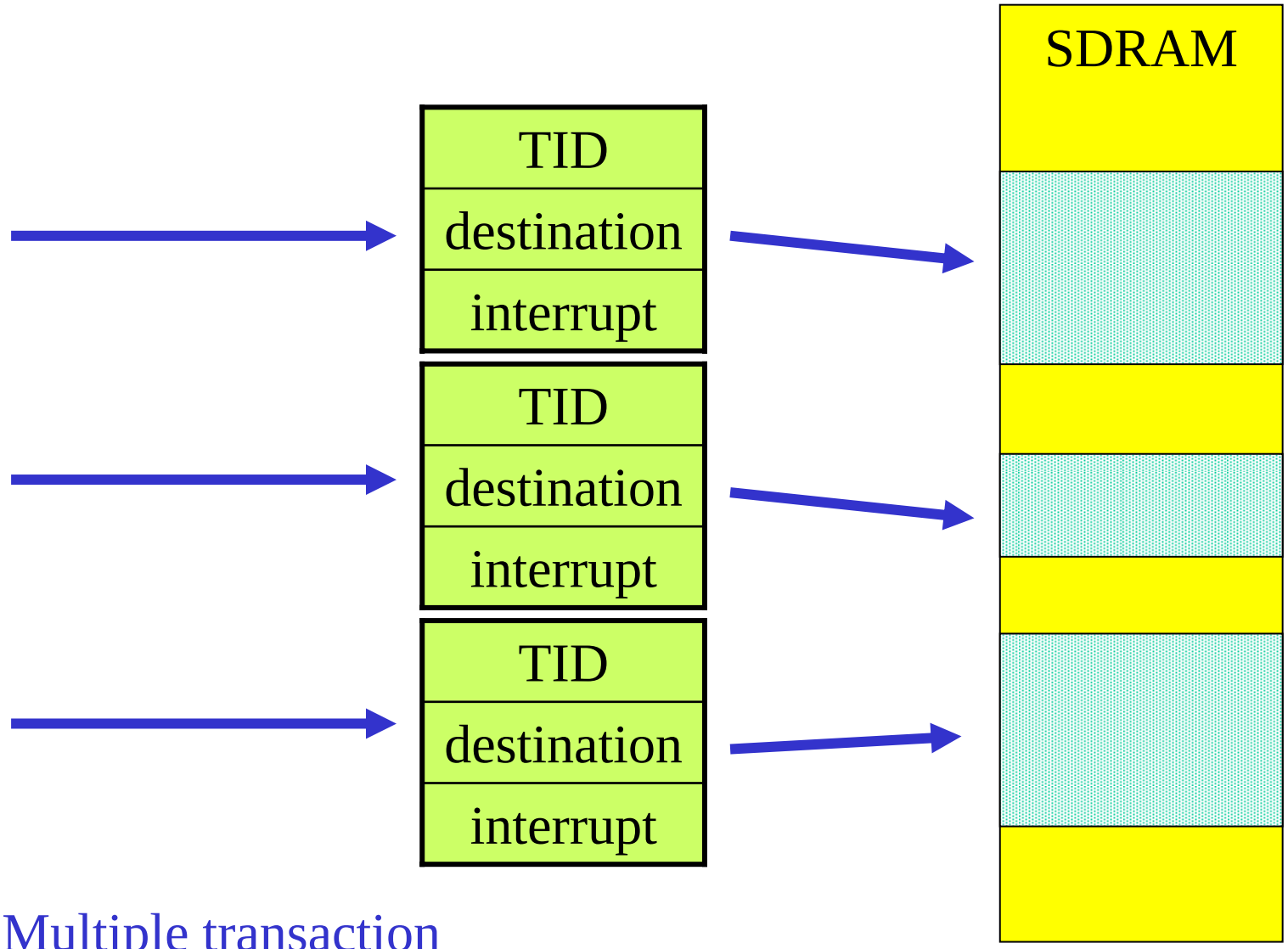
DMA transfer



Will be implemented in MHI ASIC

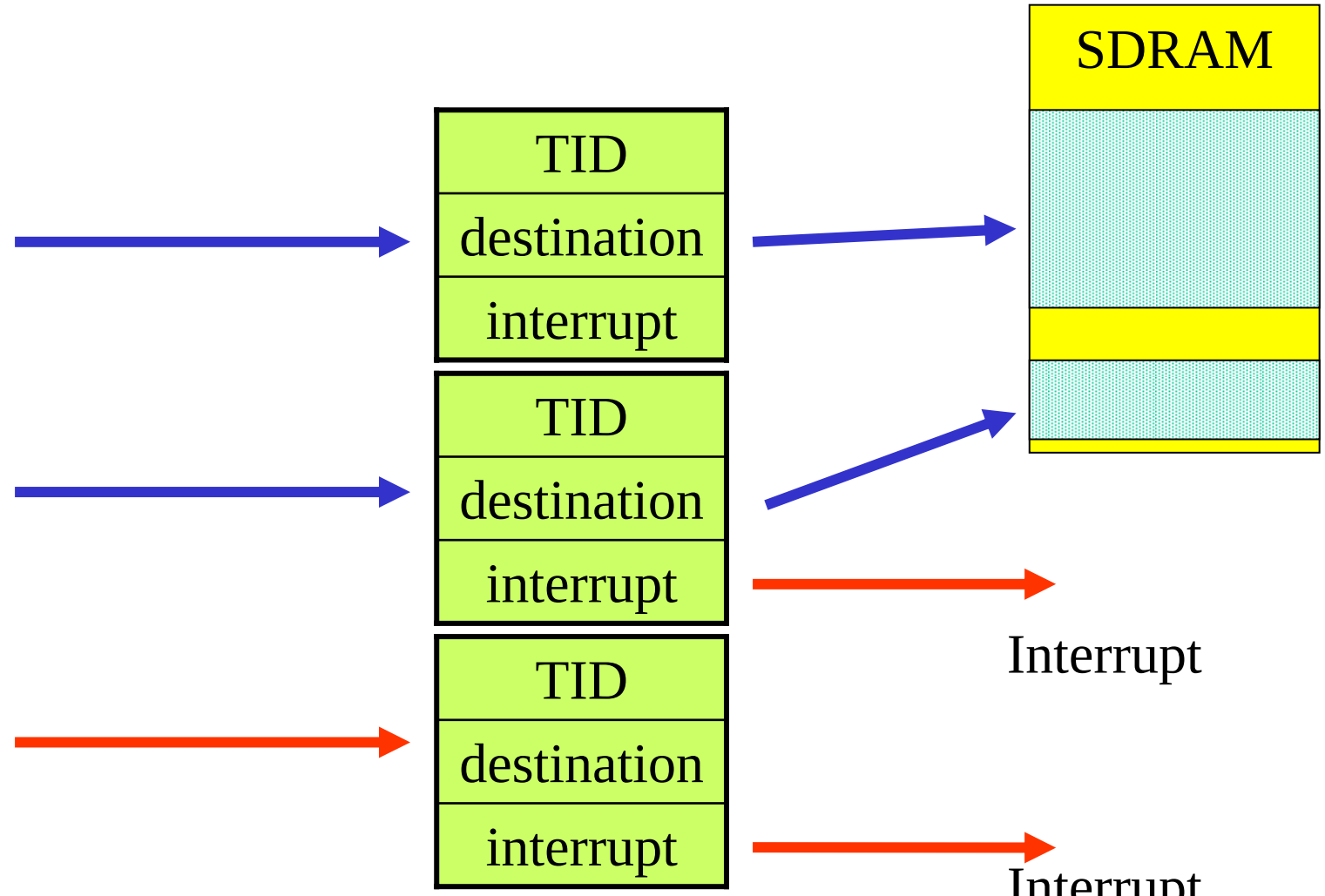
DMA engine and Host interface may share one router port.

DMA engine



Multiple transaction

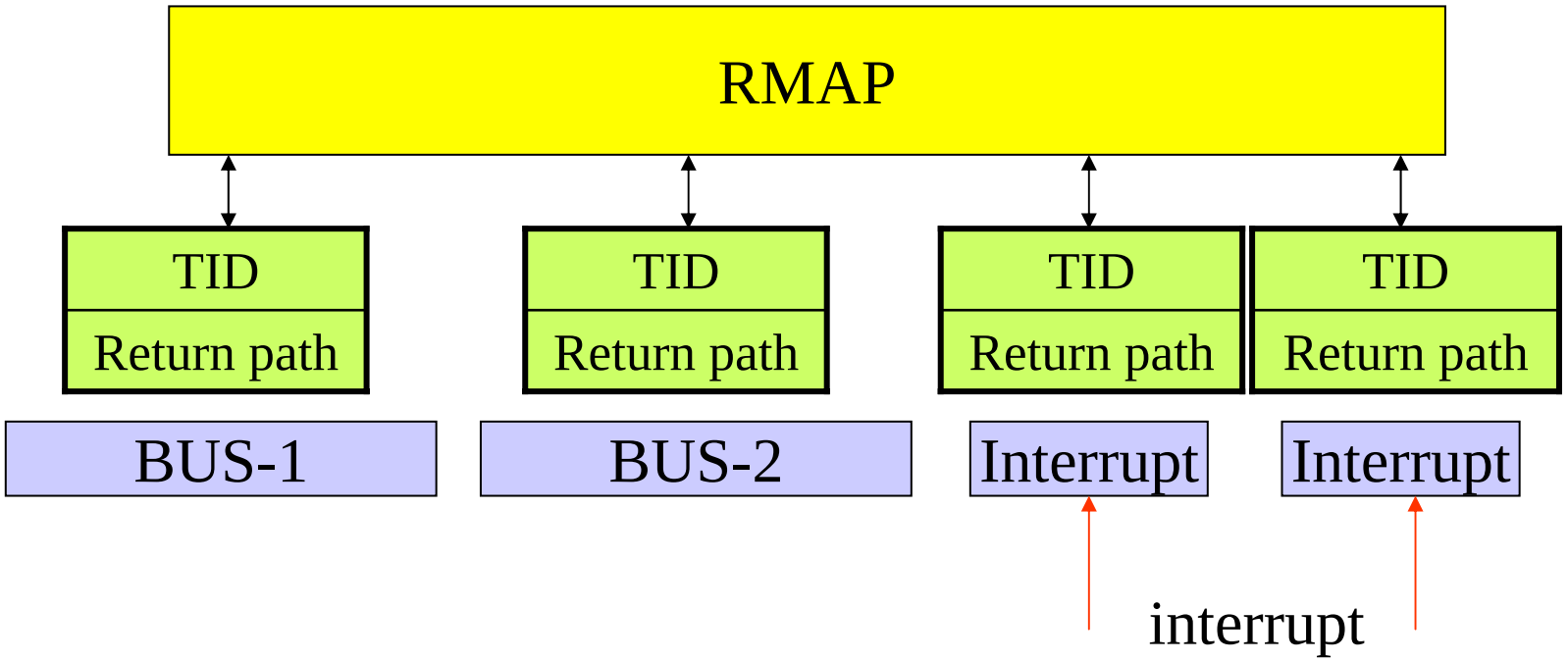
Interrupt handling



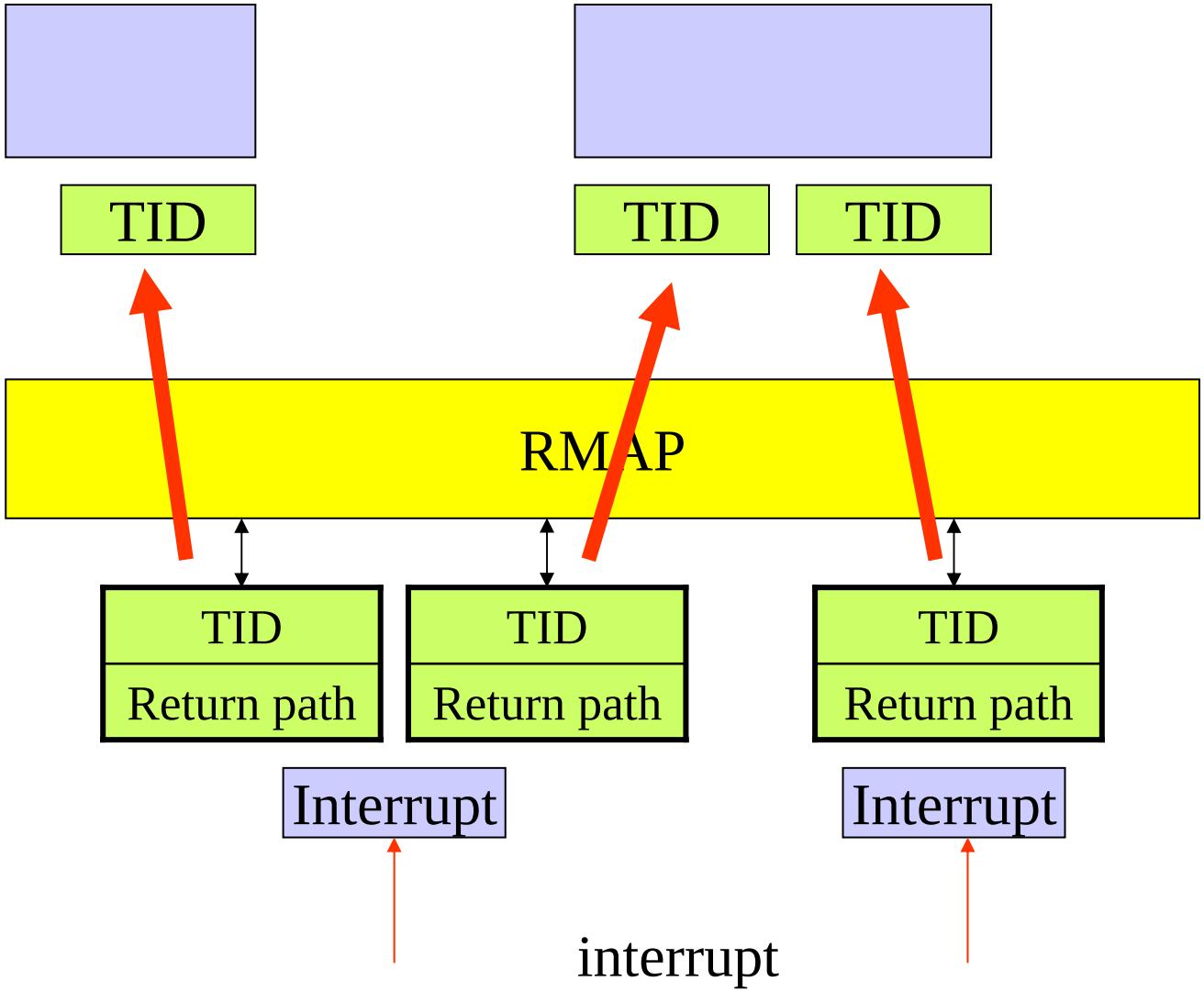
Multiple transaction

Multiple transaction handling at a front-end module

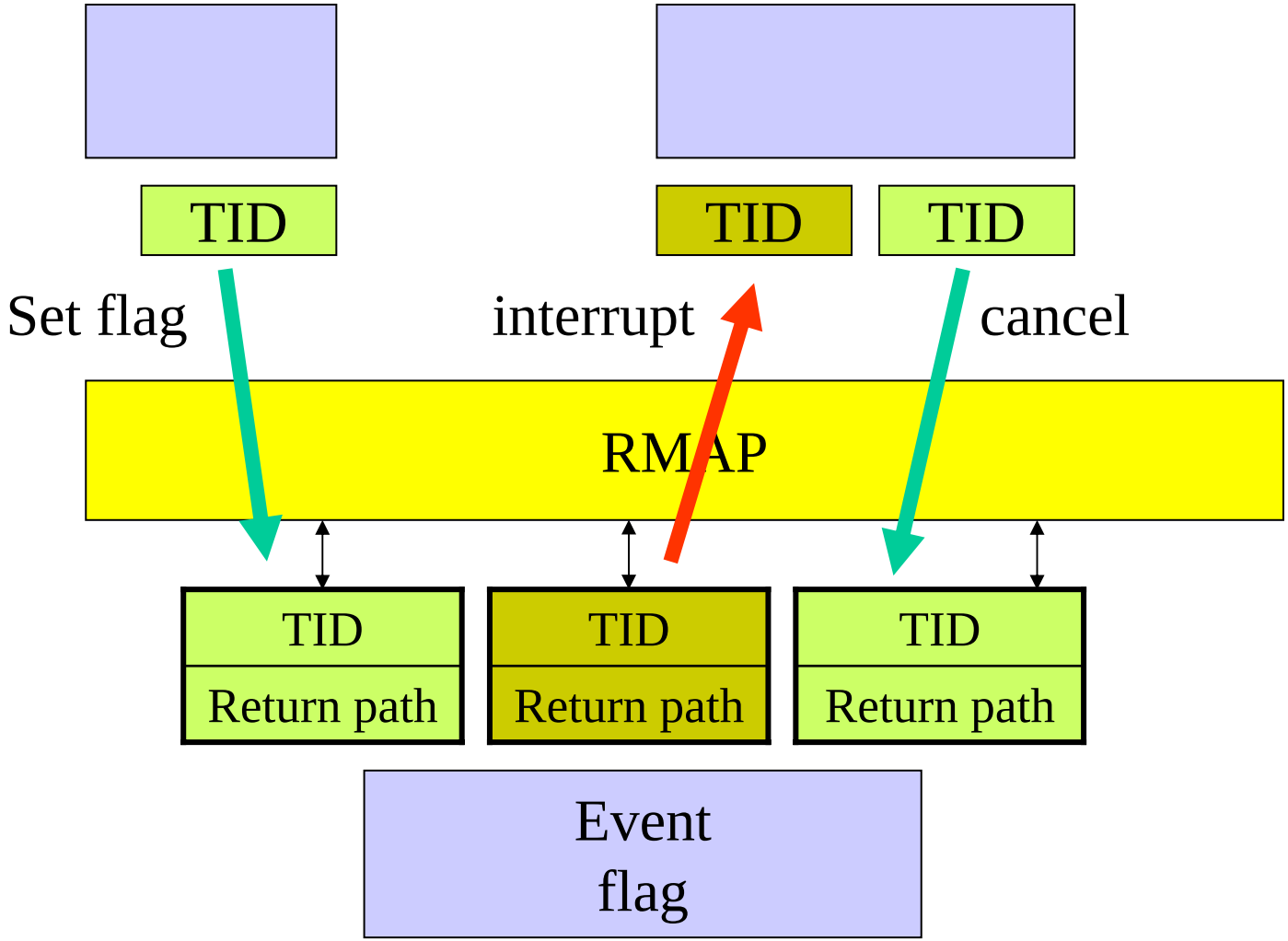
- Multiple bus
  - High speed one direction bus/random access bus
  - Interrupt handling



Interrupt handling



Event flag for multi processing units



summary

- Common architecture for many applications
- Various data collection scheme
  - Direct access
  - Collection of fragmented data
  - DMA engine
  - Multi transaction
  - Interrupt with RMAP
- Evaluation modules and templates
  - Increase the number of companies
  - More and more active students
- Real Time Conference 2007 at Chicago 29/4-5/5
  - IEEE nuclear/particle and plasma physics
  - Space applications are welcome