SpaceWire Working Group Meeting #8

"MCFlight™ - "MULTICORE" platform based chipset with SpaceWire links for distributed Aerospace systems

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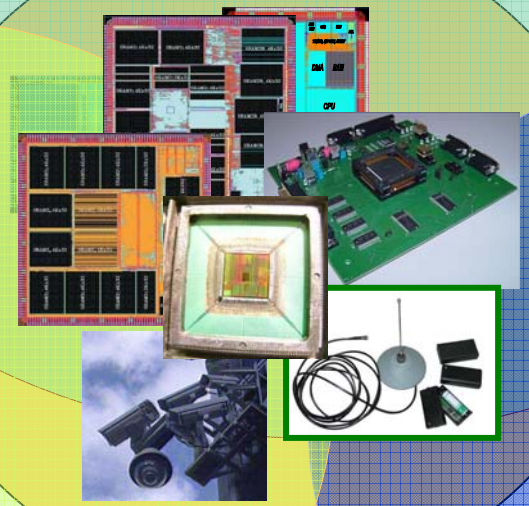
ELVEES

AGENDA

- ELVEES's market segments
- "MULTICORE" Platform
- MCFlight Chipset parameters
- The MCFlight on-board system example
- Conclusions

ELVEES market segments

ELVEES proprietary
SOC Platform "**MULTICORE**"
with **"silver/gold" IP-cores**



Embedded, space & security systems

Application specific chipsets for Telecommunications & Aerospace

ELVEES's proprietary "MULTICORE" SOC/ASIC design Platform

APPLICATIONS

SOFT

ALGORITHMS

SOFTWARE TOOLS

APPLICATION SOFTWARE

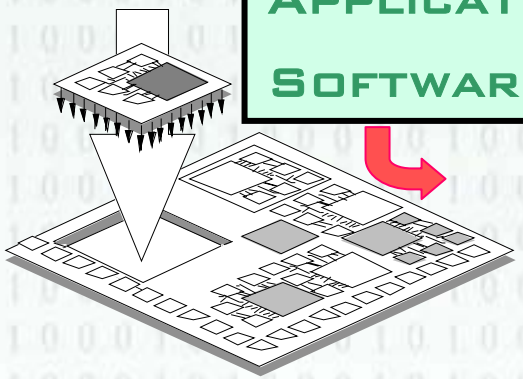
SOC DESIGN TECHNOLOGY

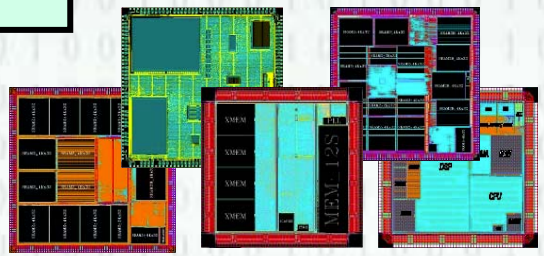
HARD

ARCHITECTURE

IP-CORES LIBRARY

6-9 MONTHLY DESIGN FLOW





Chips examples

ELVEES's "MULTICORE" platform main differences

❑ Programmability:

- ✓ very short program code (in the 8-10 time (vs. ADI and TI DSP Chips);
- ✓ powerful module SW/HW Tools (MCStudio™);
- ✓ 4 groups programmable IP-Cores;

❑ Scalability and flexibility at the levels of:

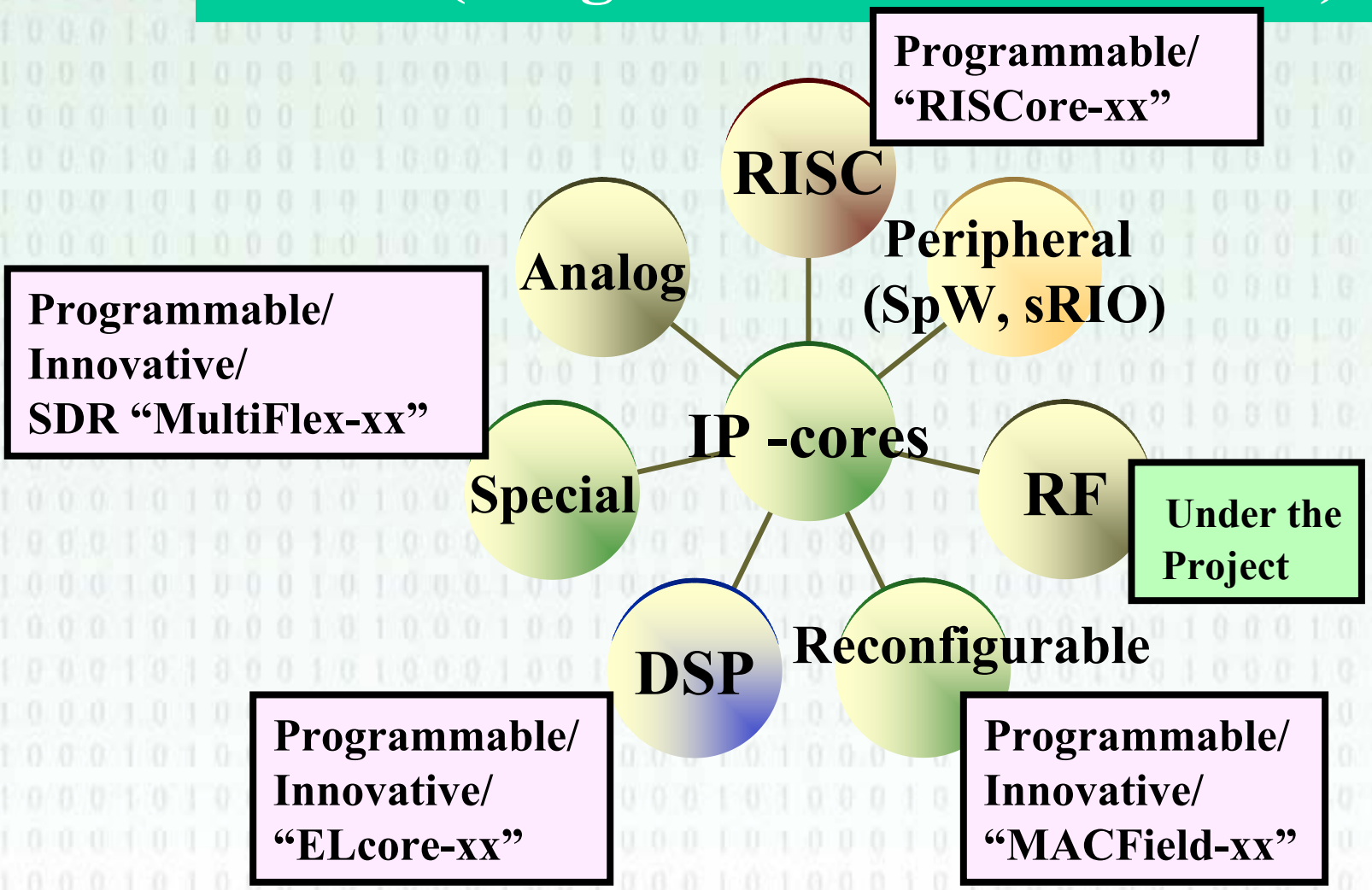
- ✓ IP-cores - SIMD/MIMD/ pipeline/ superscalar IP-cores extensions;
- ✓ chips - multiple processors on the single silicon (nRISC + kDSP + l SDR-cores+ m Reconfiguration-cores);
- ✓ systems: multidimensional systems configurations on the base SpaceWire and Serial Rapid IO standards (as RIO Trade Ass. Member);

❑ Only commercial CMOS technologies (for analog, RF - microcircuits and radiation tolerant chips);

❑ Proprietary "Gold" and "Silver" IP-cores Library

SOC integration in Chips and World level of IC characteristics (Hundreds GOPs, Tens GFLOPs)

MULTICOR IP-Cores Library groups (Programmable IP-CORES)



"MULTICORE" – RUSSIAN INNOVATIVE VLSI DESIGN PLATFORM (CHIPS EXAMPLES)

"MultiCore" - the 1-st in Russia Digital Signal Controllers (DSC) chipset

100 MHz,
300 MFLOP/s

100 MHz,
600 MFLOP/s

120 MHz,
1440 MFLOP/s

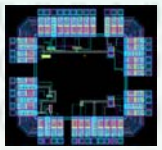
120 MHz,
1440 MFLOP/s

400 MHz, 10 GFLOP/s (EE)

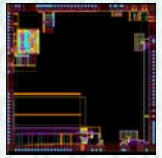
Telecommunication processor, 340 MHz

Digital SDR-receiver, 100 MHz

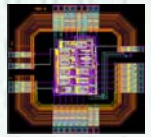
Multimedia processor, 300 MHz



LF/MF/HF/UHF transceiver, 6 GHz



DDS, 1 GHz



ADC, MFA-1410

"MCFlight" - the 1-st in Russia chipset with Space Wire Links (ELVEES&MiT)

MC-24R, DSP-controller , 600 MFLOP/s

MCB-01, 4ch SpaceWire/ PCI adapter

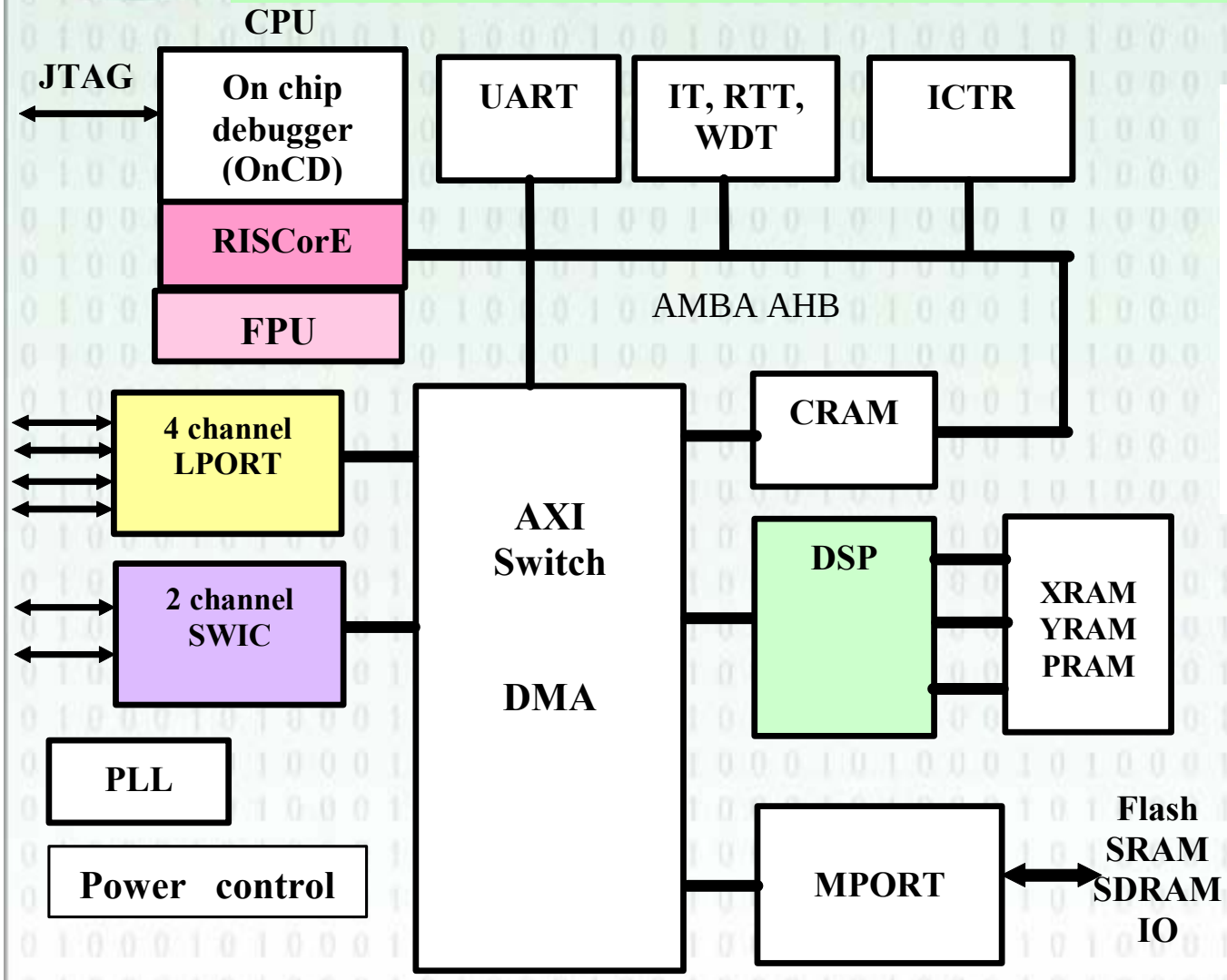
MCK-01, 16ch Space Wire Router

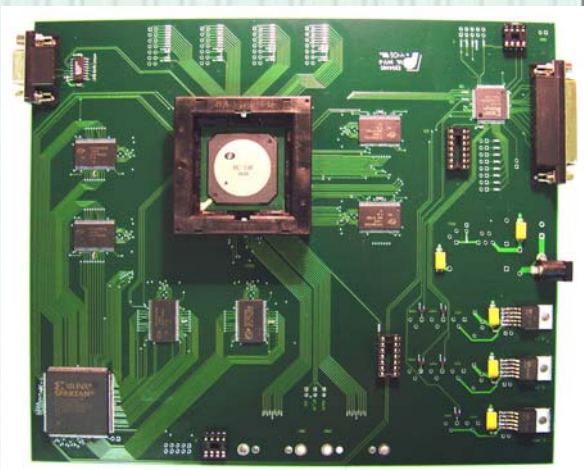
MCT-01, SpaceWire Remote controller

120 MHz, 64-bit FPU

RAM –R, 4 Mb

MC-24R – 600GFLOPs
DSP-controller with SpaceWire Links





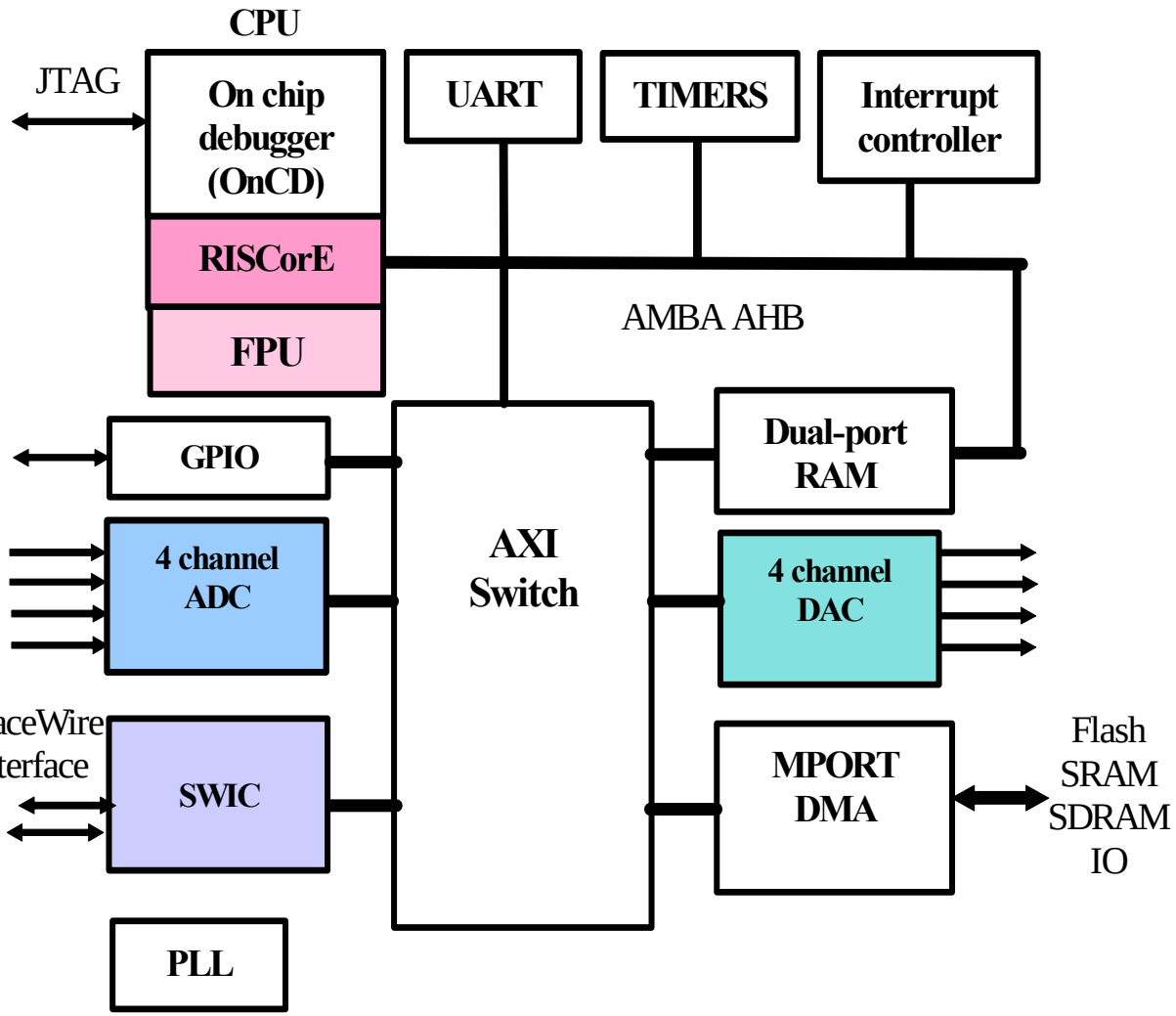
MC-24R parameters (preliminarily)

- 0.25-u;
- 2 channel SpaceWire, ECSS-E-50-12° standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- two-cores MIMD architecture with the dual processor cores:
  - RISC core (MIPS32-64FP based on “MULTICORE” IP library) with 64 bit accelerator in IEEE754 FLP standard;
  - DSP ELcore18 core, 200 MHz;
- peak performance - 600 MFLOPs;
- power consumption control;
- radiation tolerant for aerospace applications;
- package - HSBGA416 (for the engineering samples)

ELVEES "MultiCore" vs. with the TI&ADI DSP chips

Performance description	ELVEES				Texas Instruments		Analog Devices	
	MC-24 100 MHz	MC-0226 120 MHz	MC-0428 400 MHz	MC-24R, 200 MHz	C6701 166 MHz	C6416 600 MHz	TS201 600 MHz	BF-53 600 MHz
State of the art of the "MultiCore" series ICs	Mass prod.	Mass Prod.	Test, 2007	Mass Prod., 2007	Mass Prod.	Mass Prod.	Mass Prod.	Mass Prod
Peak performance, formats: • 16b FP (MIPS) • 32b FLP (MFLOPS)	1 600 600	3 840 2 880	28 800 10 800	1 600 600		4 800	9 600 3 600	3360
FIR-filter, 35 taps*1024 (mcs): INT 16*16+32	99.8	41.6	5.6	99.8	393	25.7	8.4	
FFT-1024, complex (mcs): • block FP(16+j16) • 32b FP (32+j32)	57.6 103.2	28.8 51.6	3.2 5.8	57.6 103.2	160	11	7.75 16.8	
DCT-8x8, 16b (mcs):	0.6	0.3	0.04	0.6				< 0.5
ACS-operations, MOPS: (for Viterbi decoder, 16b)	200	480	3 600	200				

MCT-01 (SpaceWire Remote controller)



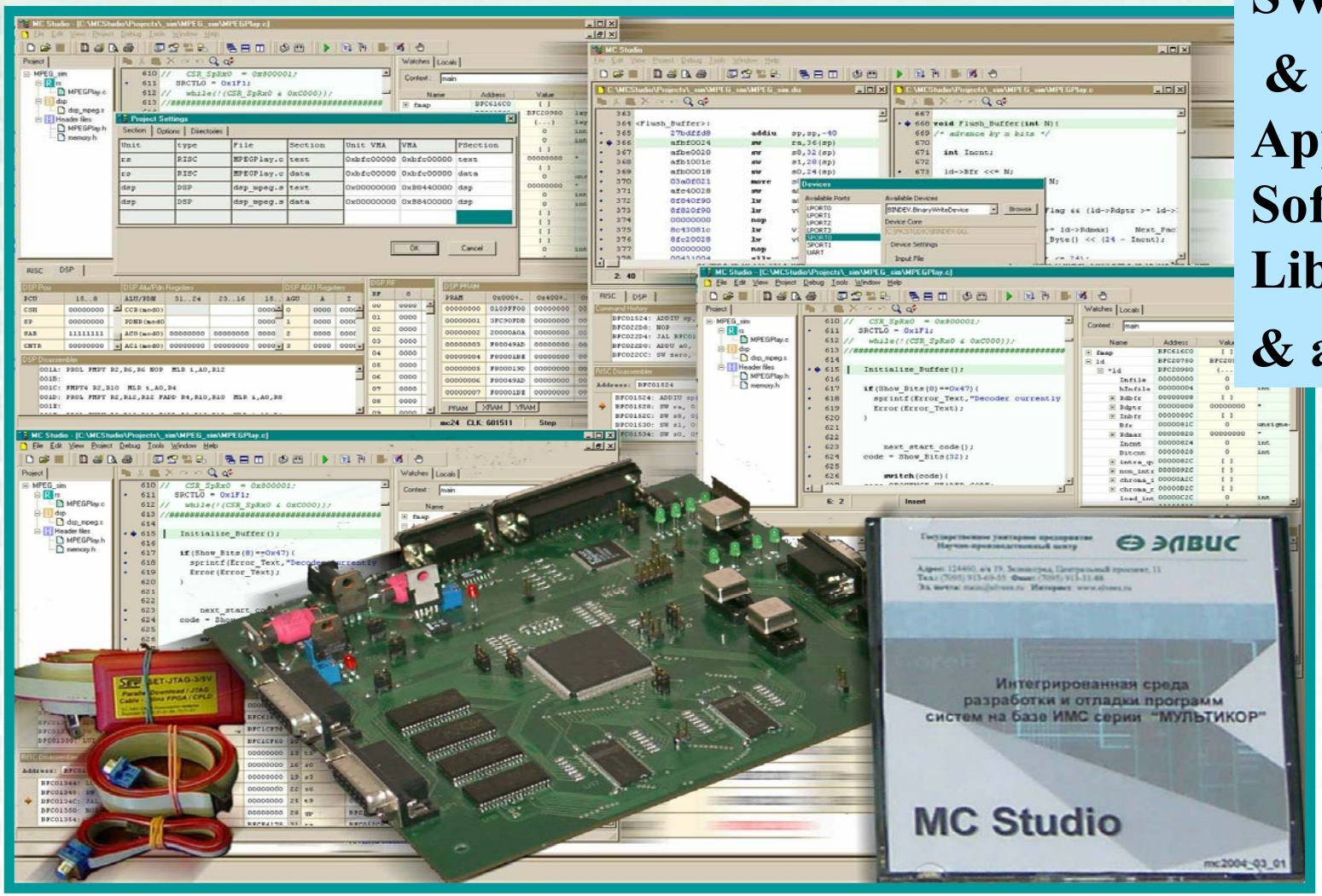
SpaceWire

MCT-01 parameters (preliminarily)

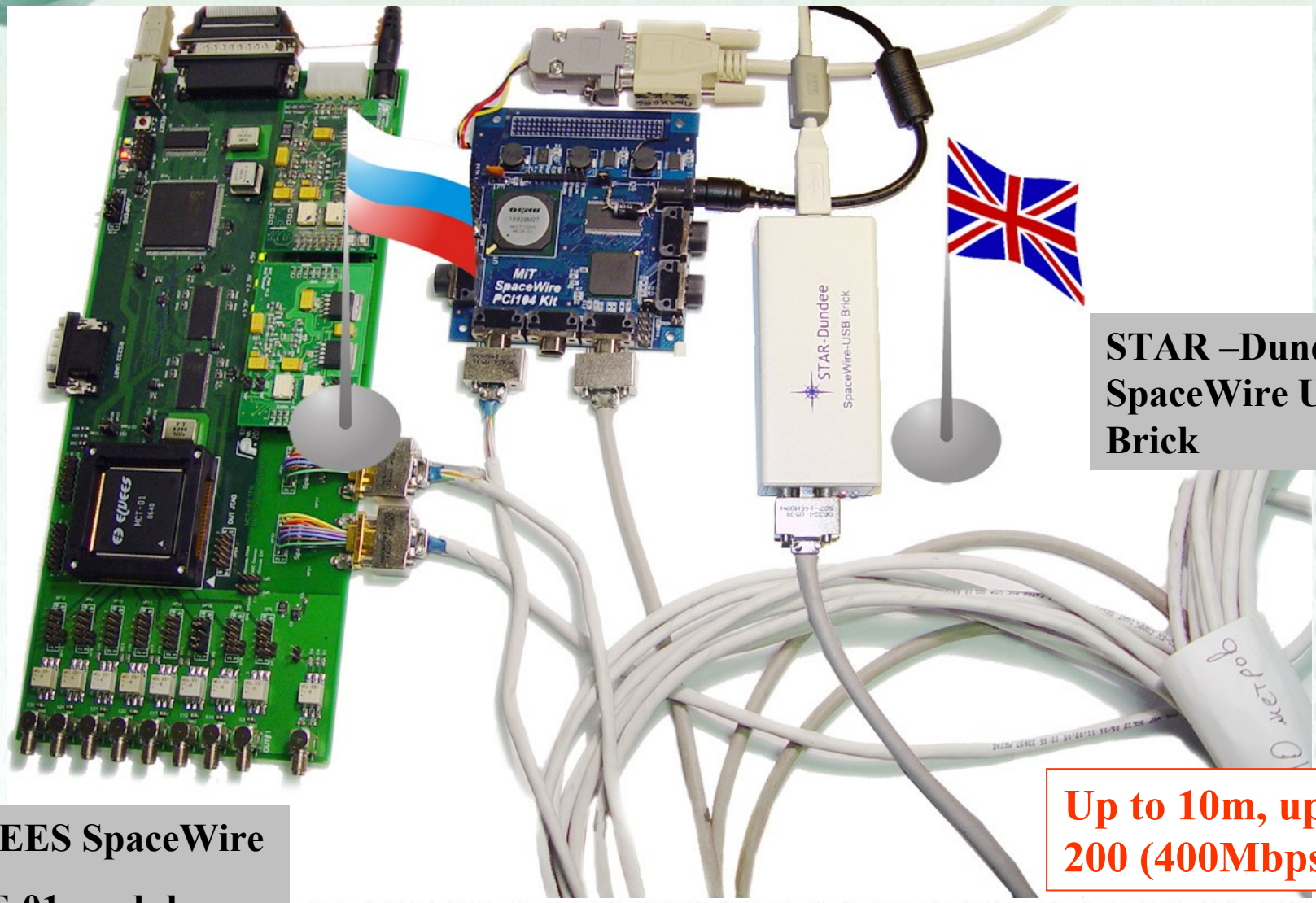
- 0.25-u;
- 2 channel SpaceWire, ECSS-E-50-12A standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- RISC core (MIPS32-64FP based on “MULTICORE” IP library) with 64 bit accelerator in IEEE754 floating point standard;
- peak performance - 120 MOPs in 32 bit fix point format;
- option - embedded 4 channel ADC and DAC, 1 MHz
- test examples are manufactured, tested and verified comparing with and an international implementation of SpaceWire;
- Radiation Tolerant for mass production chips samples ;
- package – QFP240 (for the engineering samples)

Tools: SDK (MCStudio) for Digital Signal Controllers (DSC) – MC-24R and MCT-01

SW Tools & Application Software Library & algorithms



Experiment in compatibility European/Russian SpaceWire implementation



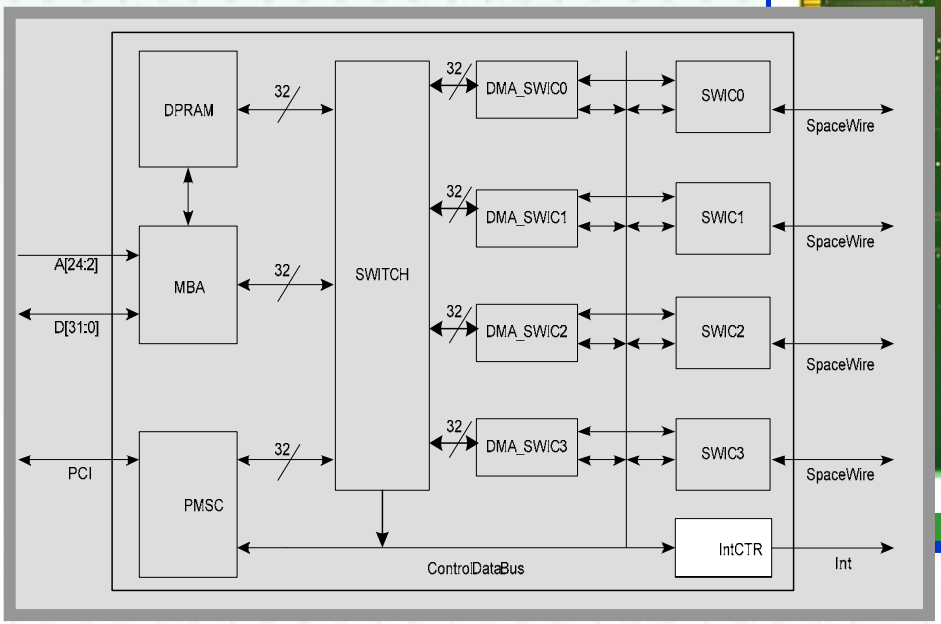
STAR –Dundee SpaceWire USB Brick

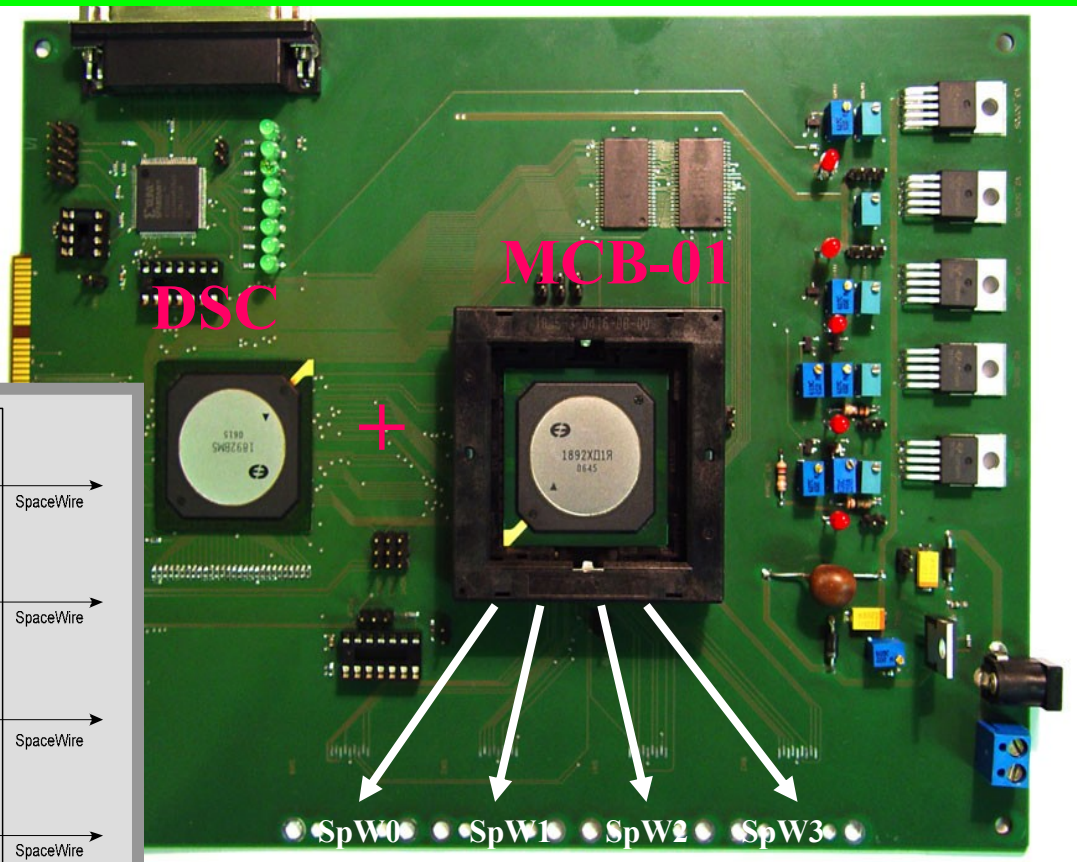
ELVEES SpaceWire MCT-01 module

Up to 10m, up to 200 (400Mbps)

MCB-01 (1892XD1Я) - 4-channels SpaceWire/PCI adapter for MultiCore Chipset enhancement

1.5 GFLOPs 4-Channel Processor Element with SpaceWire Links

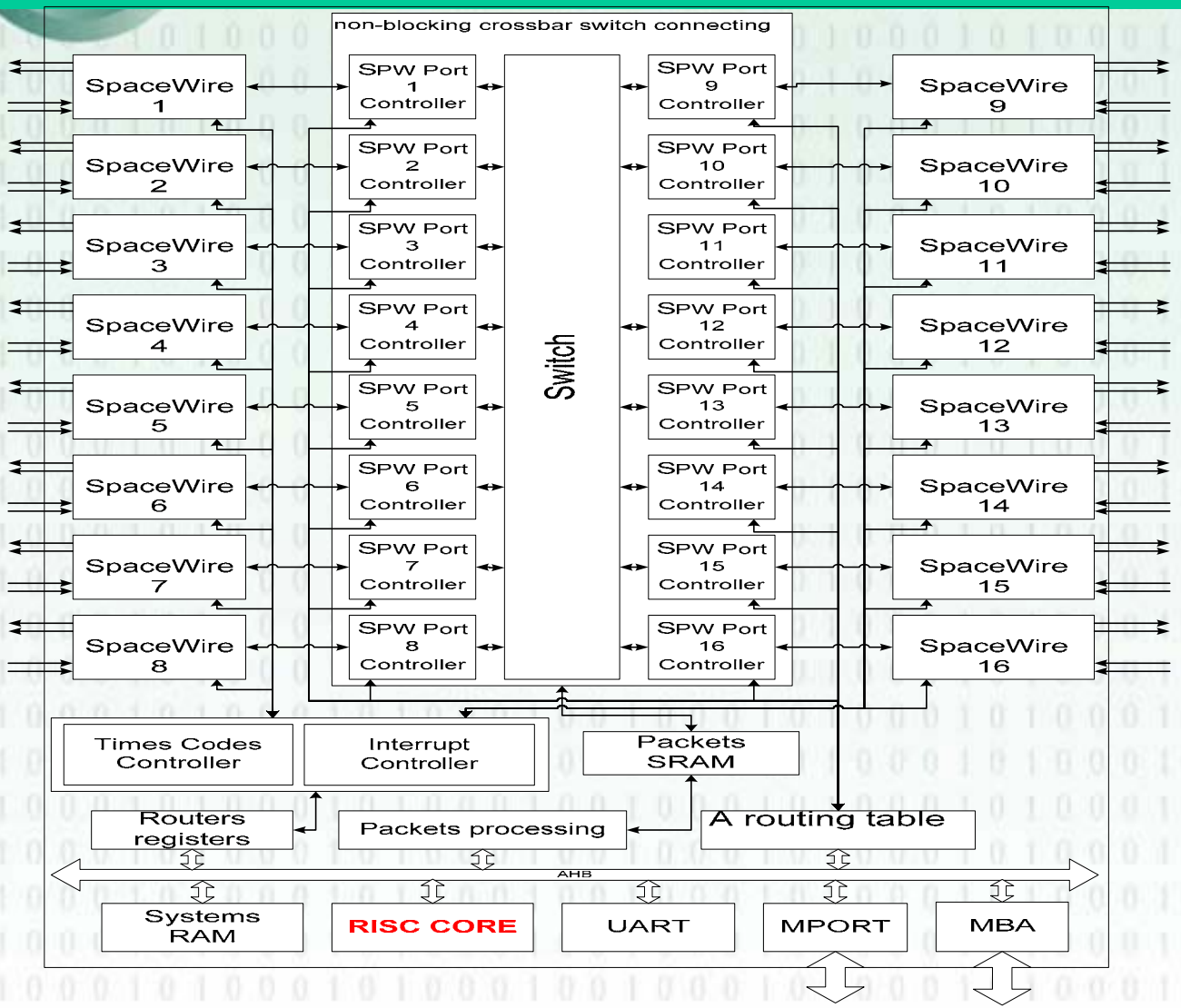


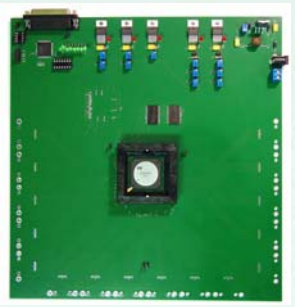


MCB-01 parameters (preliminarily)

- 0.25-u;
- 4 channel SpaceWire, ECSS-E-50-12A standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- PCI (32 bit/33-66 MHz), Local Bus Specification. Rev. 2.2.;
- 32b parallel port to Multicore chipset or others processors;
- embedded SRAM, 2Мбит (64KWx32b)
- package - HSBGA416 (for the engineering samples)

МСК-01 (1892ХД2Я)-
16-channels SpaceWire Router with embedded RISC-Core





Up to 4GB SDRAM

MCK-01 parameters (preliminarily)

- 0.25-u;
- 16 channel SpaceWire, ECSS-E-50-12A standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- support of signal, symbol exchange, packet and network stack protocols of SpaceWire;
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- embedded MIPS32 compatible RISC core (based on “MULTICORE” IP library) used for the configurable port service and administration of communication networks;
- 32 bit parallel port for “MULTICORE” chipset connections or for the additional external memory;
- Embedded RAM (25 Kbytes): program and data memory for RISC core (16 Kbytes), packet memory (8 Kbytes), routing memory (1Kbytes);
- Radiation Tolerant for aerospace applications
- package - HSBGA416 (for the engineering samples)

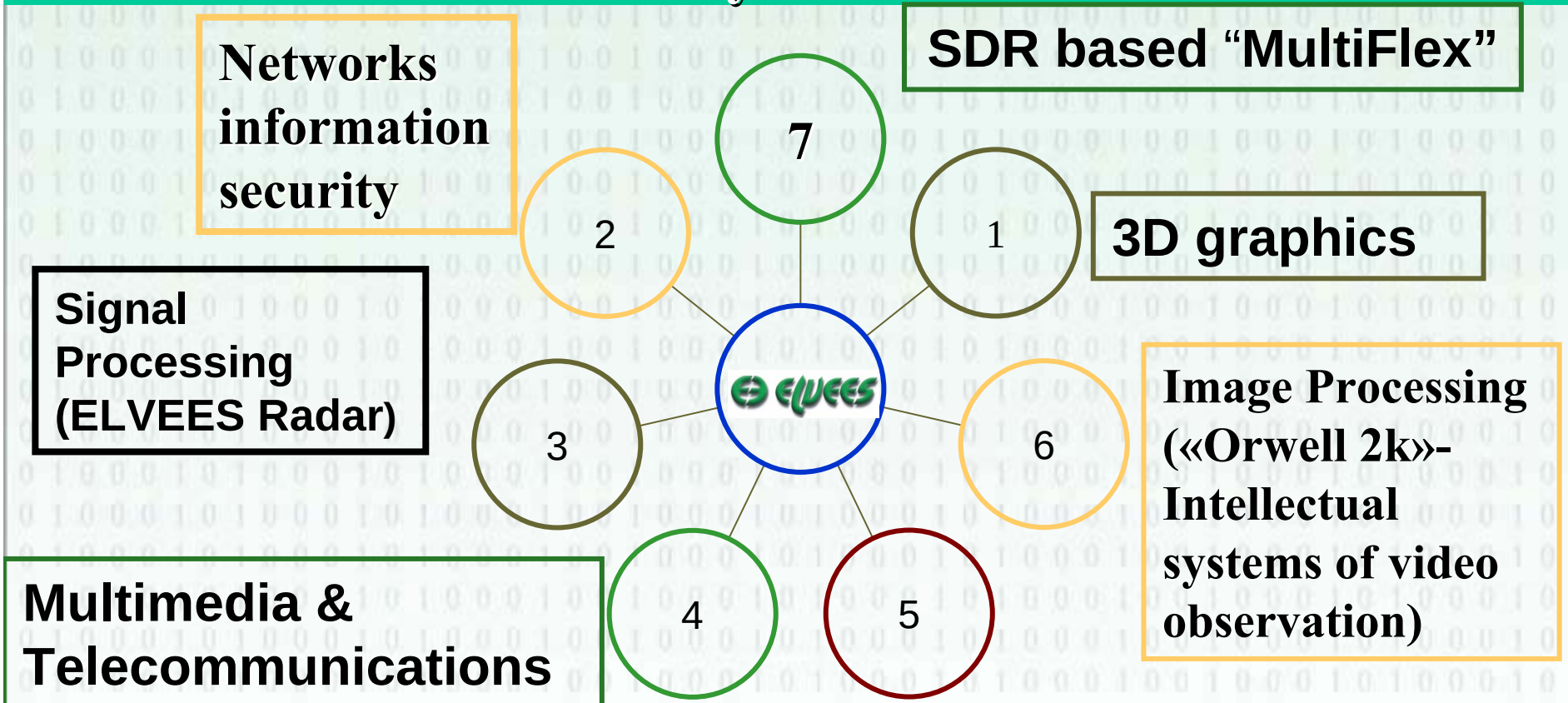
RAM for MCFlight chipset applications parameters (preliminarily)

- SRAM 4 Mbit (512KW*8b); T = 15 ns
- matched to “MULTICORE” DSC chipset, including MC-24R
- radiation tolerant for aerospace applications;
- package - HSBGA416 (for the engineering samples)

Main ELVEES technologies for chips & systems

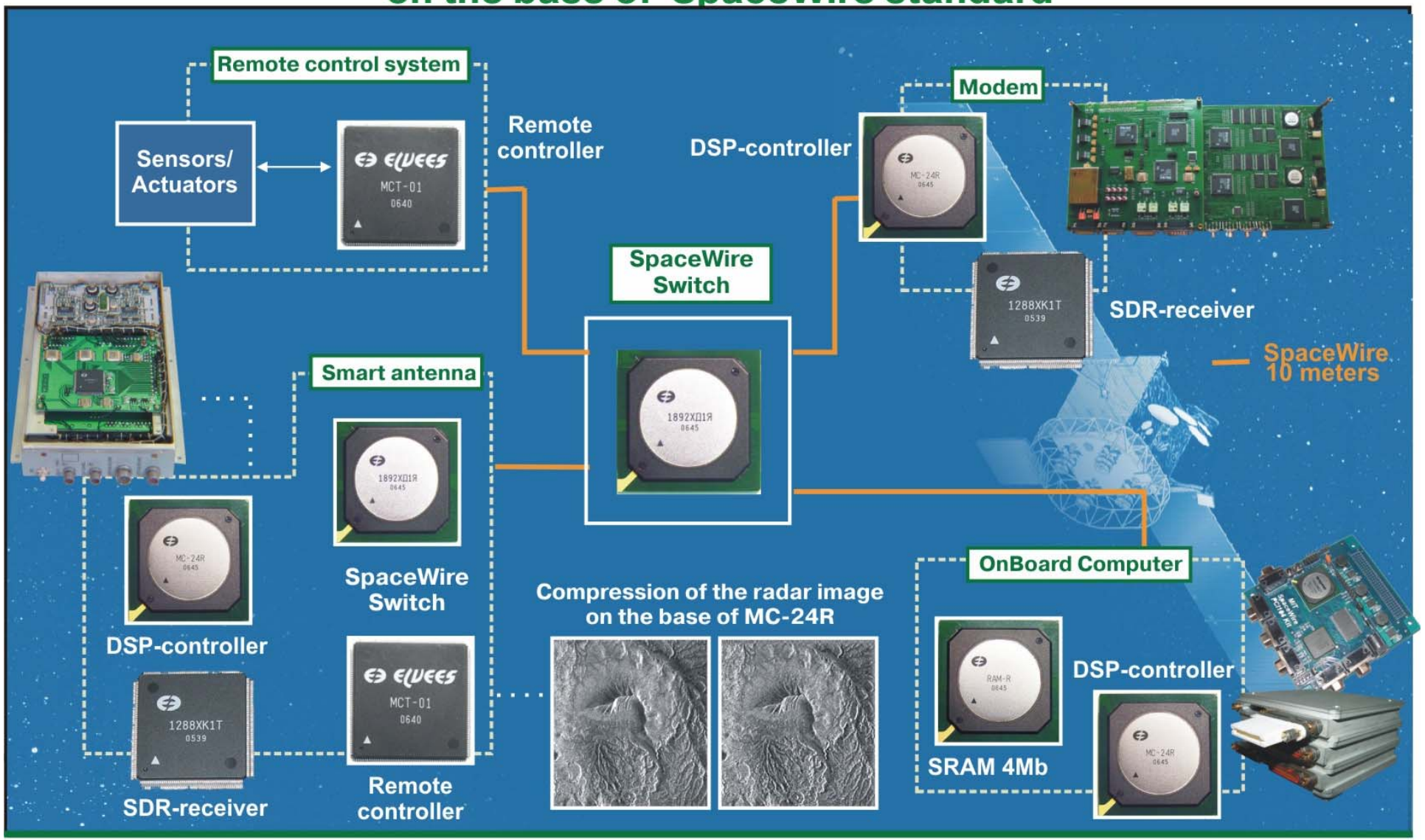
- **“Soft Defined Radio” for transceivers,**
- **Adaptive signal processing;**
- **Image processing & Multimedia & 3D graphics (compression, recognition, OpenGL support);**
- **Multistandard reprogrammable Global positioning and telecommunications (chipset, algorithms “soft” realization);**
- **Cryptographic methods and units;**
- **Radiation tolerant chipset and technologies for aerospace on-board systems with SpaceWire Links (MCFlight)**

ELVEES's technologies (chips, SW APPS Library, application systems) for image & Signal processing as a potential for perspective MCFlight based aerospace systems



“MULTICORE" - RUSSIAN INNOVATIVE VLSI DESIGN PLATFORM

Unified aerospace board on the base of SpaceWire standard



ELVEES

R&D center “ELVEES”

multicore.ru

SMALL SATELLITE BASED RADAR WITH ON-BOARD IMAGE SYNTHESIS FOR ECOLOGICAL MONITORING

Mode 1: continuous very large swath width for large scale observation

- ❑Width dimension – 630 kilometers
- ❑Linear resolution – 200 meters
- ❑Grid step for radar image – 100 meters
- ❑Number of non-coherent accumulations – 4
- ❑Number of elevation rays – 8
- ❑Number of MC-24R chips – 1

Mode 2: separate frames, high resolution

- ❑Frame dimension – 10 kilometers x 10 kilometers
- ❑Linear resolution – 3 meters
- ❑Grid step for radar image – 2.5 meters
- ❑Number of non-coherent accumulations – 4
- ❑Number of elevation rays – 1
- ❑Period of surveying (including processing) – 25 seconds
- ❑Number of MC-24R chips – 8

Conclusions

1. **The engineering samples of MCFlight - "MULTICORE" platform based chipset (0.25-u) with SpaceWire links for distributed aerospace systems have been received and its functionality is proved on the HW modules;**
2. **ASICs and FPGA SpaceWire Links provide up to 400 Mbps and higher throughput (>5m) in the cross modules connections;**
3. **Chipset provides a lot of the innovational features and supports high performance, programmability, scalability, flexibility and only commercial CMOS technologies;**
4. **A lot of ELVEES 's technologies for "MULTICORE" platform (SDR, Adaptive signal/image processing , 3D graphics , Networks information security, multimedia, Intellectual systems of video observation) will be transferred on the MCFlight chipset;**
5. **MCFlight can be easily modified (during 6-9 months) by others platforms IP-cores (for example, for SPARC RISC core) or for others interfaces**
6. **Chipsets Radiation Tolerant features are measured at the present moment and will be provided for mass production MCFlight chips at the end 2007 - the beginning of 2008 years**

Thanks for your interest!

Questions?

ELVEES TEAM

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