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Advanced Science and Novel Technology

SiGe Interconnect Solutions

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ESA 1/16/07

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Presentation Outline

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1. Dual CMOS-to-LVDS Converter.
2. Multilevel Interface (MLI).
3. Radiation Hard by Architecture (RHBA) Transponder for a cPCI Bus Extending Switching Fabric System.
4. Summary / Conclusion.

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Dual LVDS-to-CMOS Converter

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Dual CMOS/LVDS Converter

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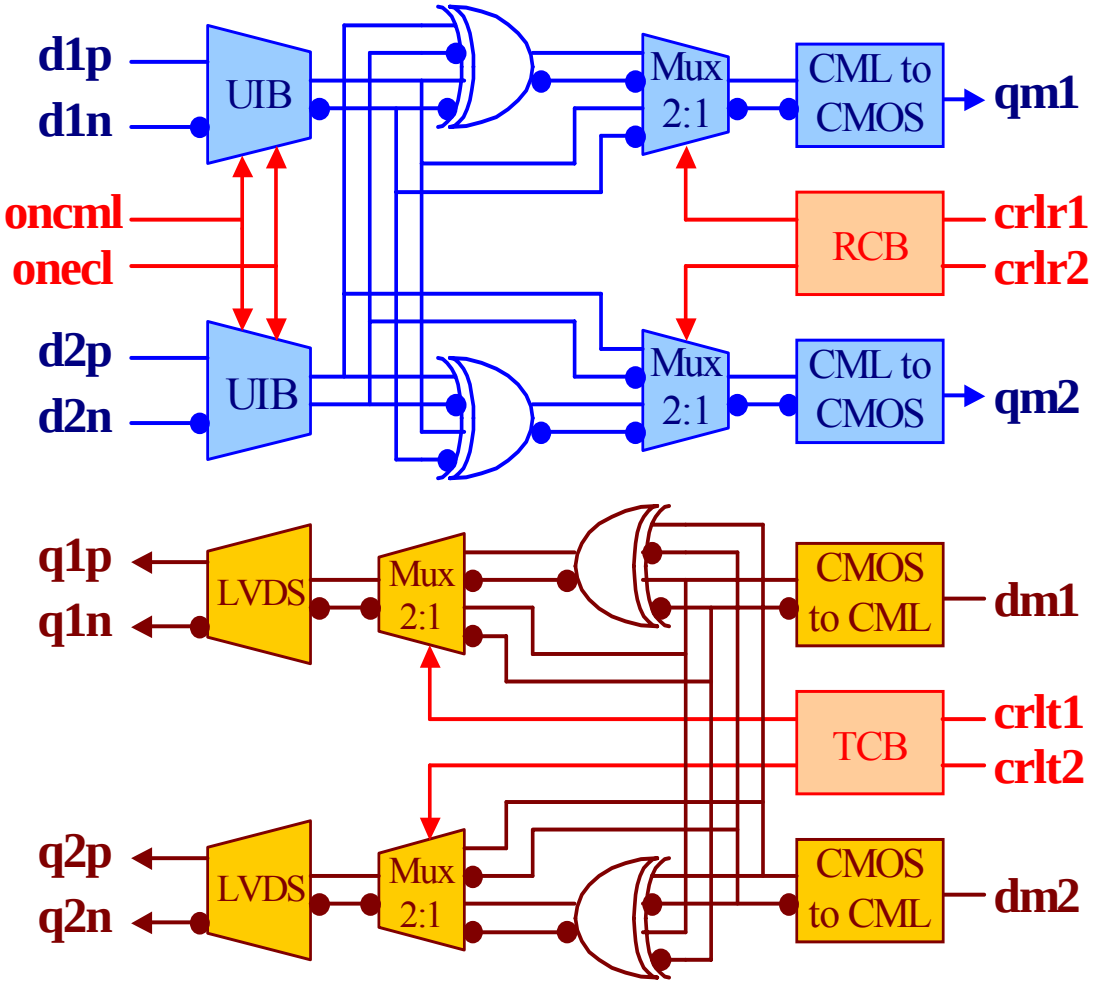
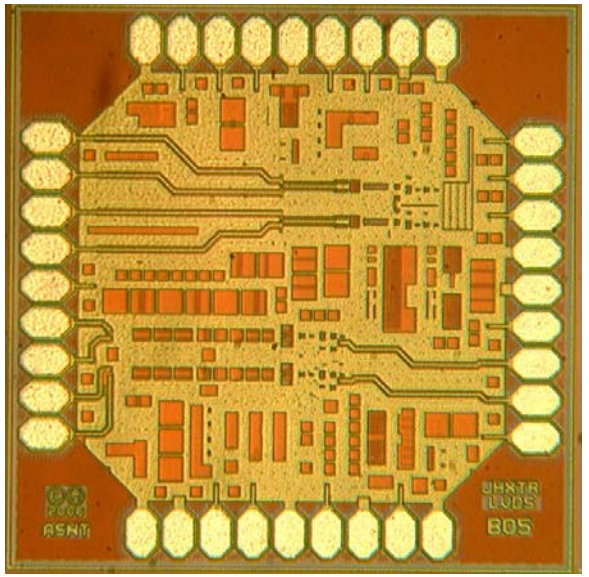


- *Optional CML/ECL input modes;*
- *Optional DS encoding/decoding (Space Wire compatibility);*
- *Flexible operational modes;*
- *High-Z output disabled states;*
- *Improved TID Protection (RHBT);*
- *Operational Speed 0…2Gb/s;*
- *Power Consumption 83mW total.*



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LVDS Output Buffer

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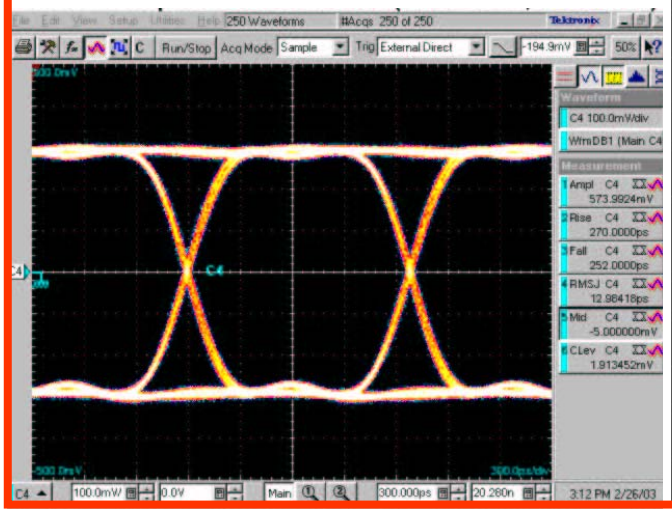
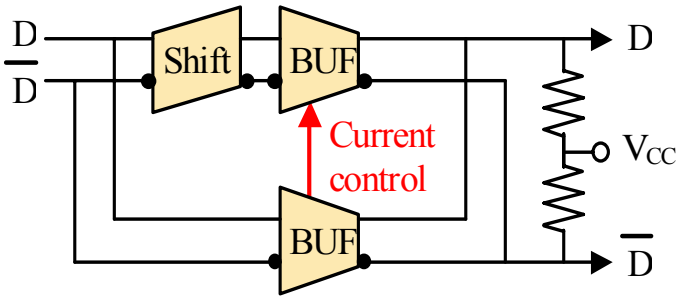
- ***Based on SiGe HBTs;***
- ***Fully compliant with IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.***
- ***Improved TID protection (by-technology);***
- ***Low power consumption.***



Symbol	Parameter	Min			Max			Units
		Standard	Simul.	Meas.	Meas.	Simul.	Standard	
V_{CC}	*Main supply voltage*		3.1	*3.1*	*3.5*	3.5		*V*
V_{CC_LVDS}	*OD supply voltage*		1.7	*1.7*	*3.5*	3.5		*V*
$\|V_{dif}\|$	*Output differential voltage*	**250**	280	*265*	*300*	360	**400**	*mV*
V_{osDC}	*DC output offset voltage*	**1125**	1182	*1192*	*1200*	1233	**1275**	*mV*
V_{osHS}	*Output offset voltage at f_{max}*	**1125**	1133	*1146*	*1153*	1198	**1275**	*mV*
V_{hi}-V_{lo}	*Output voltage shift (DC impedance test)*	**178**	193	*255*	*262*	280	**295**	*mV*
R_o	*DC output impedance (derived from V_{hi}-V_{lo})*	**40**	47	*88*	*95*	117	**140**	*Ω*
$\|(V_{ahi}$-$V_{alo})$-$(V_{bhi}$-$V_{blo})\|$	*Mismatch of the output voltage shifts (output impedance deviation)*	-	-	-	*9 (4.5%)*	12 (6%)	**20 (10%)**	*mV*
Z_o	*AC output impedance (from 0 to f_{max})*	**40**	43	*52*	-	123	**140**	*Ω*
I_{totalD}	*Total current (1 data buffer) at 1Gb/s*	-	4.1	*4.4*	*5.2*	5.6	-	*mA*
I_{totalC}	*Total current (1 clock buffer) at 1GHz*	-	5.6	*6.0*	*6.4*	6.9	-	*mA*
I_{sGND}	*Output current, driver shorted to GND*	-	-	*21*	*22*	16.5	**40**	*mA*
I_{sab}	*Output current, outputs shorted together*	-	-	*5.4*	*5.6*	6.5	**12**	*mA*
f_{maxD}	*Speed range (data buffer)*	-	0	-	*777.6*	1.0	-	*Gb/s*
f_{maxC}	*Frequency range (clock buffer)*	-	0	-	*777.6*	1.0	-	*GHz*
t_{rD}/t_{fD}	*Rise/fall time (data buffer, 20%-80%)*	**300**	-	*370*	*400*	402	**500**	*ps*
t_{rC}/t_{fC}	*Rise/fall time (clock buffer, 20%-80%)*	-	-	*210*	*230*	280	-	*ps*
j	*Jitter (data buffer)*	-	9	*13.5*	*14.2*	14	-	*ps*

Universal Input Buffer



"oncml" value	"onecl" value	Termination		
		Type	Resistance	Voltage
vcc	vee	SE	50*Ohm*	vcc
vee	vcc	SE	50*Ohm*	vecl
vee	vee	Diff.	100*Ohm*	-

Main Parameters:

V_{CM} 0-V_{CC}

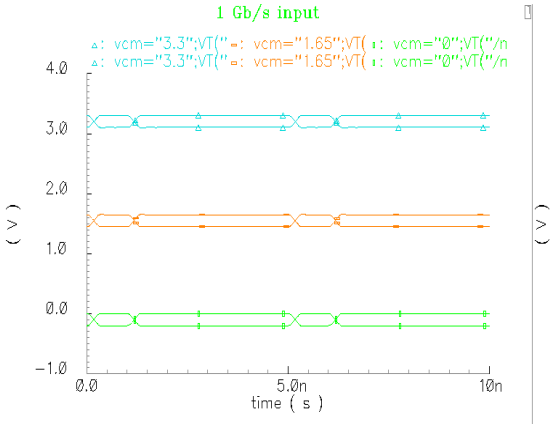
ΔV_{IN_Dif} $40mV$

ΔV_{IN_SE} $\pm 20mV$

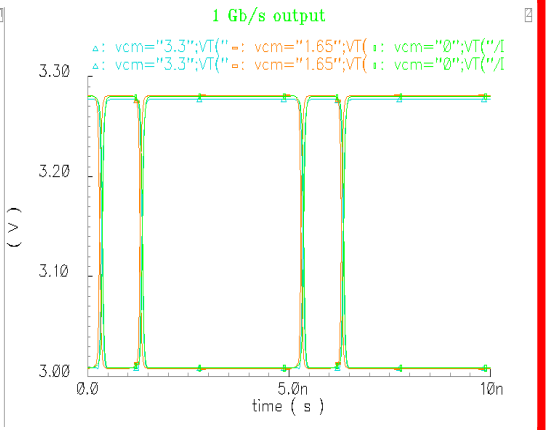
f_{IN} $0\text{-}1GHz$

Not Sensitive to Vcm!

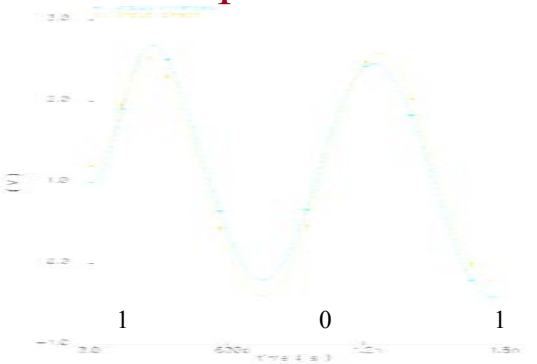
Diff. Input with DC Shift



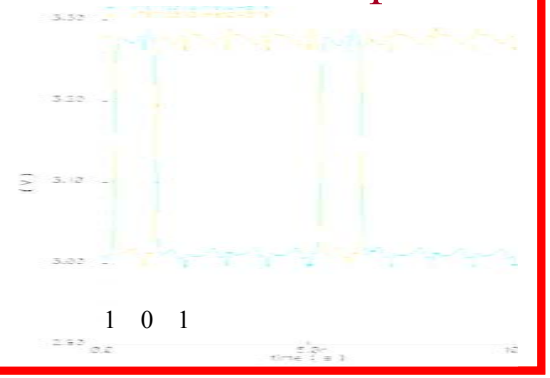
CML Output



Diff. Input with AC Shift



CML Output



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Multi-Level Interface (MLI)

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ML Interface Concept

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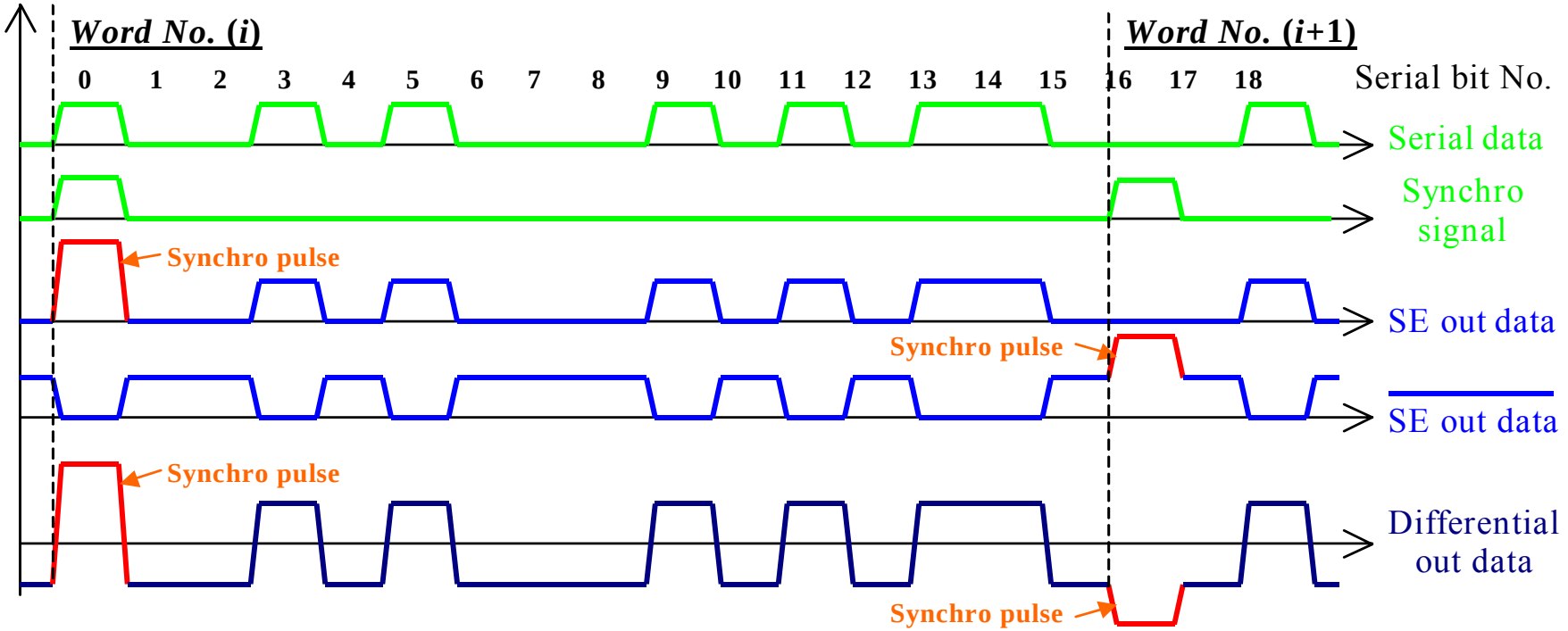
ADSANTEC's patent-pending solution (filed January 6, 2004)



A ***Synchro pulse*** of increased amplitude is imposed by the ***transmitter*** onto the ***first bit*** of ever ***outgoing serialzed word***.

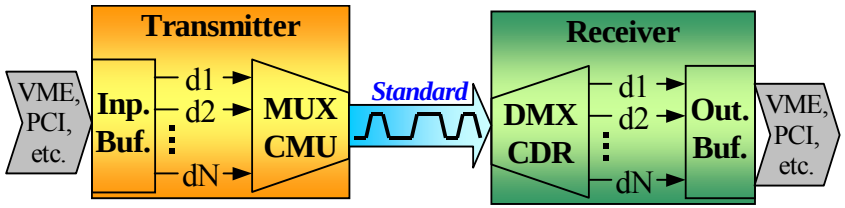
The pulses appear ***arbitrarily*** in ***single-ended*** (SE) data, but ***regularly*** in ***differential*** data.

The repeating pulses are ***retrieved*** from the ***incoming serial data stream*** by the ***receiver*** and are used for simplified ***clock & data recovery*** and ***bit/word alignment***.

2-Level vs. Multi-Level

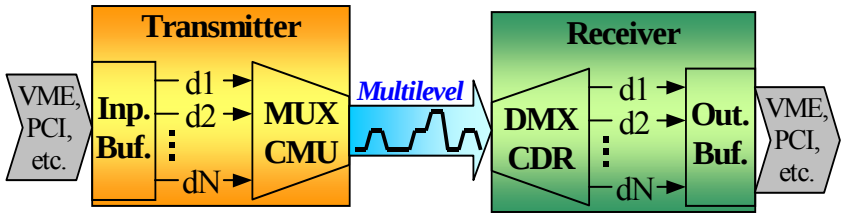
ADSANTEC's patent-pending solution (filed January 6, 2004)

Standard Serial Interface



- Advantages:
  - *simple input/output circuitry,*
  - *simple media loss equalization.*
- Problems:
  - *reduced transmission speed,*
  - *extra latency,*
  - *complicated hardware,*
  - *code-specific encoding software,*
  - *poor upgrade ability.*

Multilevel Interface



- Advantages:
  - *maximum transmission speed,*
  - *minimal latency,*
  - *efficient clock recovery,*
  - *easy multi-channel alignment,*
  - *high upgrade ability.*
- Problems:
  - *more complex I/O circuitry,*
  - *more complicated equalization.*

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Multi-Level MUX CMU

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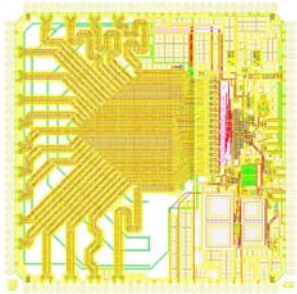
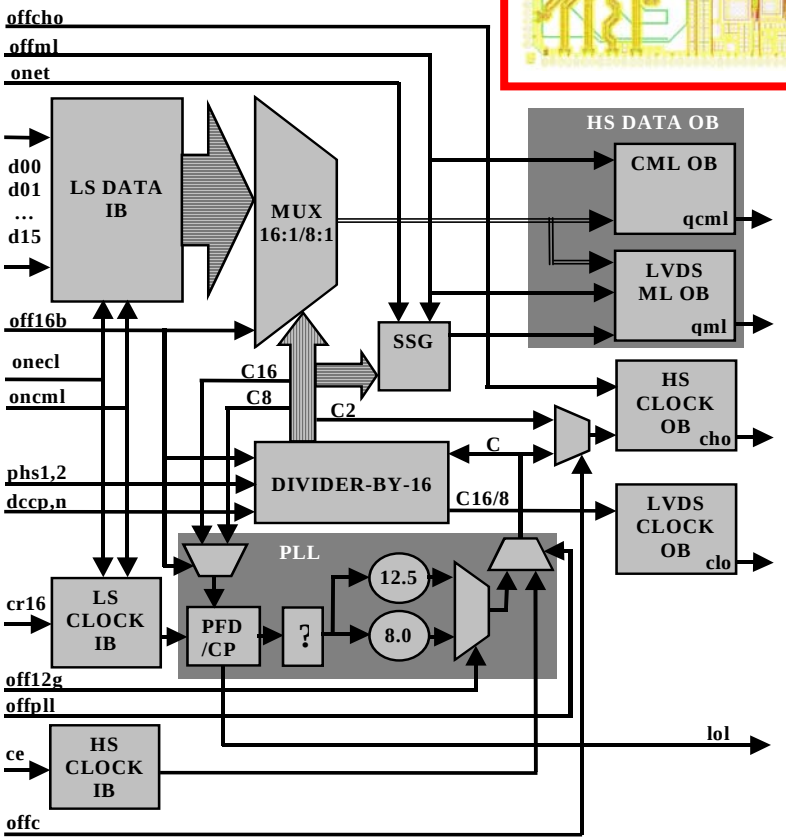
12.5/8.0*Gbps*, 16:1/8:1 Serializer with CMU or 12.5*Gbps* Digital broad-band 16:1 Serializer



- Single +3.3*V* power supply (V_{CC});
- LVDS, CML, and ECL compatible Input Data and Reference Clock buffers;
- Output Data buffer featuring LVDS Multi-level or CML output signaling;
- On-chip PLL provides clock synthesis from low-speed clock reference;
- Selectable CML Clock Output buffer with a standard 50*Ohm* termination scheme;
- Full-rate CML Input Clock buffer with on-chip 50*Ohm* termination;
- Clock-Divided-By-Sixteen LVDS Output Buffer with 90°-step phase selection;
- Rated for industrial temperature range;
- 550*mW* nominal power consumption at 12.5*Gbps*.



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Multi-Level DMUX CMU

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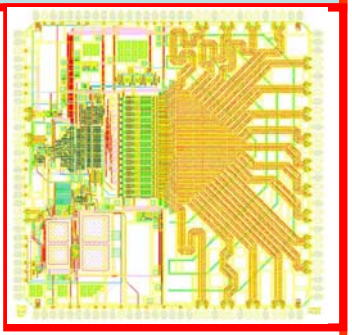
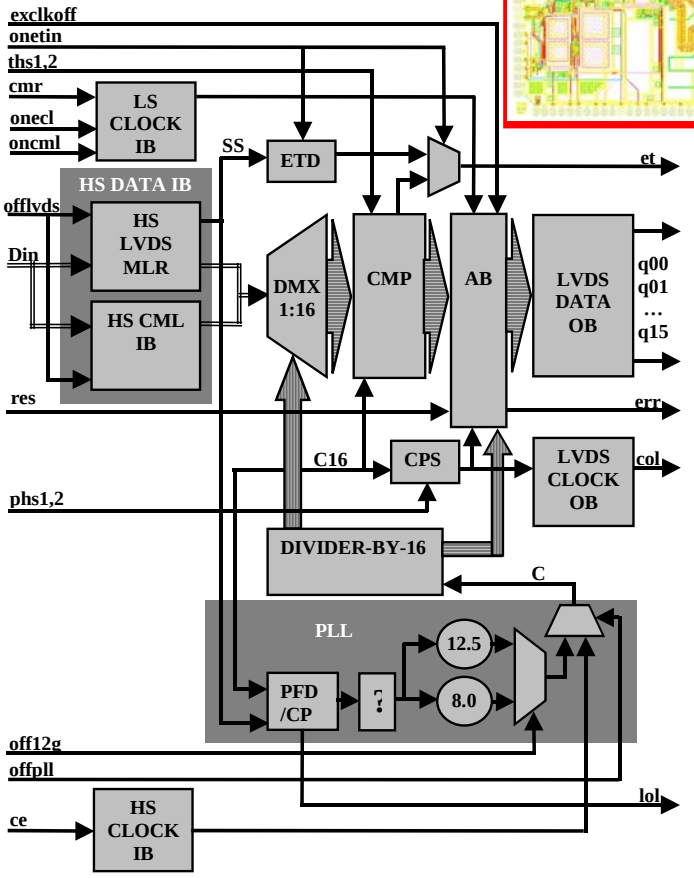
12.5/8.0*Gbps* 1:16 Deserializer with CMU or 12.5*Gbps* Digital broad-band 1:16 Deserializer



- Single +3.3*V* power supply (V_{CC});
- Input Data buffer featuring a selectable Multi-level LVDS or CML interface;
- LVDS Output Data and Clock buffers for low-power operation;
- On-chip PLL provides clock synthesis from recovered Synchro-pulses;
- Full-rate CML Input Clock buffer with on-chip 50*Ohm* termination;
- Output FIFO with external Master Clock input;
- Digital comparator with programmable threshold;
- Clock-Divided-By-Sixteen LVDS Output buffer with 90°-step phase selection;
- Rated for industrial temperature range;
- 450*mW* nominal power consumption at 12.5*Gbps*.



MLI Summary

- Utilization of MLI will result in:

  - Reliable data channel alignment on the receiver side of a serial link with no additional latency or overhead,

  - Stable half rate clock recovery on the receiver side by means of a simple clock multiplication technique (i.e. elimination of a complex CDR unit),

  - Double redundancy due to the requirement of only a single differential link needed to transport both clock and data (SpaceWire).

- Application Areas:

  - Low-latency interconnects.

    - *PCI, USB, and other standard bus extensions,*
    - *Scalable Coherent Interface (SCI) links,*
    - *Improved SpaceWire-compatible interconnects.*

  - Any SERDES product.

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Switching Fabric Based on Multi-Level LVDS Compatible RHBA Interconnect

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SF Block Diagram

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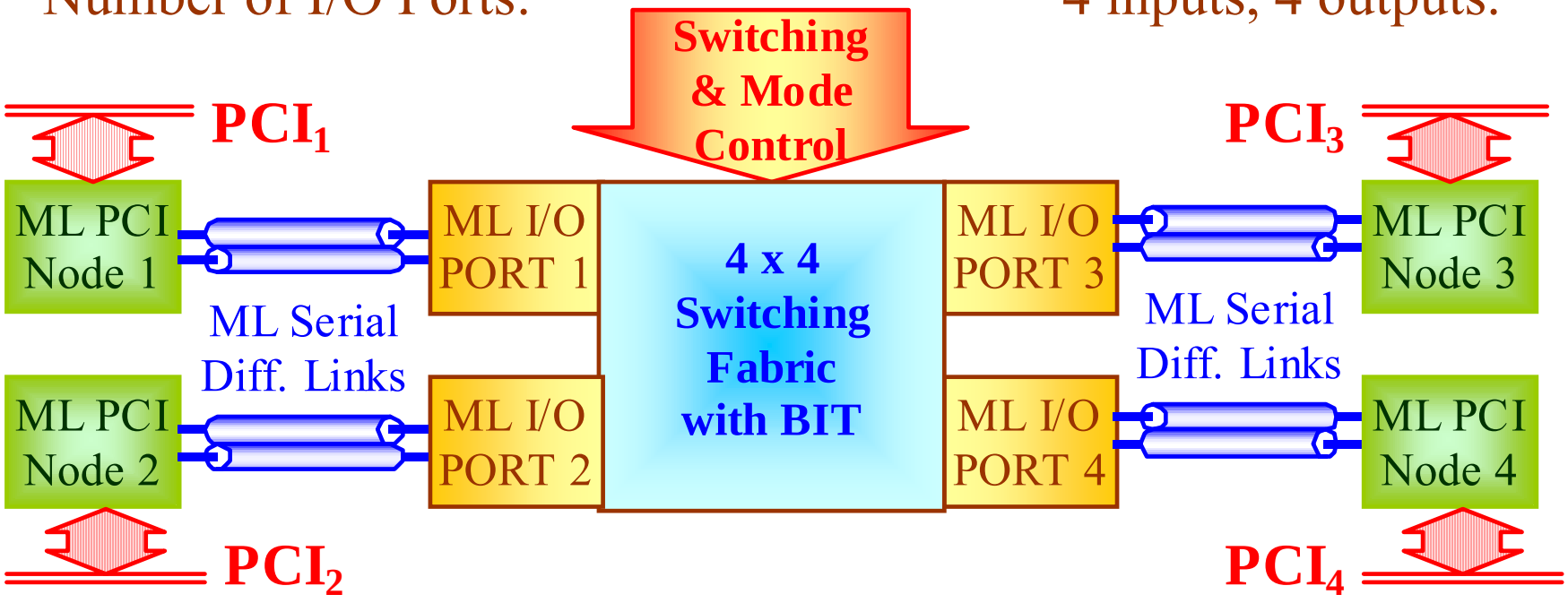
LS Interface:	cPCI, 32-bit wide, 33 MHz clock;
HS Interface:	ML LVDS-compatible, 1 Gb/s;
FIFO Depth:	8 bit;
Control Interface:	CMOS;
Number of I/O Ports:	4 inputs, 4 outputs.



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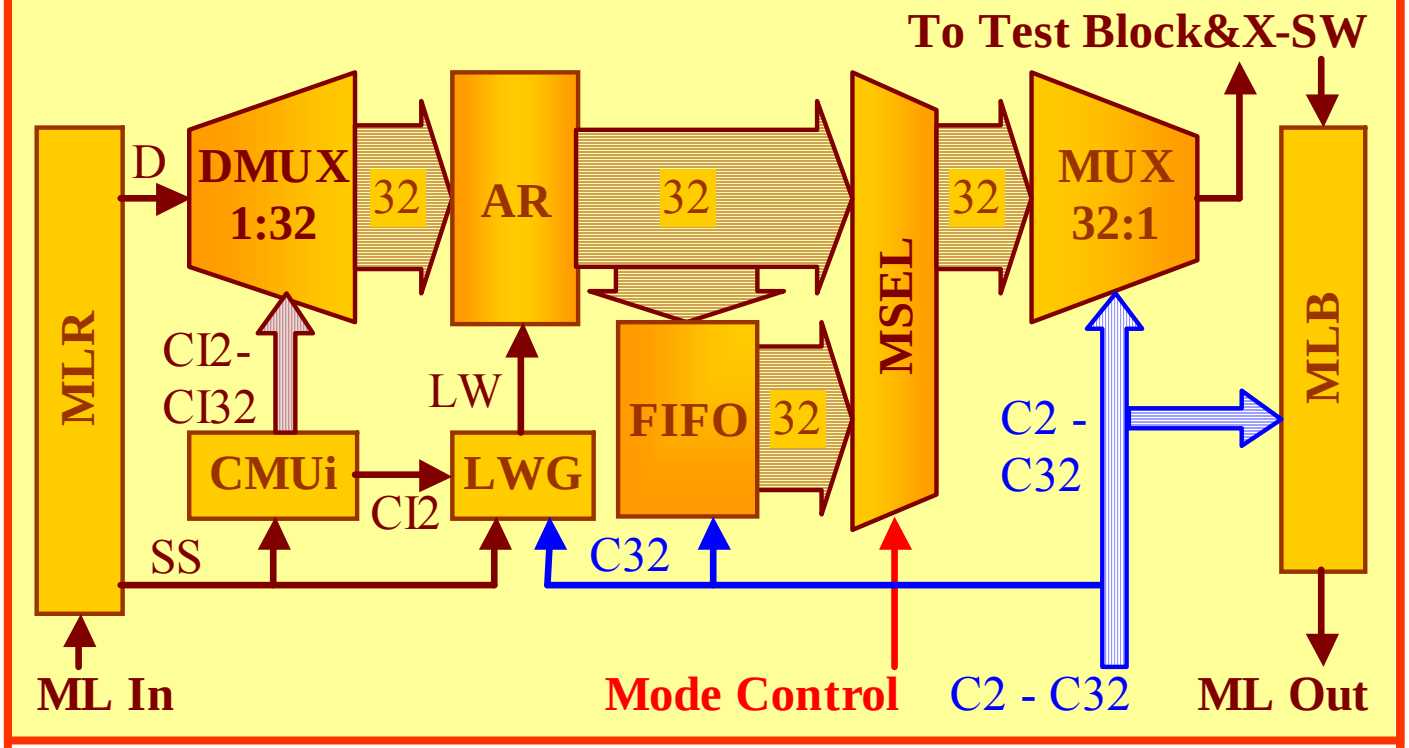
RHBA ML Transponder

Main Blocks:

- ***ML Deserializer:***
  - ML Receiver,
  - CMU internal,
  - DMUX 1:32;
- ***Alignment Block:***
  - Align Register,
  - LW Generator;
- ***Memory:***
  - FIFO,
  - Mode Selector;
- ***ML Serializer:***
  - MUX 32:1
  - ML Buffer.



Functions of the Blocks:

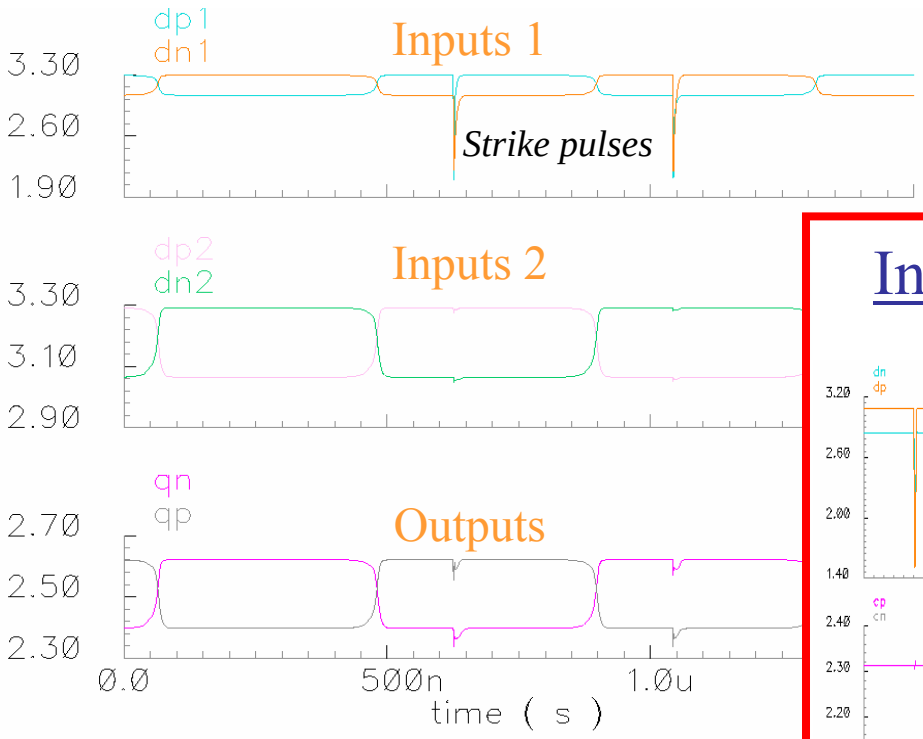
- *ML Deserializer* reconstructs clock signals and 32-bit parallel data from input serial bit stream;
- *Alignment Block* retimes the data by Local Write (LW) signal not coincident with I/O clocks;
- *Memory* stores the data temporarily and delivers either original or delayed data to the MUX;
- *ML Serializer* converts parallel data into serial bit stream with imposed Synchro pulses.

RH-by-Architecture

- Based on SiGe HBT CML cells;
- Utilization of logic functions for SEE/SEU mitigation;
- Lower speed/power/area penalty than standard TMV technique;
- 6 power levels from 14*μW/cell* to 1.85*mW/cell;*
- Up to 2.5*Gb/s* worst-case simulated speed;
- Complete RHBA library of standard and custom cells including:

  660MHz Ring VCO, PFD, and Charge Pump;
  I/Os, ML I/Os;
  D-Type Latch, DFFs, RSFFs
  Buffer and Emitter Follower;
  MUX2:1, AND, and XOR Gates.

Strike Effects Simulations

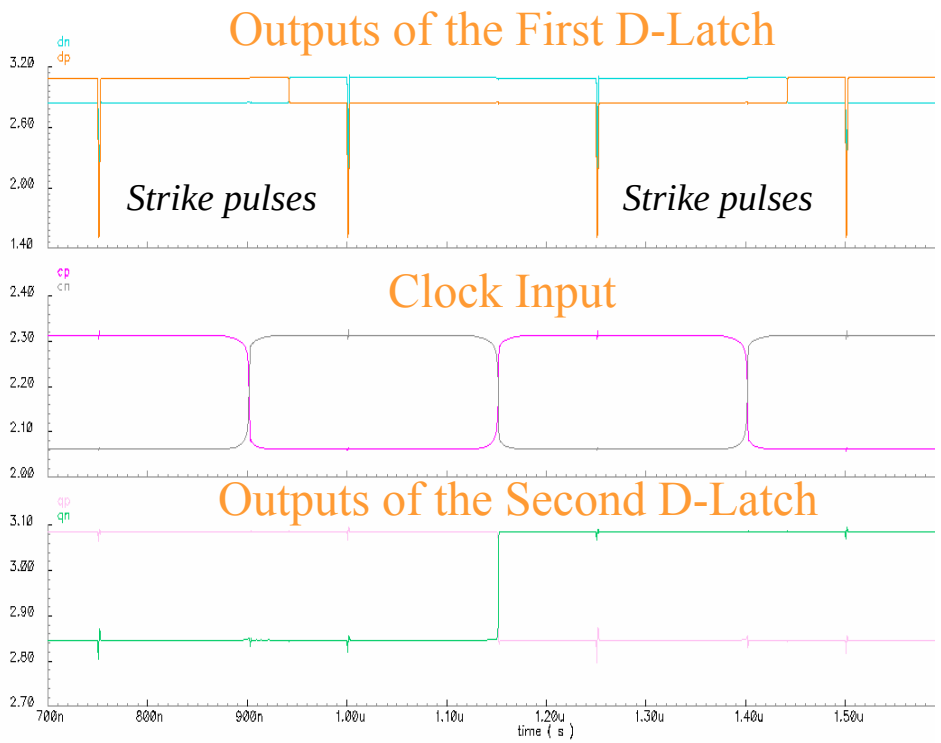


Inputs and Outputs of Dual EF

SEE model includes realistic current pulses at transistor level.

Provided by J. Cressler, GeorgiaTech

Inputs and Outputs of a Flip-Flop



Outputs of both EF and D-latch demonstrate negligible disturbance with a significant SEE-related impact at the inputs of the circuits.

Summary / Conclusion

- A dual, low power CMOS-to-LVDS IC solution has been presented that operates at GHz speeds with an improved level of TID protection. The IC contains switchable Data Strobing encoding/decoding circuitry that is fully Space Wire compatible and innovative I/O blocks.
- ADSANTEC has developed a novel multilevel interface (MLI) technology that significantly improves the performance of high-speed serial data links, specifically Space Wire interconnects, and has multiple fields of application.
- An innovative radiation hard by architecture (RHBA) library has been utilized to construct a ML transponder that is utilized in the presented switch fabric intended for cPCI bus extension.