# *SpaceWire* in Russia


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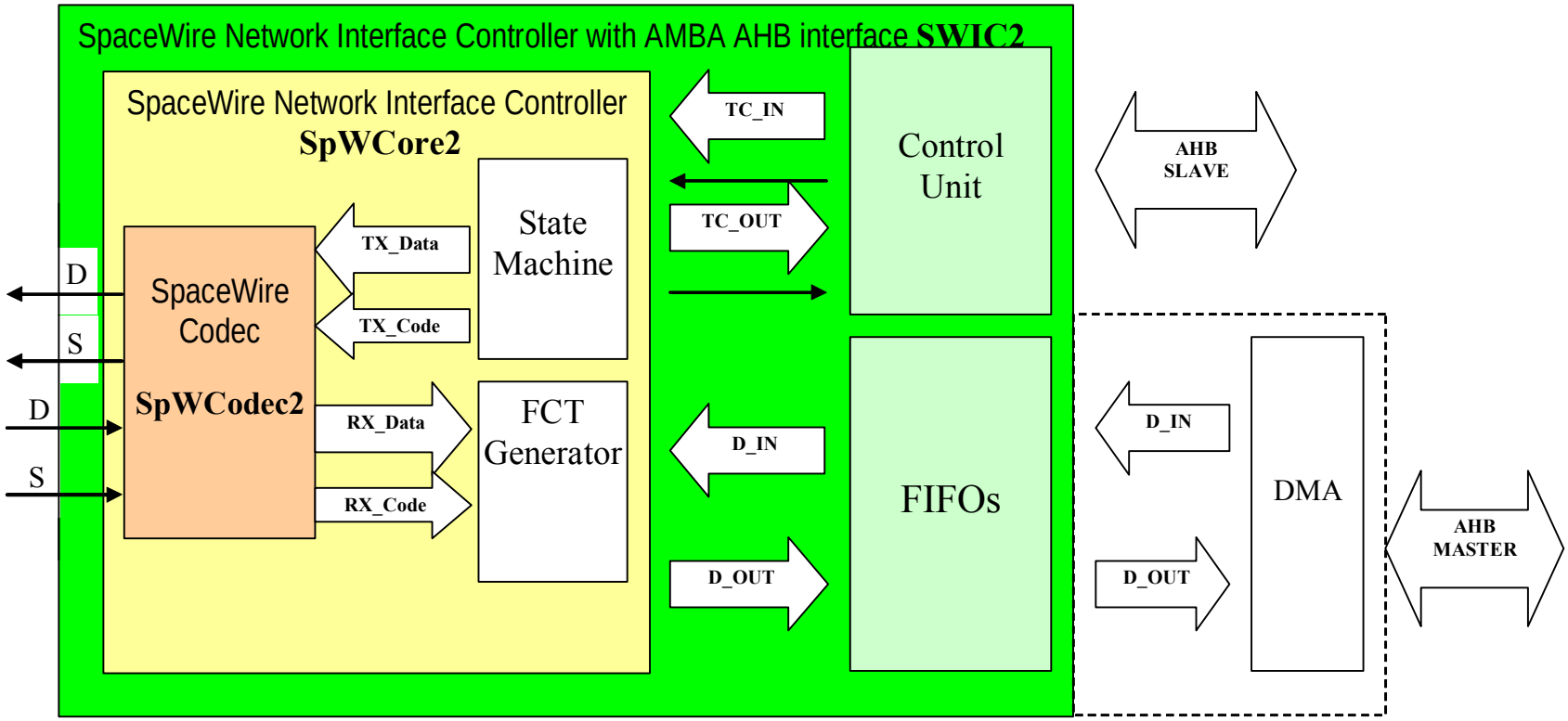
# SpaceWire implementation: IP-cores, chips, boards

| Class | Type | Code | Timescale |
|---|---|---|---|
| ***IP-cores*** | SpaceWire Codec IP-block | *SpWCodec2* | 2004 |
| | SpaceWire Network Interface Controller IP-core | *SpWCore2* | 2005 |
| | SpaceWire Network Interface Controller with AMBA AHB interface | *SWIC2* | 2005 |
| | SpaceWire multichannel communication controller bridge (FPGA implementation) | *MCB-SpW-F* | 2005 |
| ***Chips*** | MultiCore Terminal Controller with SpaceWire links | *MCT- 01* | 2006, Q2 samples, 2007 |
| | SpaceWire multichannel communication controller bridge (ASIC implementation) | *MCB-01* | 2006, Q4 samples, 2007 |
| | 16-channel SpaceWire routing switch | *MCK-01* | 2006, Q4 samples, 2007 |
| ***Boards*** | DSP module with SpaceWire links | *PCI104 SpaceWire Kit* | 2006, Q1 |

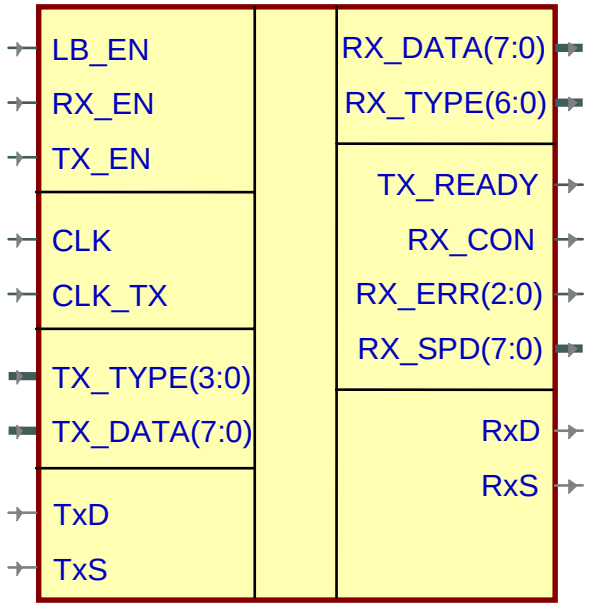
# Hierarchy of IP-blocks for SpaceWire



# *SpWCodec2*

## IP-block SpaceWire Codec

- High-speed duplex link: 5 Mbit/s to 400 Mbit/s in each direction (@ 0,25 µm )
- Completely synchronous interface (interface signals are fixed on ascending front)
- RX clock computation scheme (detection up to 800Mbit/s)
- LoopBack included
- The ratio of local and reception frequencies is 1:6
- Small number of triggers working on TX and RX clock

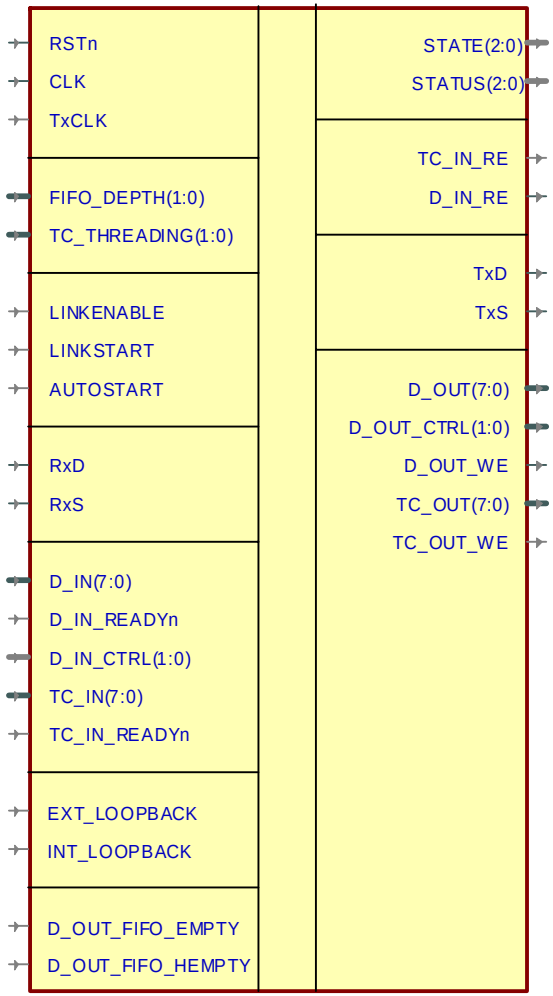



IP-block complexity:

- ASIC – 500 logic gates,
- FPGA – 250 LUT

# IP-core SpWCore2

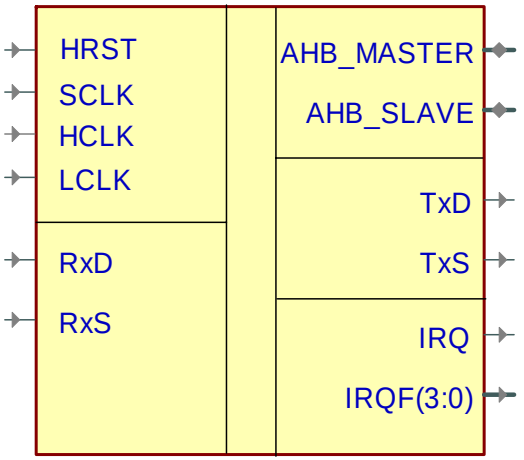
- High-speed duplex link:
  5 Mbit/s to 400 Mbit/s in each direction (@ 0,25 µm )
- Transmits/receives data packets, time codes and distributed interrupts signals
- Simple parallel interfaces with typical FIFO
- 2 levels of LoopBack
- Programmable crediting scheme depending on the sizes of the reception buffer (16, 32, 64 and 128 words)
- Completely synchronous interface (interface signals are fixed on ascending front)
- RX clock computation scheme (up to 800Mbit/s)




Compexity:
ASIC – 1100 gates, FPGA – 550 LUTs

# SpaceWire Network Controller *SWIC2*

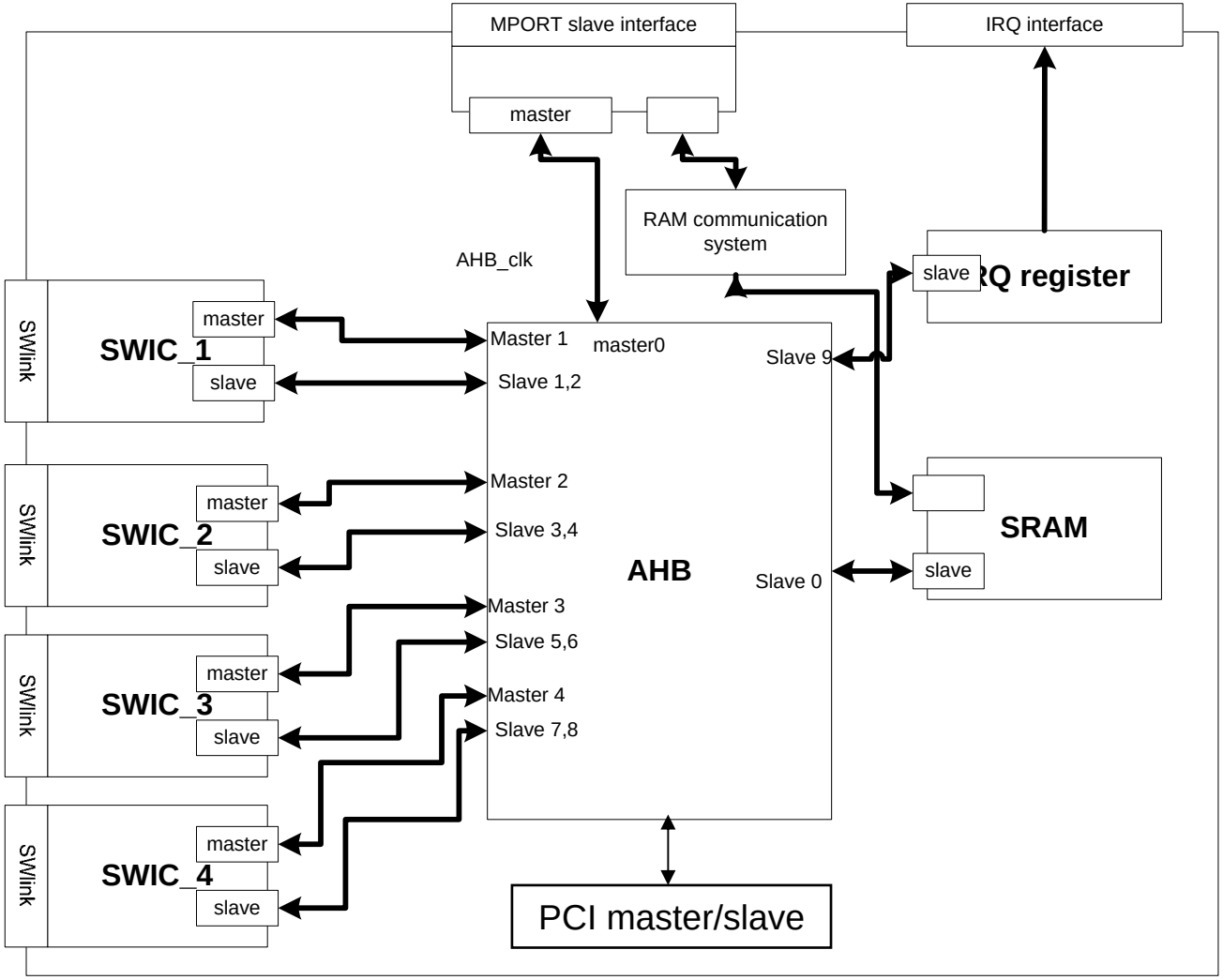
- 5 Mbit/s to 400 Mbit/s in each direction
  (@ 0,25 µm )
- Transmits/receives data packets, time codes and distributed interrupts signals
- 32-bit AMBA AHB bus interface (master/slave), 100MHz
- Parameterized internal FIFOs in both directions (8, 16, 32, 64, 128 words).
- DMA component, multi-channel
  (32-bit AMBA AHB master)
- 3 interrupts on the AMBA AHB
  (error in link, packet reception, time labels or distributed interrupts).
- 3 levels of LoopBack included
  (DS-codec, SpWCore2, Controller SWIC2)
- RX clock computation scheme




Compexity:
ASIC – 6300 gates,
FPGA – 3000 LUTs

# MCB-01

## SpaceWire multi-channel communication controller bridge

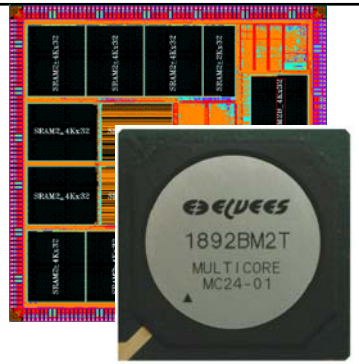


# *MCB-SpW-F*

## **SpaceWire multichannel communication controller bridge**
(FPGA implementation)

| | |
|---|---|
| SpaceWire channels | 4 |
| SpaceWire channel speed | From 2 Mb/s up to 400 Mb/s |
| External interface | 32-bit, 40 ns, SRAM-like |
| Internal buffer RAM | 16 Kbytes |
| FPGA type | Xilinx Spartan-3 1500 |

# Multi-core DSP chips *“ MULTICORE”*

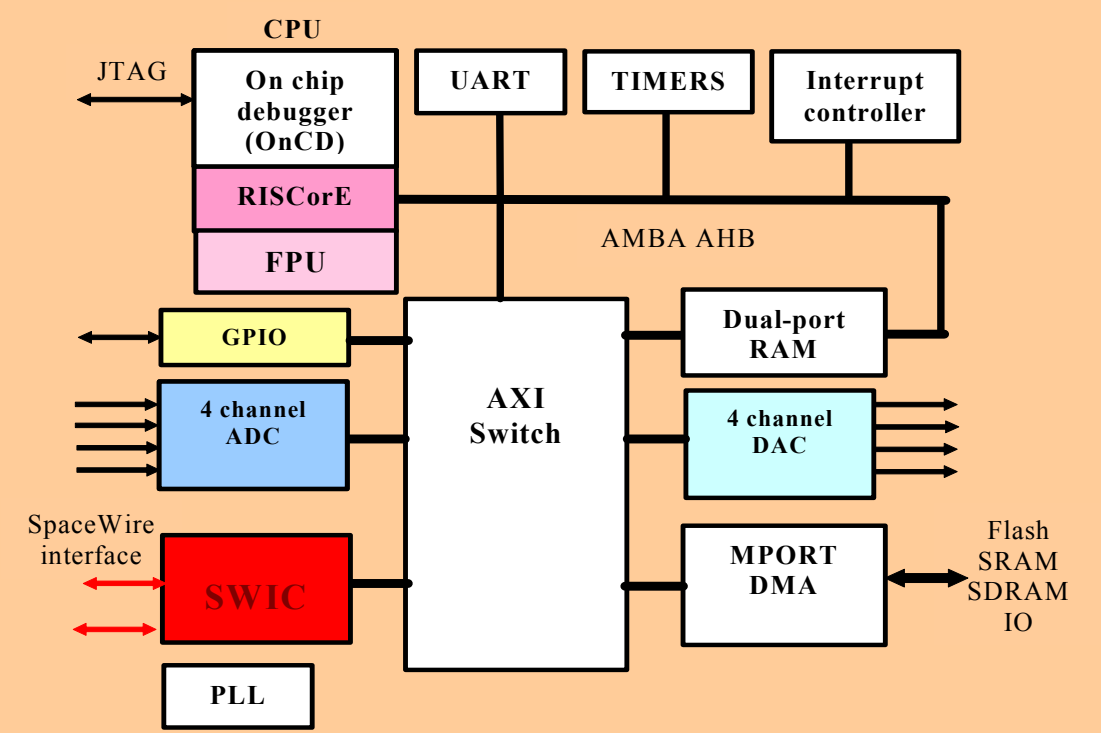
| market@elvees.com<br><br>WWW. ELVEES.RU<br><br>ЭЛВИС |  |  |  |  |
|---|---|---|---|---|
| **Multi-core chip (RISC+DSP cores)** | **1892BM3T (MC-12)** | **1892BM2T( (MC-24)** | **1892BM4Я/ 1892BM5Я** | **MCF- 0428,** (Test chip – MC-0128) |
| **Implementation technology, μm** | **0,25** | **0,25** | **0,25** | **0,18/0.13** |
| **Transistors, mln. /on-chip RAM (Mbit)** | **~18**<br>**2** | **~19**<br>**2** | **~26**<br>**3** | **65**<br>**~8** |
| **Multi-core chip, MIMD (RISC+*n*xDSP cores)** | **RISCore32** (MIPS32) + **1xDSP** (ELcore-14) | **RISCore32** (MIPS32) + **1xDSP (2SIMD)** (ELcore-14) | **RISCore32** (MIPS32) + **2xDSP**(ELcore-26) **(MIMD)** | **RISCore32** (MIPS32) + **4xDSP**(ELcore-28) **(MIMD)** |
| **CLK, MHz / Power (W)** | **100**<br>**(1.2)** | **100**<br>**(1.4)** | **120**<br>**(1.8)** | **400**<br>**(6.5/3.3)** |
| **Performance:**<br>**8b, Int ,** MOPs<br>**16b Int,** MOPs<br>**32b, float, (IEEE754),** Mflops | <br>**1800**<br>**800**<br><br>**300** | <br>**3600**<br>**1600**<br><br>**600** | <br>**8640**<br>**3840**<br><br>**1440** | <br>**57600**<br>**25600**<br><br>**9600** |
| **Package** | **PQFP240** | **HSBGA292** | **HSBGA416** | **HSBGA, > 600** |
| **Production** | **2004** | **2004** | **2005** | **2007** |

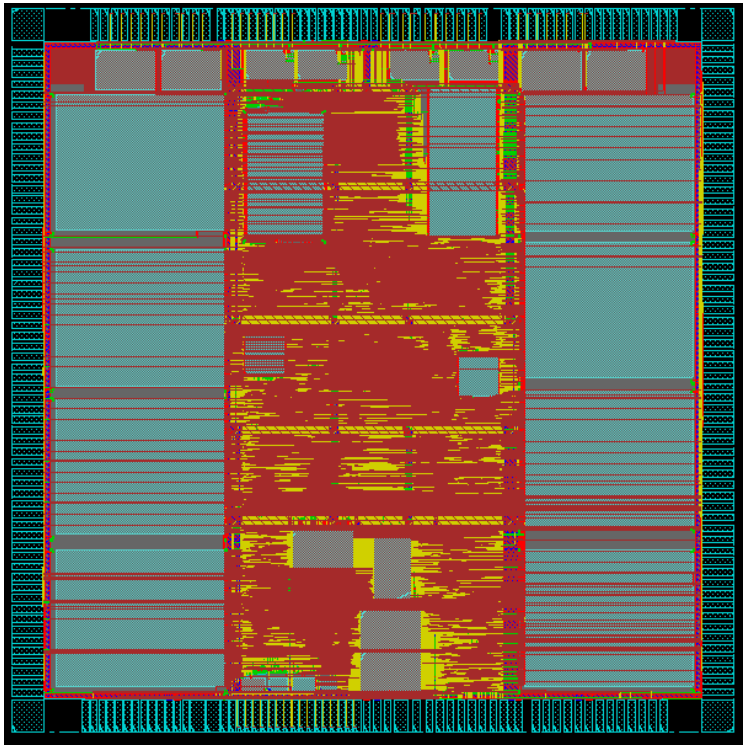
# Development Kit and Software Tools for *"MULTICORE"* DSP chips

*MCStudio*


# MCT- 01

## MultiCore Terminal Controller with SpaceWire links



**9.5x9.5 мм²**
**CMOS, 0.25 µm**
**3.3B**

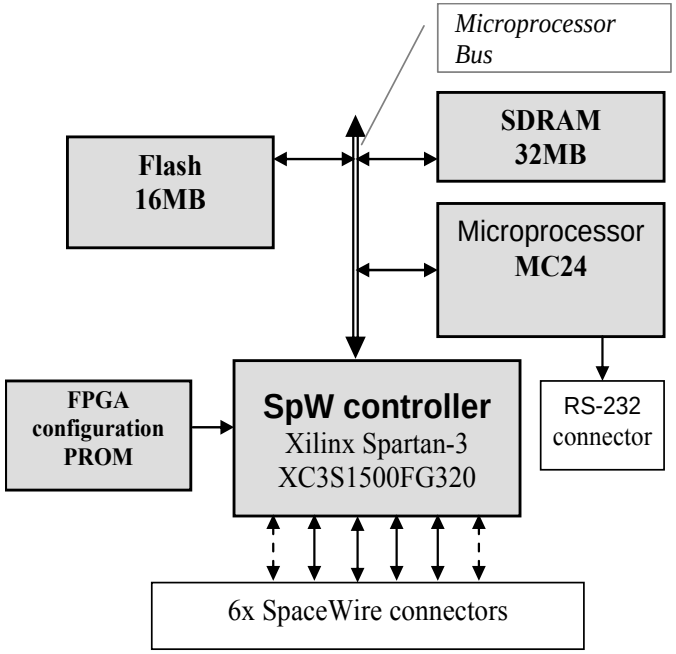
**Engineering samples**
**2Q 2006.**

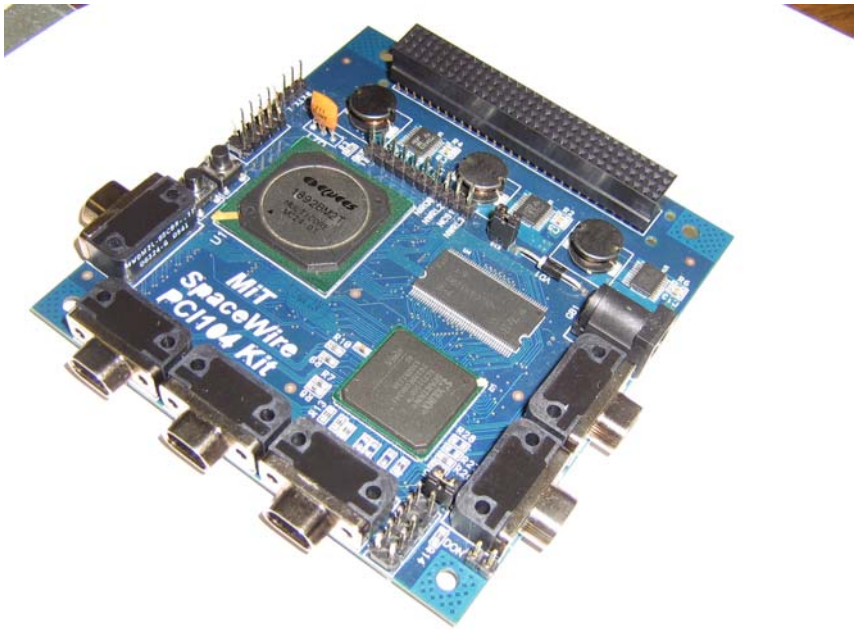
# PCI104 SpaceWire Kit

The one-board high performance DSP module:
- a ready-made building block

- for SpaceWire-compatible EGSE systems
- for on-board distributed & parallel space data systems prototypes with high-speed SpaceWire communication technologies.

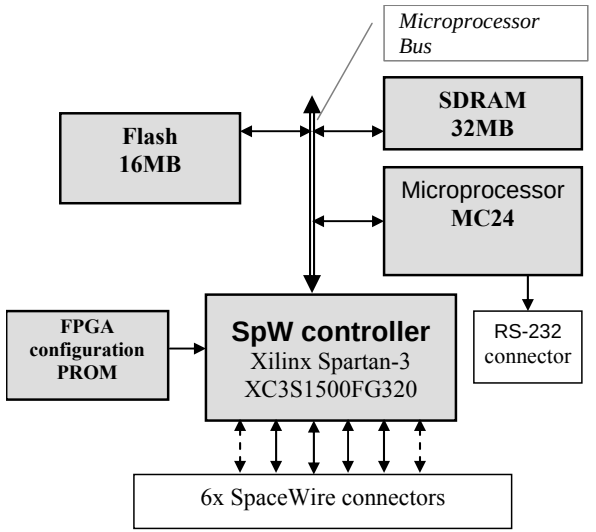
PCI104 form-factor



# PCI104 SpaceWire Kit

| | | |
|---|---|---|
| SpaceWire links | Number of links | 4 - 6 |
| | Rates | 2 to 400 Mb/s, duplex |
| Processor | Type | 1892BM2T ("*MultiCore-24*") |
| | Features | Double core (RISC+DSP)<br>On-chip RAM (3 blocks)<br>RISC core – MIPS32 arch. |
| | Performance | up to 600 Mflop |
| RAM | Capacity | 32 MBytes |
| | Type | SDRAM |
| ROM | Capacity | 16-64 MBytes |
| | Type | Flash |
| CPU bus width | | 32 (8 for ROM) |
| Other interfaces | | RS-232<br>EJTAG |
| Power supply | | 5 V |
| Power consumption | | 10 W max. |
| Software | | MCStudio Tools for *MultiCore-24* programming<br>Linux<br>SpW links driver |



# *MCK-01*

## 16–channel SpaceWire routing switch

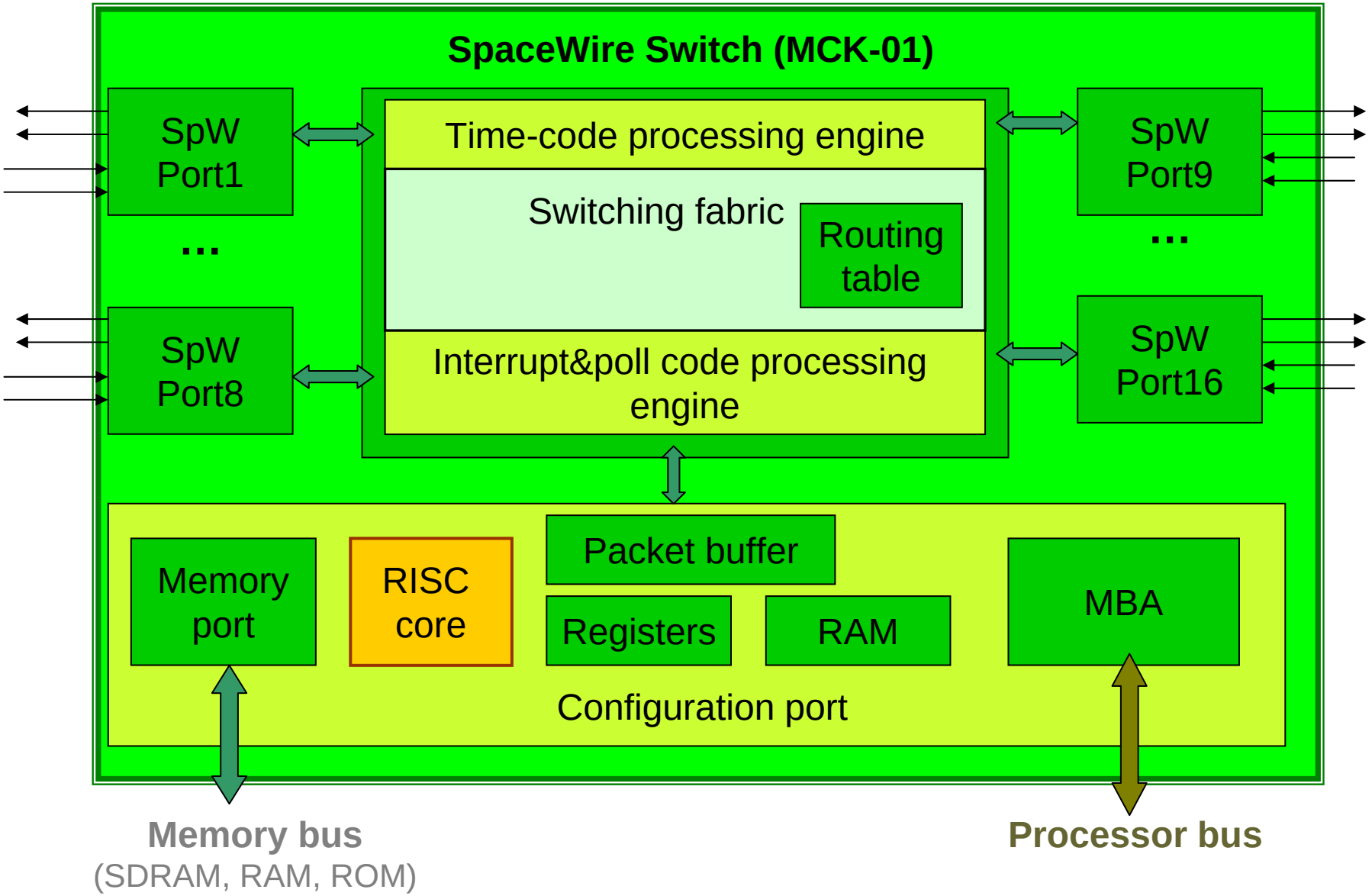
- Supports signal, symbol, exchange, packet, network protocol stack levels
- Advanced non-blocking internal switching fabric
- Supports adaptive routing
- Supports multicast routing
- Provides time-codes distribution in compliance with the ECSS-E-50-12A SpaceWire standard
- Provides interrupt codes and poll codes distribution in compliance with the project of the second part of the ECSS-E-50-12A SpaceWire standard
- Includes the internal RISC core for configuration, monitoring and network administration purposes

**Interfaces**:

- 16 full-duplex SpaceWire interfaces
- Transmission rate of each interface from 5 Mb/s to 400 Mb/s; can be set independently for every of 16 links
- Parallel interface to external static memory
- Parallel SRAM-like interface to external RISC processor (includes masked interrupt signal)

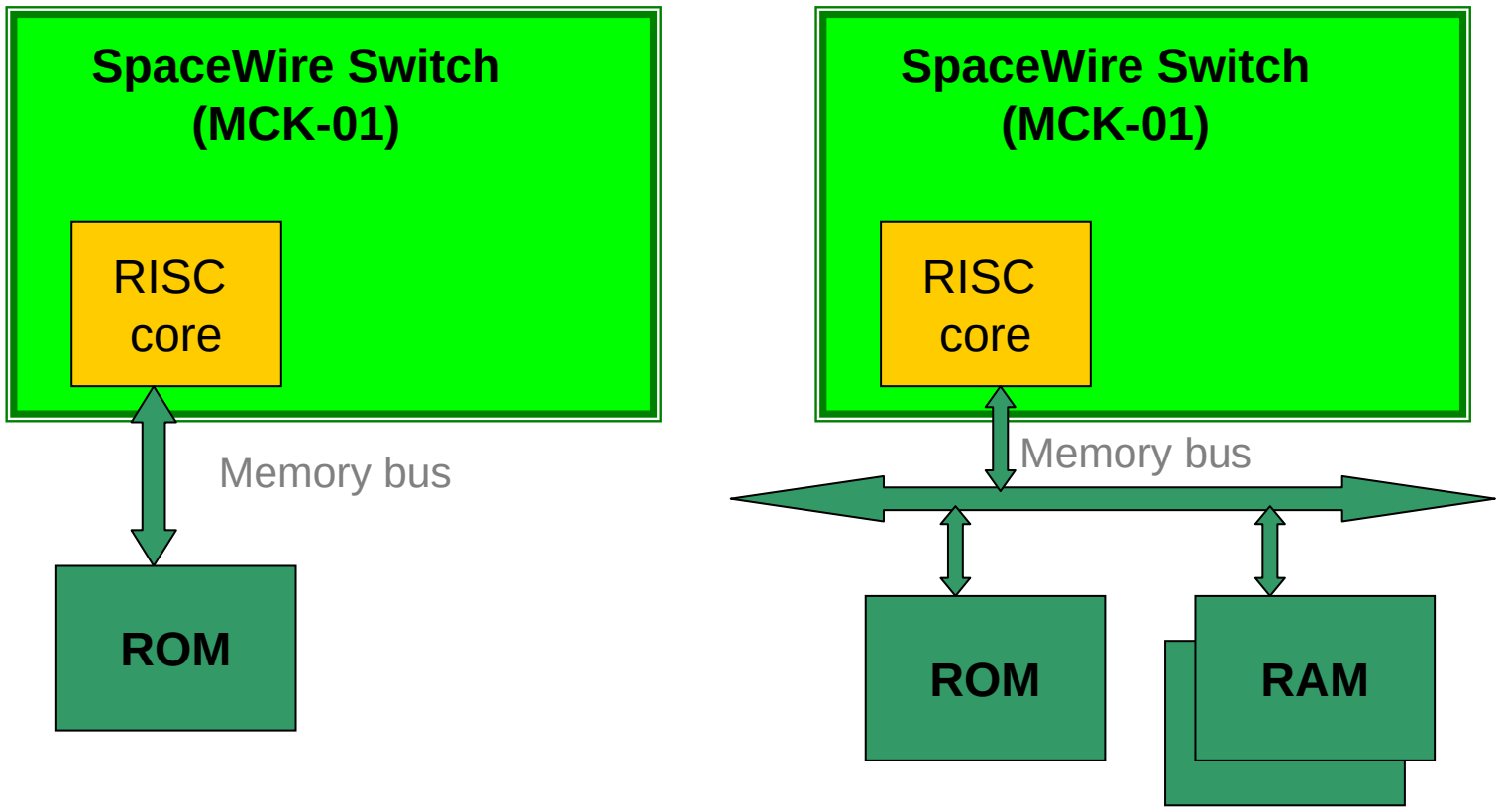
# *MCK-01*

SpaceWire routing switch



# *MCK-01* applications

(without external processor)



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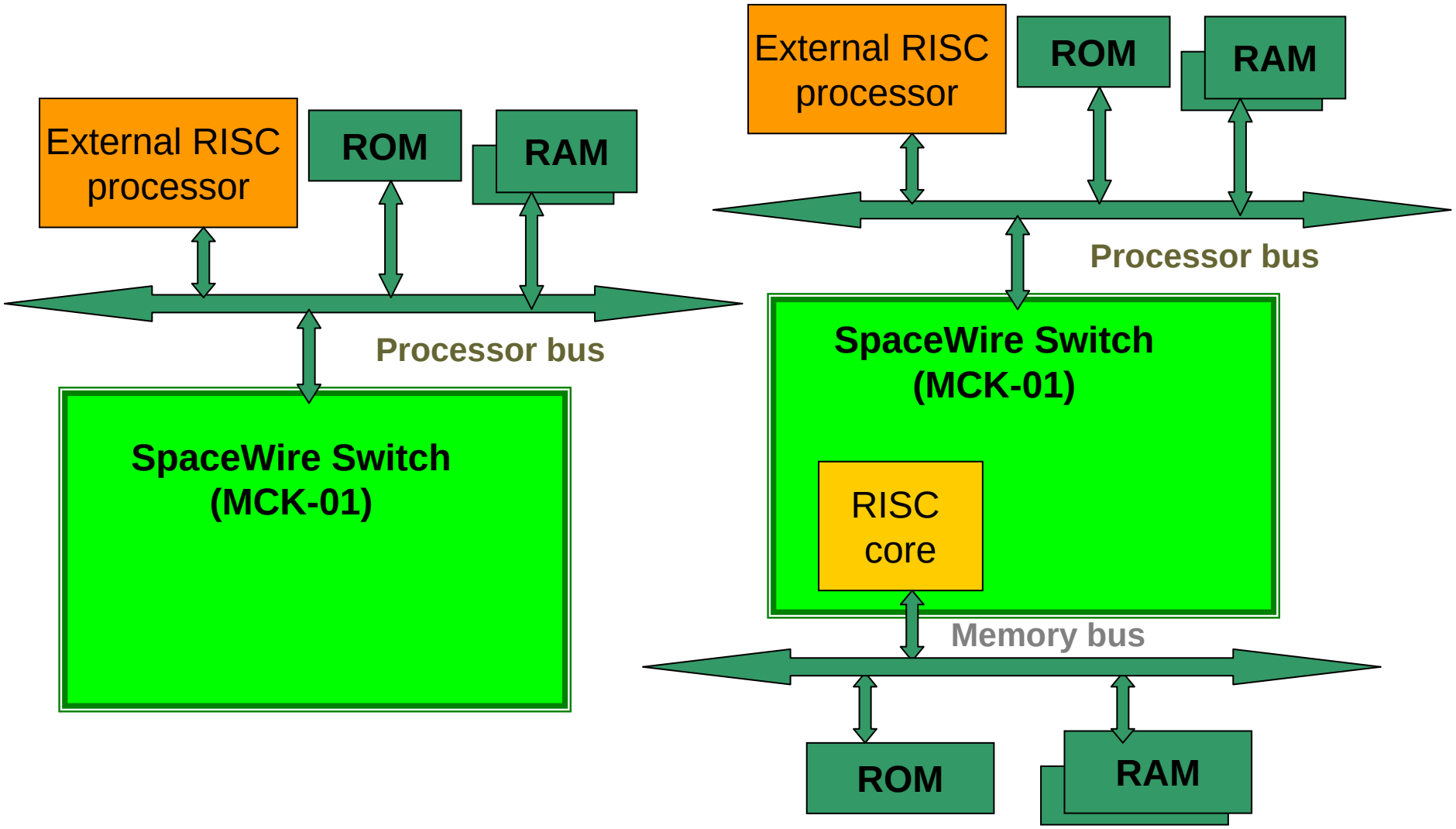

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# Latest news:

- The Federal Space Agency of Russian Federation is to apply officially in support of the SpaceWire technology

# *Thank you!*