VPC2
A generic SpaceWire-RMAP I/O module for space cameras

SpaceWire working group 6

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ESTEC

Summary

- VPC2 concept and performances objectives
- Global architecture
- VPC2 breadboard
- SpaceWire RMAP interface
- First results of a breadboard with a TH7834C CCD detector
- VPC2 flight model and associated product line

VPC2 concept and performances (1)

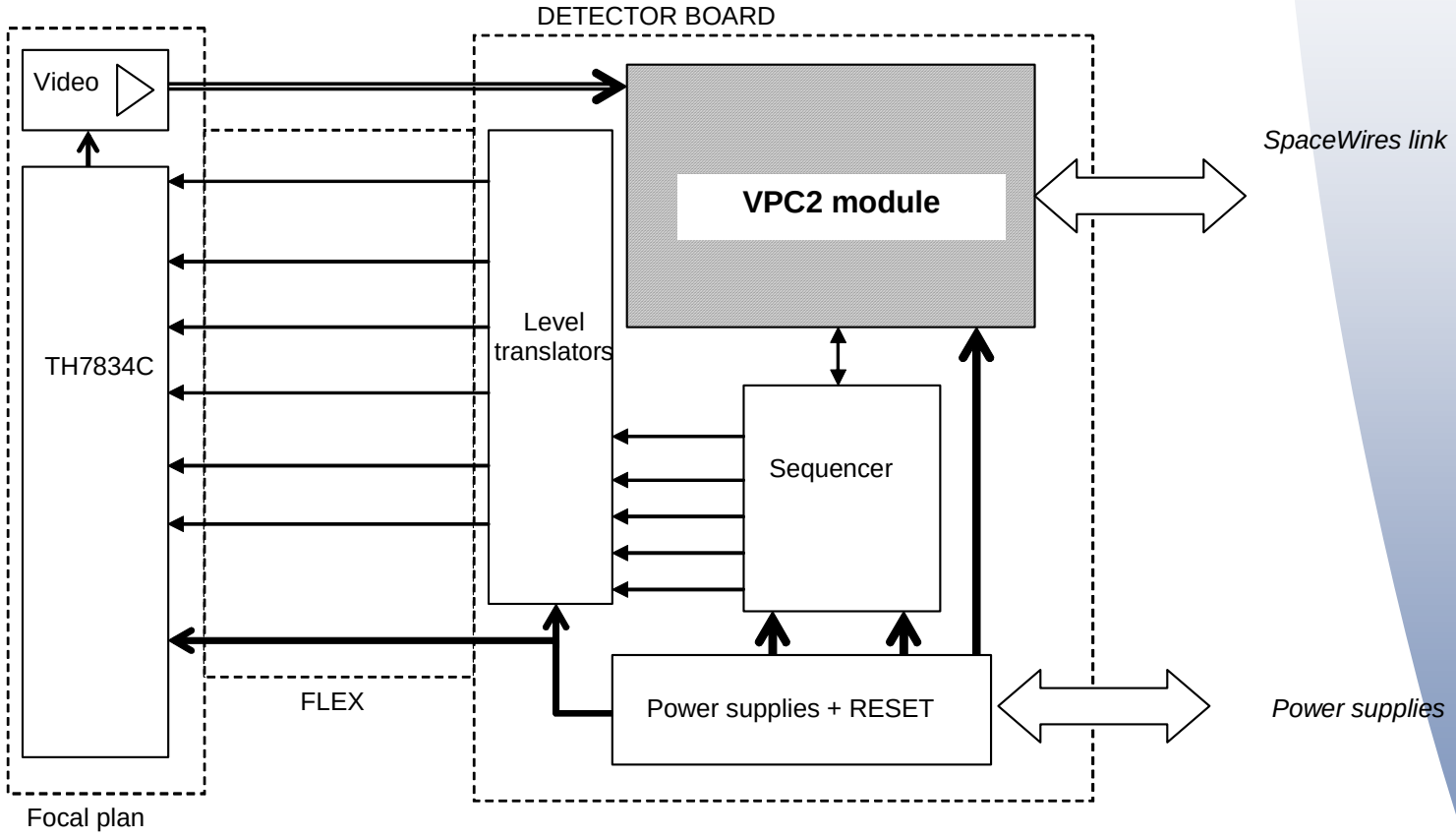
- Propose a ready to use module to interface a wide range of electro-optical detector (CCD, APS, HgCdTe...) with a SpaceWire network using the RMAP protocol.

- This module fulfils the following functions:
  - ✓ Video acquisition (2 video inputs):
    - CLAMP
    - CDS or single sampling
    - Offset correction
    - Digital conversion
  - ✓ Multiplexing with 4 house keeping
  - ✓ RMAP protocol
  - ✓ Interface with the SpaceWire network

- Data and control transit exclusively through a single SpaceWire connection

VPC2 concept and performances (2)

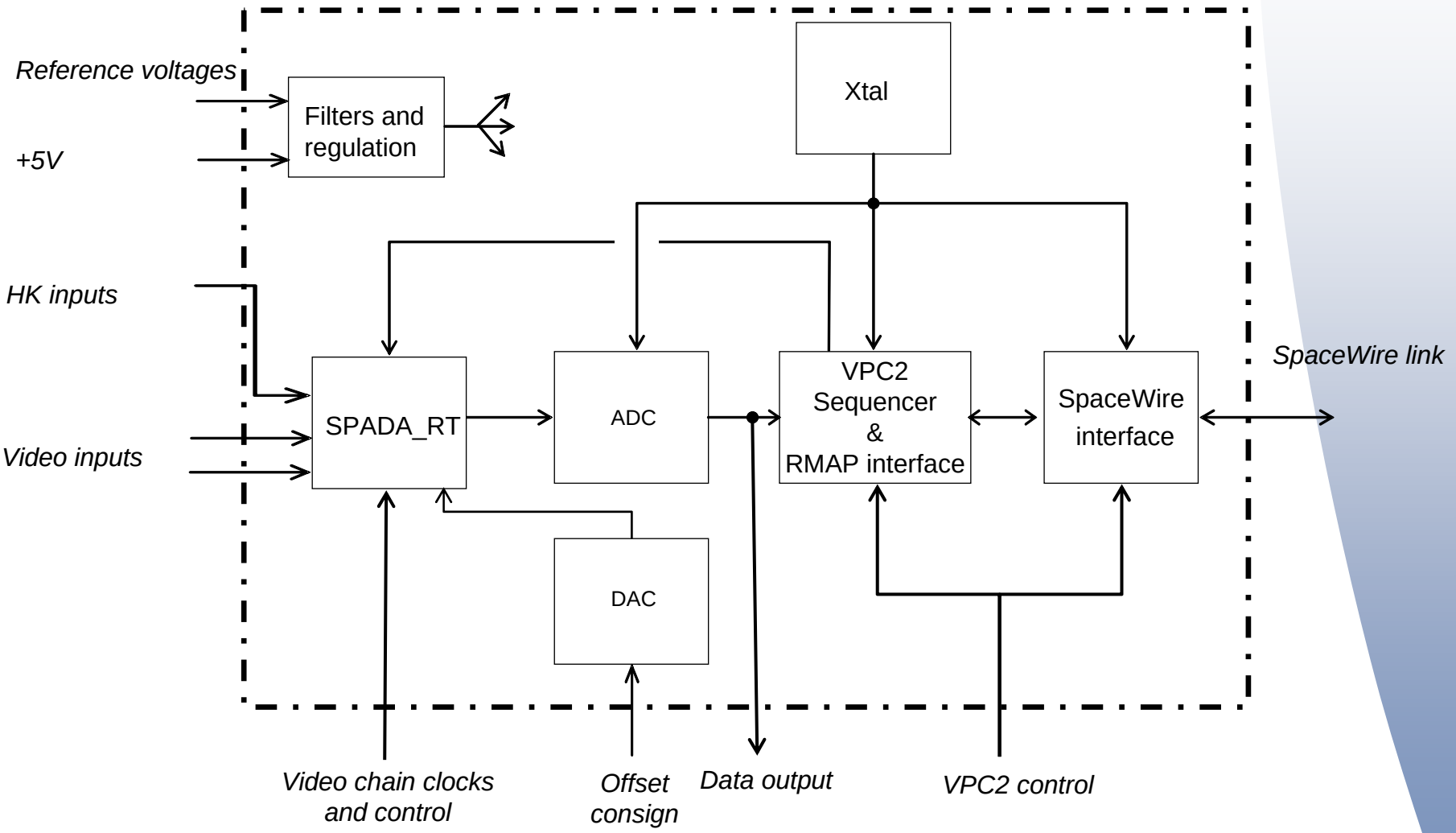
- Example of architecture



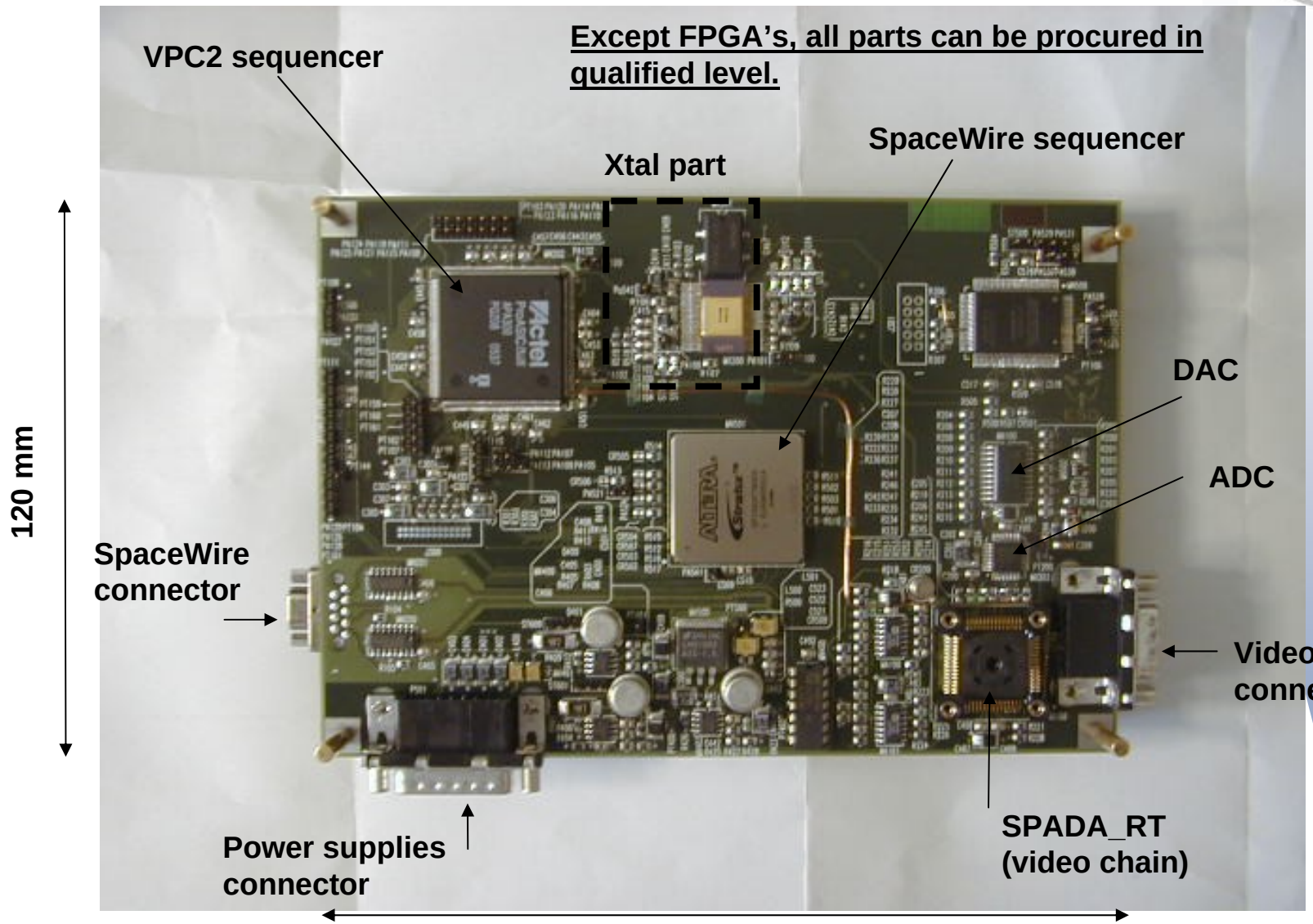
VPC2 concept and performances (3)

Pixel frequency	Settable from 100KHz to 3MHz
Data conversion frequency	12MHz (stable)
Conversion accuracy	14 bits
ENOB	12 bits
Analog treatments	CLAMP CDS or single sampling (programmable) Programmable gain from 1V/V to 8V/V Offset correction (12 bits)
Analog input	2 fully differential video inputs 4 single ended house keeping inputs
Analog input range (video)	+/- 2V
Input bandwidth	> 35MHz
Gain error	< 1%
Power supplies	+5V
Power consumption	< 1.5W (1W typ.)
Radiometric temperature range	0°C / +30°C

VPC2 architecture



VPC2 breadboard photo (1)

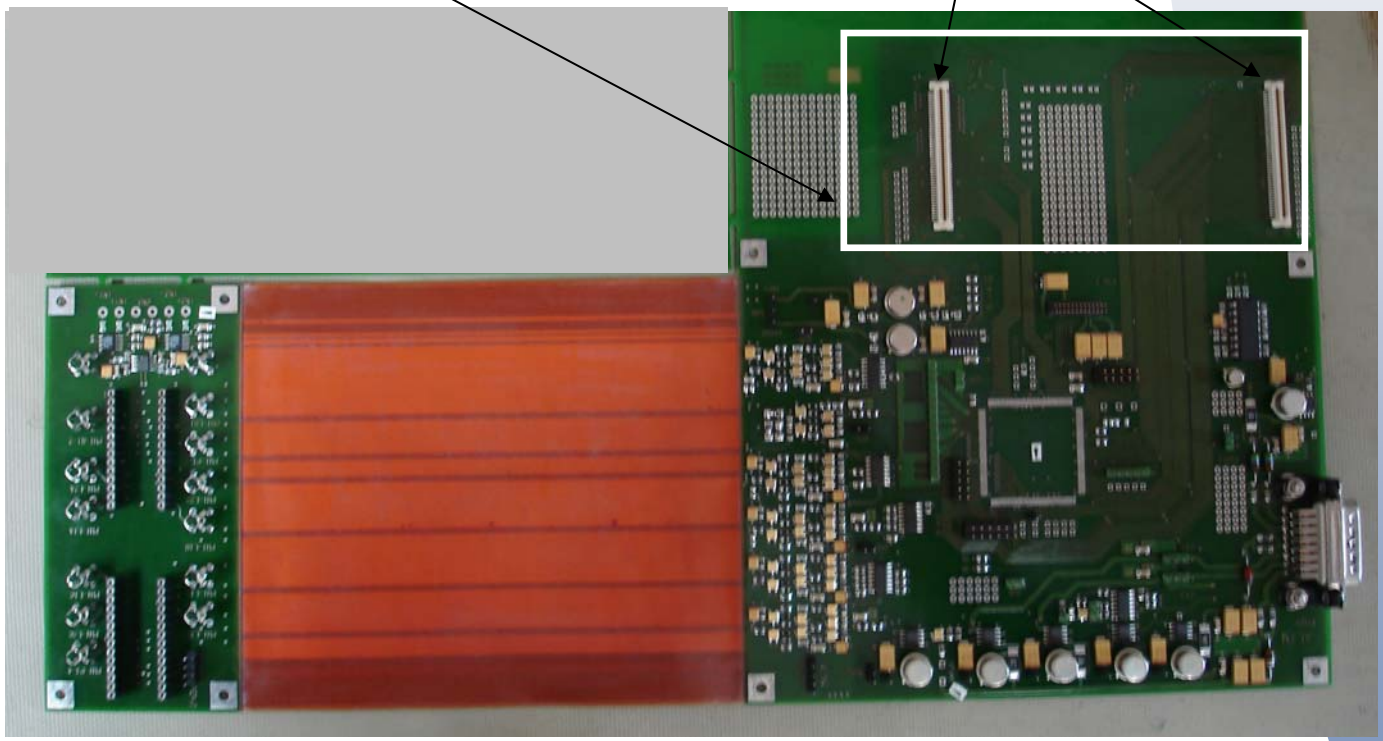


VPC2 breadboard photo (1)

The acquisition module is plugged on the detector board via 2 board to board connector (2x128 pins)

Print of the VPC2 acquisition module board

Detector board

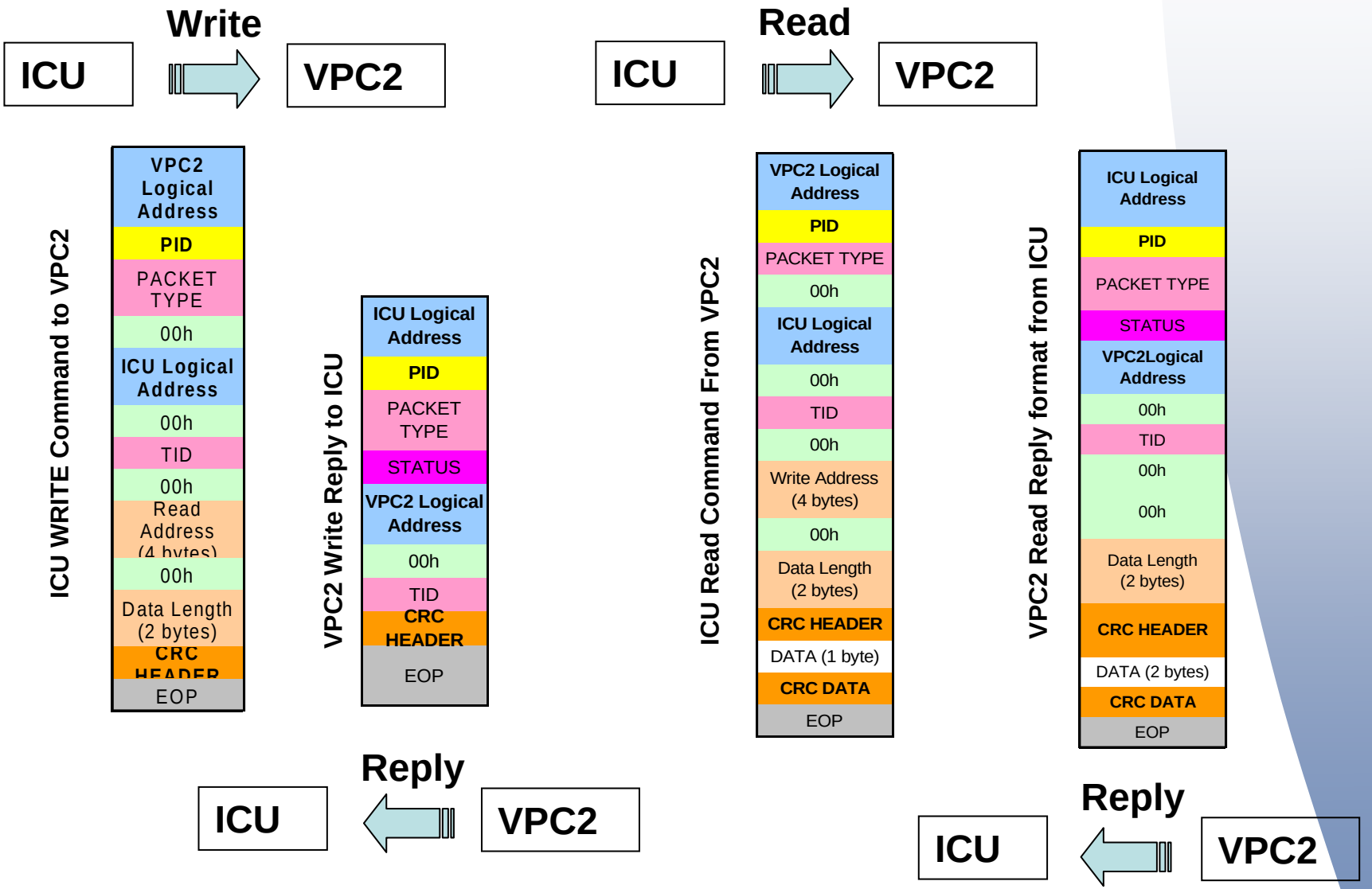


SpaceWire RMAP interface

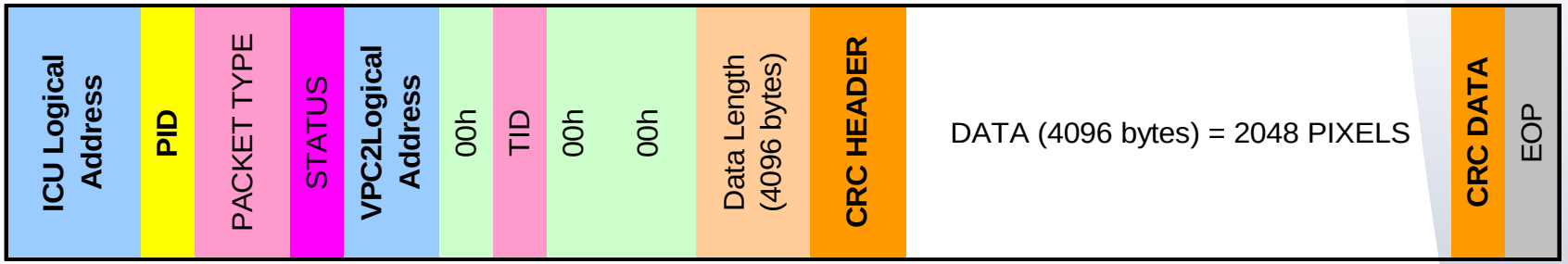
- Spacewire ECSS-E-50-12A
- ESA IP core (UoD) VERSION 1.4
- RMAP protocol
- Spacewire and VPC2 baseline 100 Mbits/s
- Configuration of VPC2 Analogue Chain
- Store video samples in memory with RMAP packets
- No embedded processor

SpaceWire RMAP management

RMAP FRAME FORMAT



RMAP VIDEO FRAME FORMAT



RMAP VIDEO FRAME :

- 4113 bytes Packet
- Correspond to 2048 pixels
- Video Packet protected by CRC

- 6 packets are needed to acquire one image of 12000 pixels

SpaceWire RMAP PERFORMANCE

- Up to 144 Mbits/s in SDR (Absolute maximum Rate)
- 51 Mbits/s measured for a 3 Mhz video of 12000 pixels image

- FPGA RMAP SPACEWIRE : 3300 Logic Cells
- 3 FIFOs
- Internal Clock Frequency : 24 Mhz and 144 Mhz

- Clocks are delivered by RADCLOCK (AEROFLEX component)

RMAP issues

- CRC very useful for frame integrity and for debug
- TID field not use for our application
- ICU CRC computation should be designed in Hardware due to timing reason

- Spacewire RMAP is easy to implement in hardware with no need of using embedded processor

First result with a TH7834C detector

- TH7834C detector:
  - ✓ Linear CCD detector used for the SPOT5 instrument
  - ✓ 12000 pixels
- This detector is used in 2 outputs.
- Results are given for T=30°C

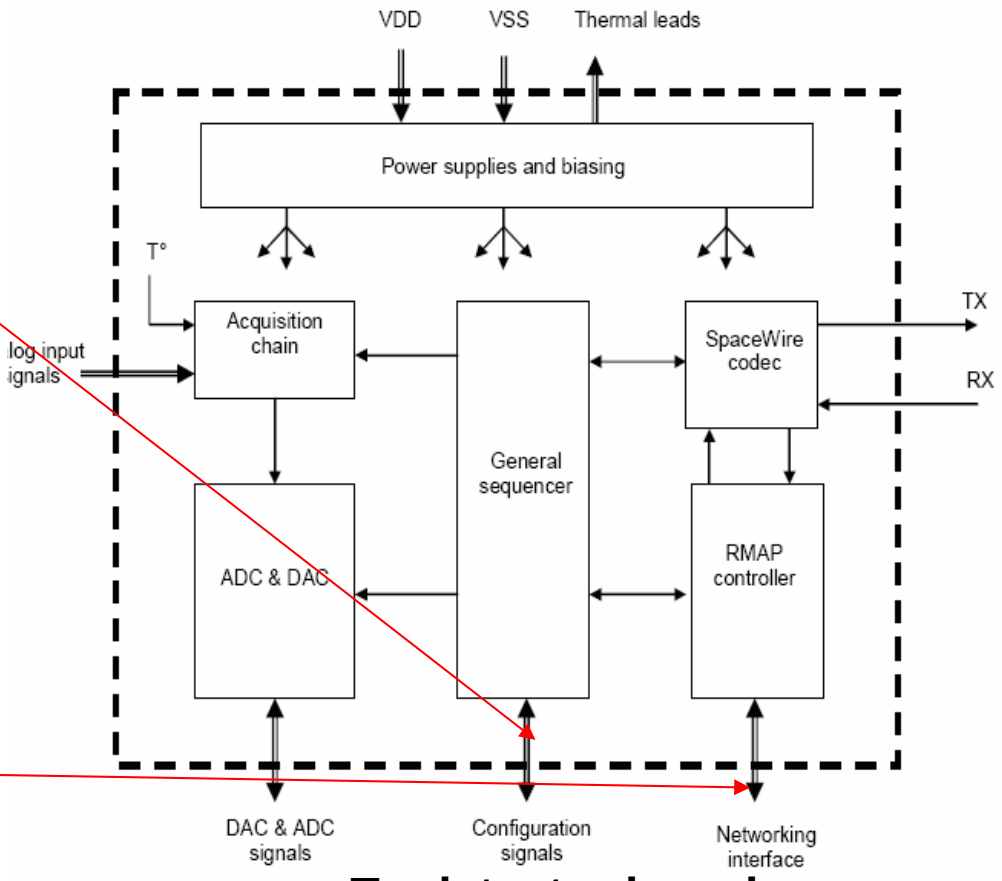
RMS noise	<9.5LSB(RMS)
Non linearity at unity gain (70% of the full well)	~0.8%
Pixel frequency	3 MSPS
Integration time dynamic	4ms – 40ms

VPC2 flight model and associated product line (1)

- From this breadboard, SODERN will propose a flight model.
- This flight model is smaller (130mm x 70mm) and has less pin count (128) than the breadboard.
- SpaceWire sequencer, VPC2 sequencer and RMAP management are included in a single FPGA (AX1000 / AX2000).
- A complete documentation is available.

Interface User

- Interface User is between VPC2 flight model board and DETECTOR parts
- 2 interfaces in fact :
- 1/ for Detector configuration register (interface similar to microprocessor)
- 2/ for RMAP frame (fifo like interface)



To detector board

VPC2 flight model and associated product line (2)

Issued from the VPC2 development, a complete product line dedicated to space instrumentation is now available

- **VPC2 board**
- **Hardened technology:**
  - ✓ **60KRad(Si) / latch-up threshold > 65Mev/mg.cm² / ESD > 4.5KV(HBM)**
  - ✓ **Complete digital and analog library**
  - ✓ **Can be use with a classical design kit (HYPER Silicon suite) or with a "netlist-to-layout" flow, where the front end is design with common software (PSPICE) and SODERN SODERN assumes the back-end, the manufacturing and packaging administration**
- **SPADA_RT ASIC:**
  - ✓ **The VPC2 video chain is now available in component form**
- **A wide range of Space Electronic Component:**
  - ✓ **Op Amp, voltage / current reference, video amplifier…**