SpaceWire
Remote Terminal Controller

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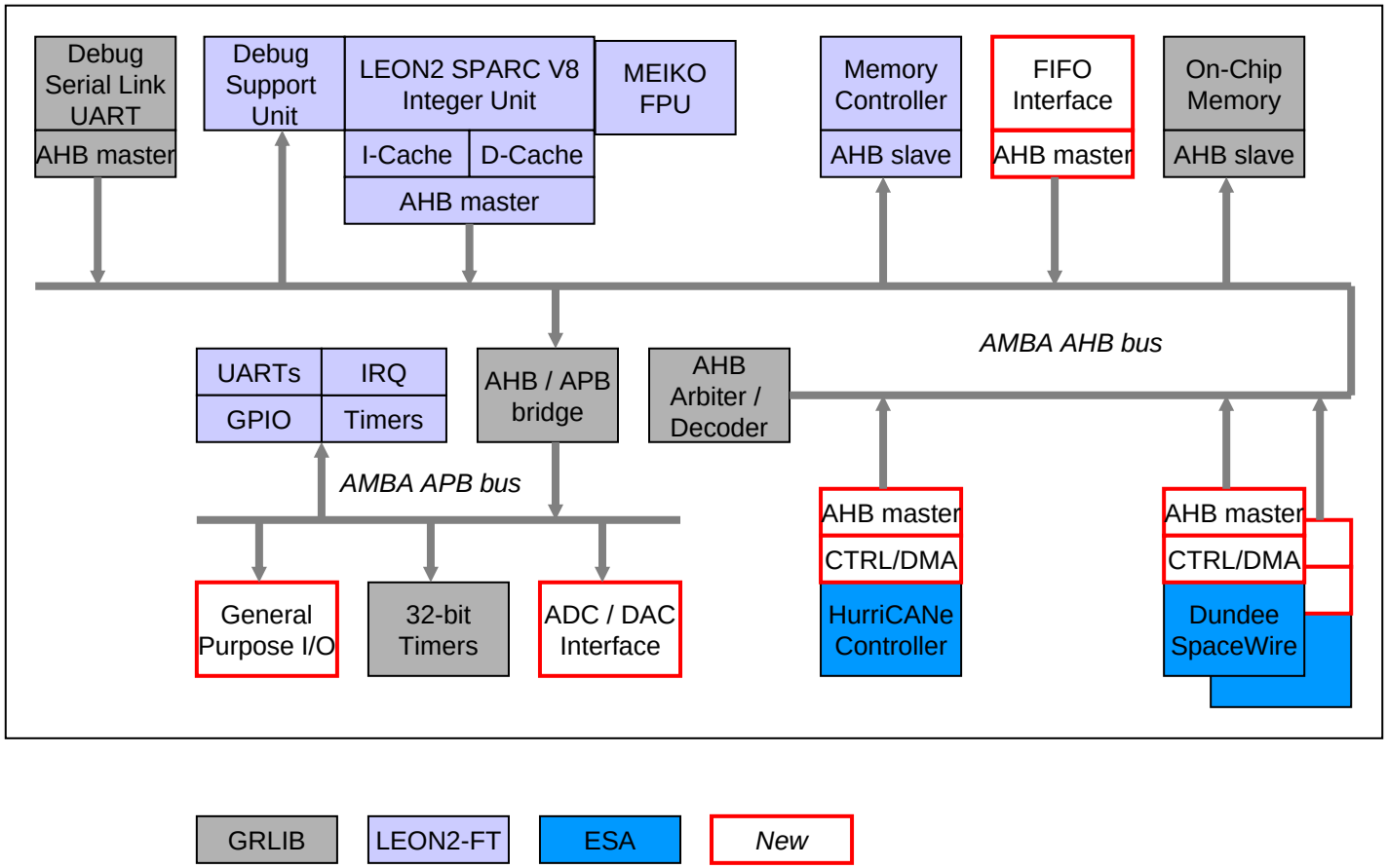
Saab Ericsson Space

SpaceWire RTC contract

- ESA study
- Prime Contractor: Saab Ericsson Space
- Subcontractor: Gaisler Research
- Foundry: ATMEL, ATC18RHA 0,18µm process, multi-project wafer run

SpaceWire RTC overview



For more details, see the RTC presentation from SpaceWire WG4 meeting

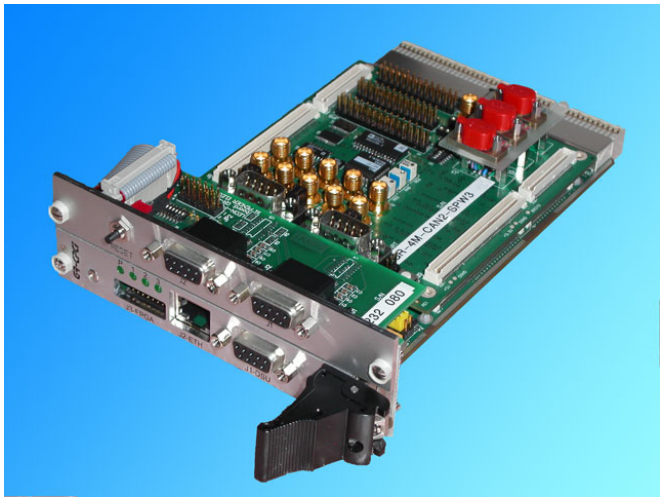
Saab Ericsson Space

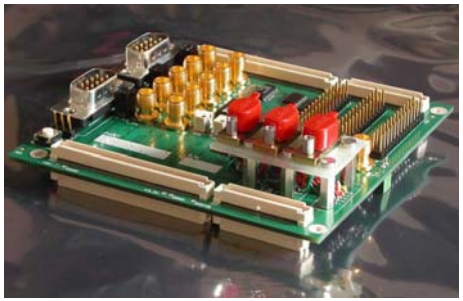
SpaceWire Module Functions

- SPW CODEC IP from ESA (UoD) used
- RMAP support (Read & Write block)
- Extra Rx and Tx Channels controlled by S/W
  - Packet handling (multiple packet, buffer limits, alignment, debug)
  - Sending RMAP commands, separating header and data, CRC generation for header (data CRC is generated in H/W)
  - Reception of Transfer protocols not supported in HW.
- Time Code, Receive and transmit
- 200 Mbit/s capability, @ 100MHz SpW Clock, i.e. DDR only
- I/F to AMBA bus

FPGA Validation

- Based on a Gaisler Research GR-CPCI-XC2V Development Board
- Additional mezzanine modules to house CAN, SpaceWire, FIFOs, UARTs and analogue I/O
- Device operation
  - System incl. Leon: 30 MHz
  - SpaceWire: 100 MHz, no DDR
- Tests performed
  - Individual function validation
    (CPU, SpaceWire, CAN, FIFO, Timers etc)
  - Five different system applications
    Full speed transfers on FIFOs + SpaceWire links (2)
    Full speed transfers + Dhrystone in CPU
    Full speed transfers + Stanford in CPU
    Full speed + Dhrystone + CAN + ADC/DAC + GPIO





FPGA Validation results

- CPU performance:
  - Comparable to AT697 test results
- SpaceWire link performance:
  - Two bidirectional links running at max speed giving only 2.2% NULL tokens
- FIFO operation:
  - FIFO operation at 1,5% overhead average when writing from on-chip RAM, up to 39% overhead when writing from off-chip RAM
- Mixed operation:
  - SpaceWire: <3% NULL tokens
    FIFO: 150 – 200 Mbps
    CPU: <30% reduction in performance when running I/O

RMAP implementation experience

- Error handling interpretation:
  - Some cases of interpretation difficulties have been seen:
    - EEP received instead of EOP with correct packet length
      Report early or late EEP, i.e. cargo too large?
    - Read command packet that includes data
      Report Late EOP (cargo too large) or consider it as general header error, i.e. no reply?
    - Verified write with both misalignment error due to odd number of data and too much data
      Report buffer overrun or authentication error due to the misalignment?
    - Others that have now been included in Draft E
      E.g. how to differentiate between commands supported by the standard and commands not implemented by the node
- CRC generation
  - The examples in the RMAP draft E uses LSB to the left (or as MSB for all normal use) according to Figure 15 in the standard. Especially for the C code example this causes some confusion as data has to be reversed before using the table. The examples should be improved and a clarifying figure useful
  - Header CRC generation in S/W and data CRC generation in H/W was found to be the most practical solution

Remaining work

- ASIC synthesis
- Prototype manufacturing
- Prototype validation