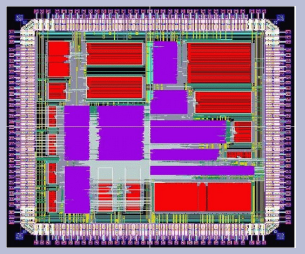
Gaisler Research



Spacewire Development Activities at Gaisler Research

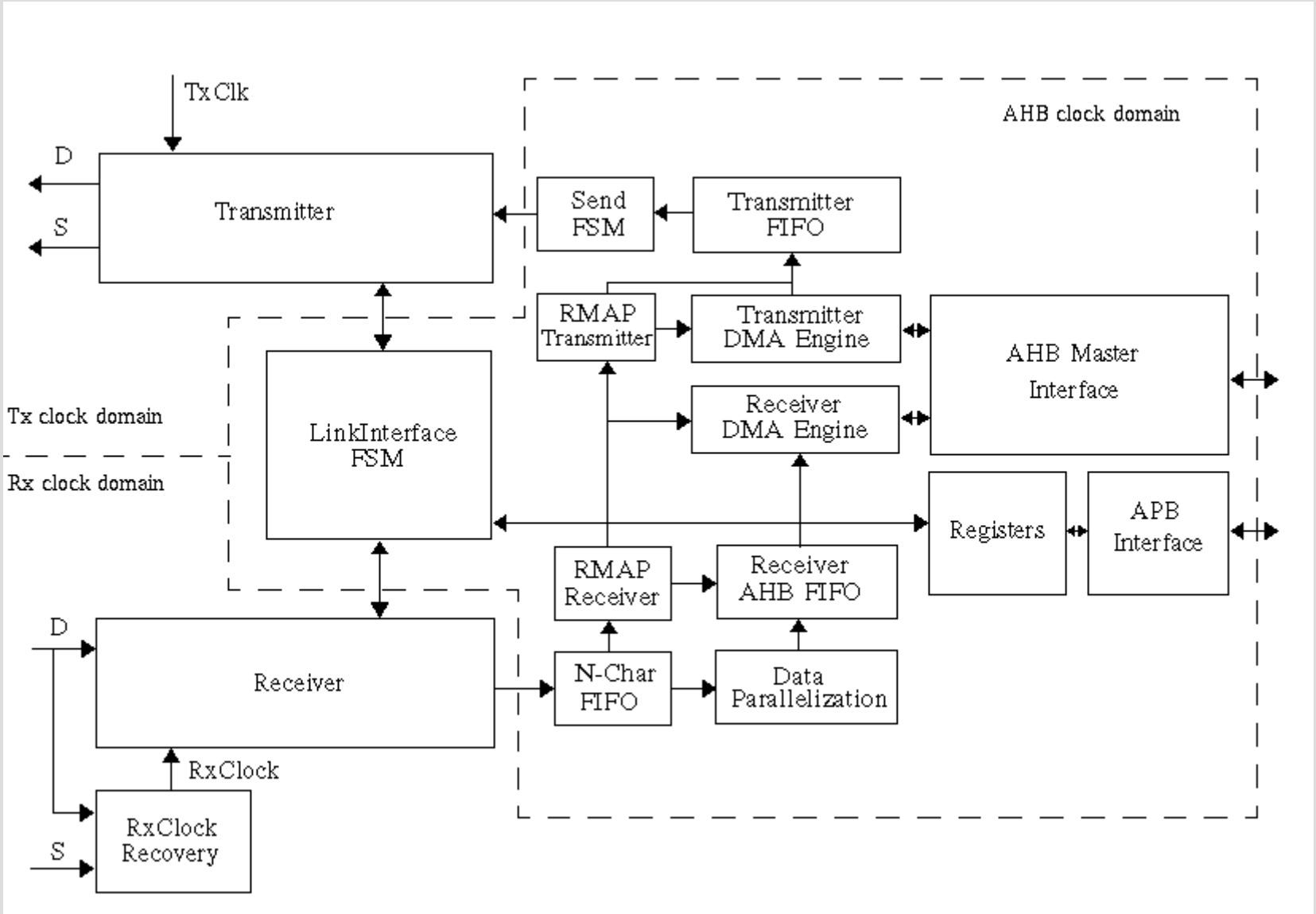
Introduction

- GRSPW Spacewire IP Core
  - Feature
  - Area
  - Performance
- Spacewire / Ethernet Bridge
  - Functionality
  - Usage

GRSPW Spacewire Core

- Developed from scratch on internal funding
- Contains SPW front-end and AMBA AHB Master back-end
- Data is transferred with DMA using chained descriptors for maximum throughput and minimum CPU overhead
- Includes full RMAP protocol handling (draft C/E)
- Extensively configurable through VHDL generics
- Inherently portable through GRLIB technology API
- Available as separate IP core or integrated in GRLIB

GRSPW Architecture



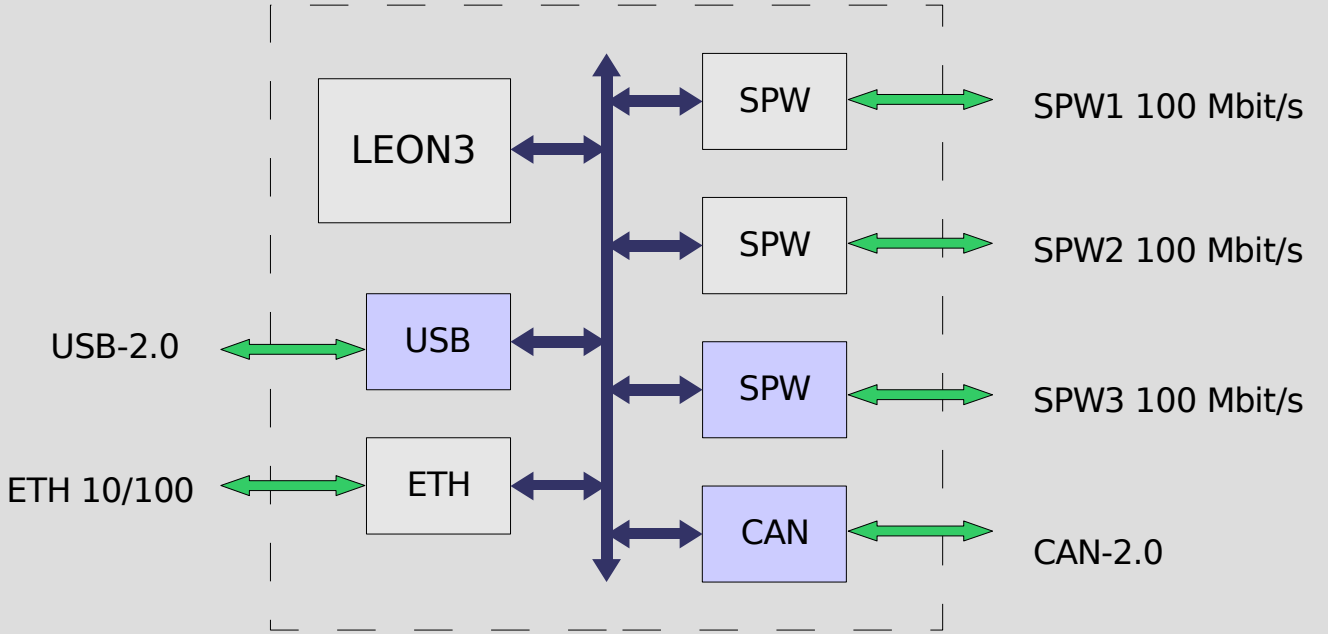
GRSPW Design Features

- Full fault-tolerance against SEU effects (FIFO/RMAP)
- Low area: 1,800 - 3,400 LUT on Virtex2
- Robust and portable design style
  - Fully synchronous, no multiplexed clock, no DDR
- High performance
  - 100 MHz on Actel RTAX
  - 250 MHz on Virtex2
  - 400 MHz on ATC18

GRESB Spacewire/Ethernet Bridge

- Low-cost Spacewire / Ethernet bridge
  - 100 Mbit ethernet (TCP/IP)
  - 3 x 80 Mbit SPW links
- Uses standard BSD socket() interface
- Built-in web browser for status and configuration
- Options with USB-2.0 and CAN-2.0

GRESB Architecture



GRESB Housing

GRESB Usage

- Simple communication from any host on the network, using the O/S independent BSD socket() interface.
- Each SPW uses separate TCP ports for receive/transmit
- Transmit bit rate individually programmable
- Fixed or dynamical IP address (DHCP)
- Used with GRMON to debug LEON systems over RMAP
- Used for validation tests during RTC development
- Used by several projects (ESA and Industry)