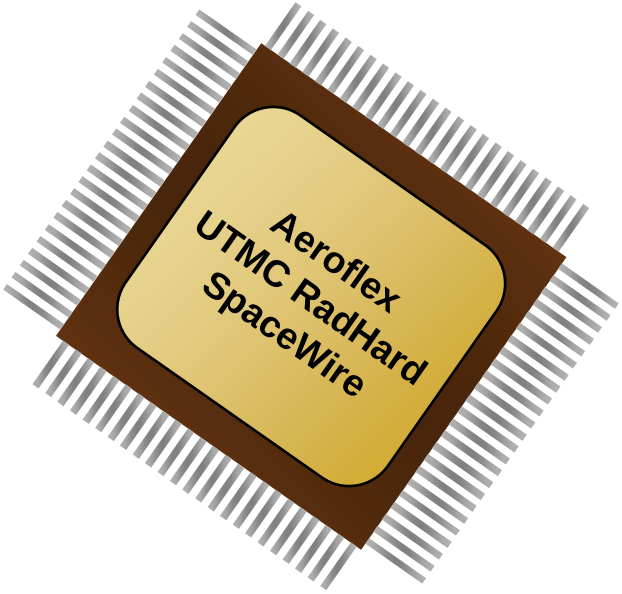
SpaceWire

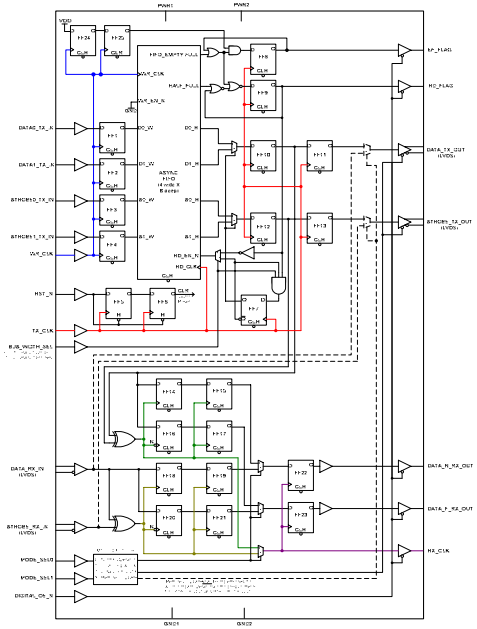
Interface Products

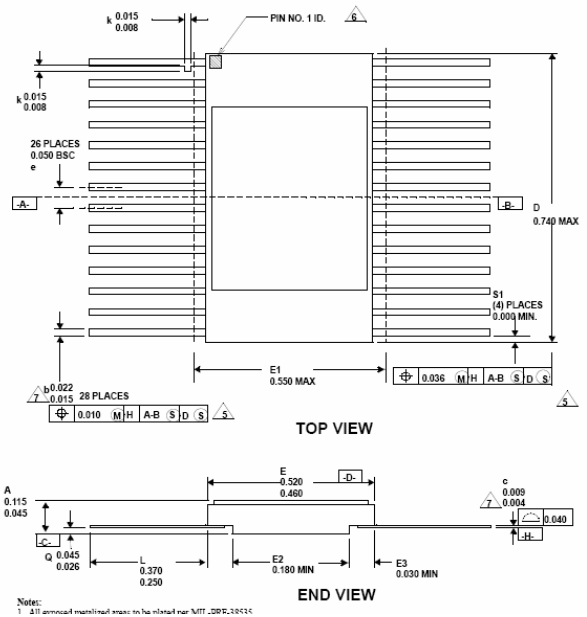
May 18th, 2006
www.aeroflex.com/spacewire



SpW PHY Product Description

- Implements low level SpaceWire Physical Layer allowing for predictable system performance and margin
- Operates on a 3.3 Volt Power Supply
- Two transmit and two receive LVDS differential signals for SpaceWire Interface
- External resets for the TX and RX flip-flops.
- Separate output enables for the TX and RX outputs
- LVTTL Compatible Inputs (5 volt tolerant)
- 3.3 Volt CMOS Outputs
- Cold Sparing on LVDS pins
- 28-lead flatpack
- Empty/full flag
- Read flag
- Samples Available June ‘06





SpW Phy Chip vs Standard LVDS

- PHY Chip
  - Better for FPGA Designs
    - FPGA's can have high worst case skew on I/O's
  - Allows the Protocol Handler to run slower
  - Each Device is a single link
    - Better for redundancy systems
  - Provides a buffer between connector and the Protocol Handler
- Standard LVDS
  - Suitable for ASIC SpaceWire Implementations
  - Provides a buffer between connector and the Protocol Handler