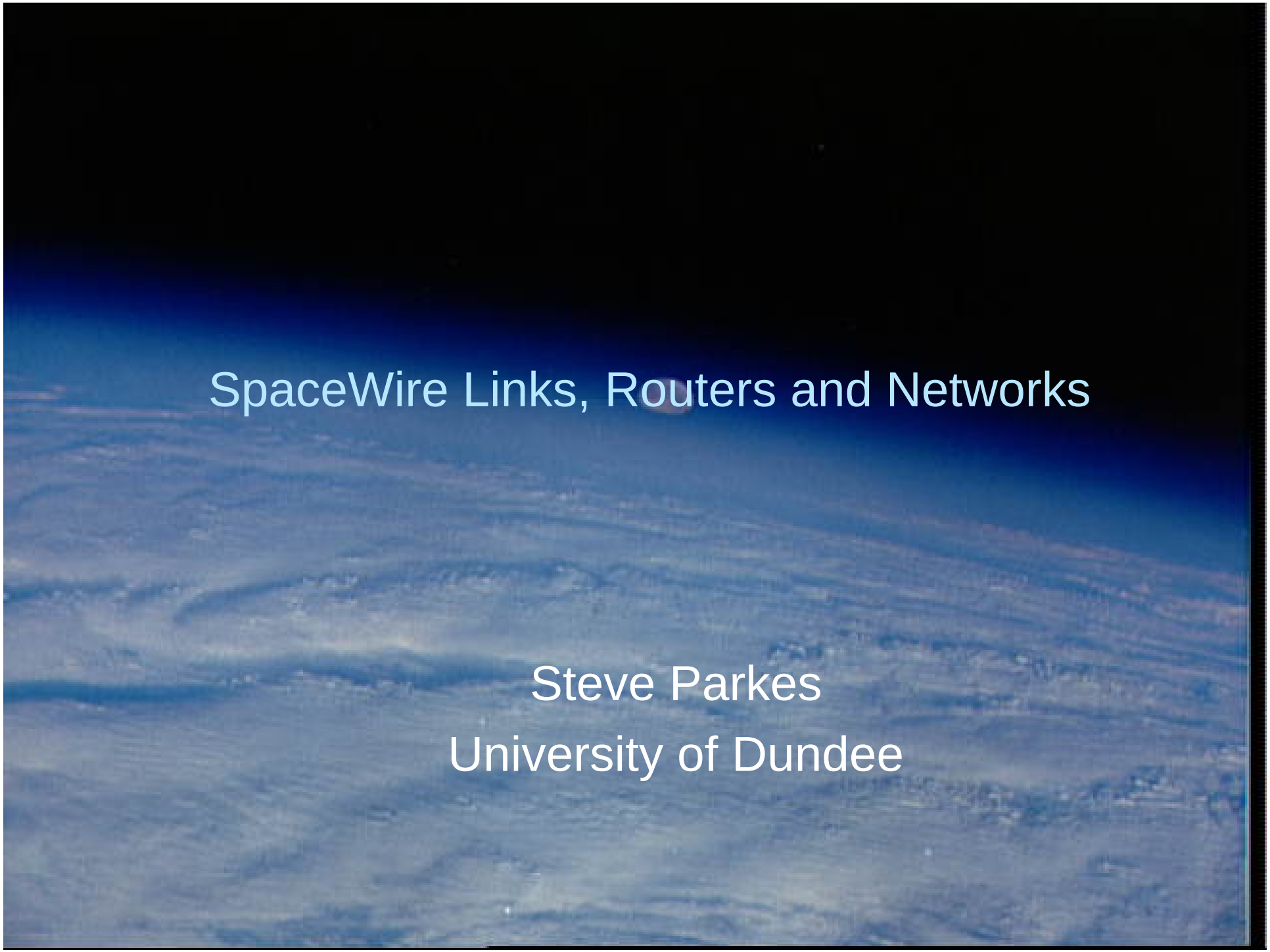

SpaceWire Links, Routers and Networks
Steve Parkes
University of Dundee

Contents

- Introduction
- SpaceWire Standard
- SpaceWire Time-Codes
- SpaceWire IP and Devices
- Key Features of SpaceWire
- Higher Level Protocols

Introduction

- SpaceWire provides a unified high-speed data-handling network for connecting together
  - Sensors,
  - Processing elements,
  - Mass-memory units,
  - Downlink telemetry sub-systems,
  - EGSE

Introduction

- SpaceWire a standard for spacecraft onboard data-handling
  - ESA ECSS-E-50-12A
- Based on two commercial standards
  - IEEE-1355 with bugs fixed
  - LVDS (Low Voltage Differential Signalling)
- SpaceWire is the result of work by many people across the world

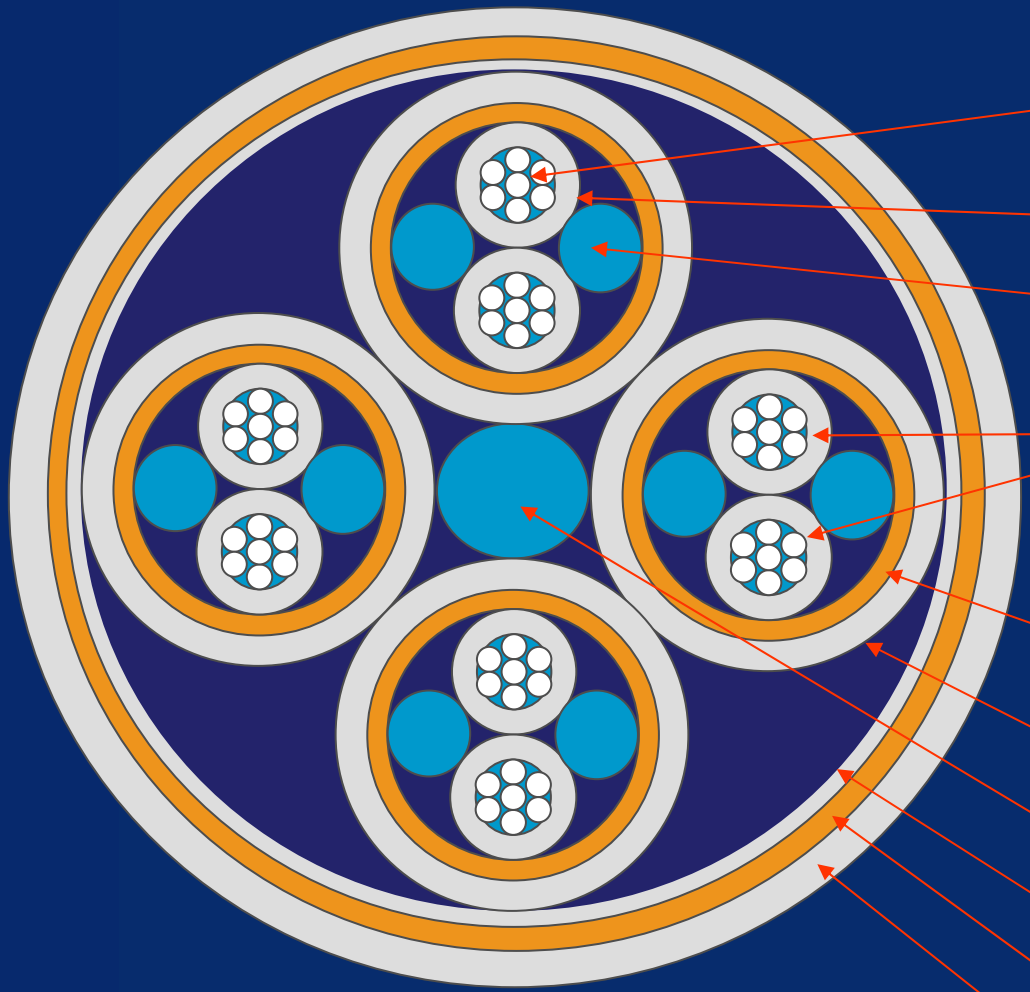
Standard

- The SpaceWire standard covers the following normative protocol levels
  - Physical Level: Connectors, cable assemblies and PCB tracks
  - Signal Level: Data-Strobe signal encoding, voltage-levels, noise margins, and data rates
  - Character Level: Data and control characters used to manage the flow of data across a link
  - Exchange Level: Protocol for link initialisation, flow control, link error detection and link error recovery
  - Packet Level: How data is split up into packets for transfer across a SpaceWire link
  - Network Level: Structure of a SpaceWire network, transfer of packets across a network, handling of errors

Physical Level

- Cables
- Connectors
- Cable Assemblies
- PCB Traces

Cable Construction



Conductor 28 AWG
(7 x 36 AWG)

Insulating layer

Filler

Twisted pair

Inner shield around
twisted pair (40AWG)

Jacket

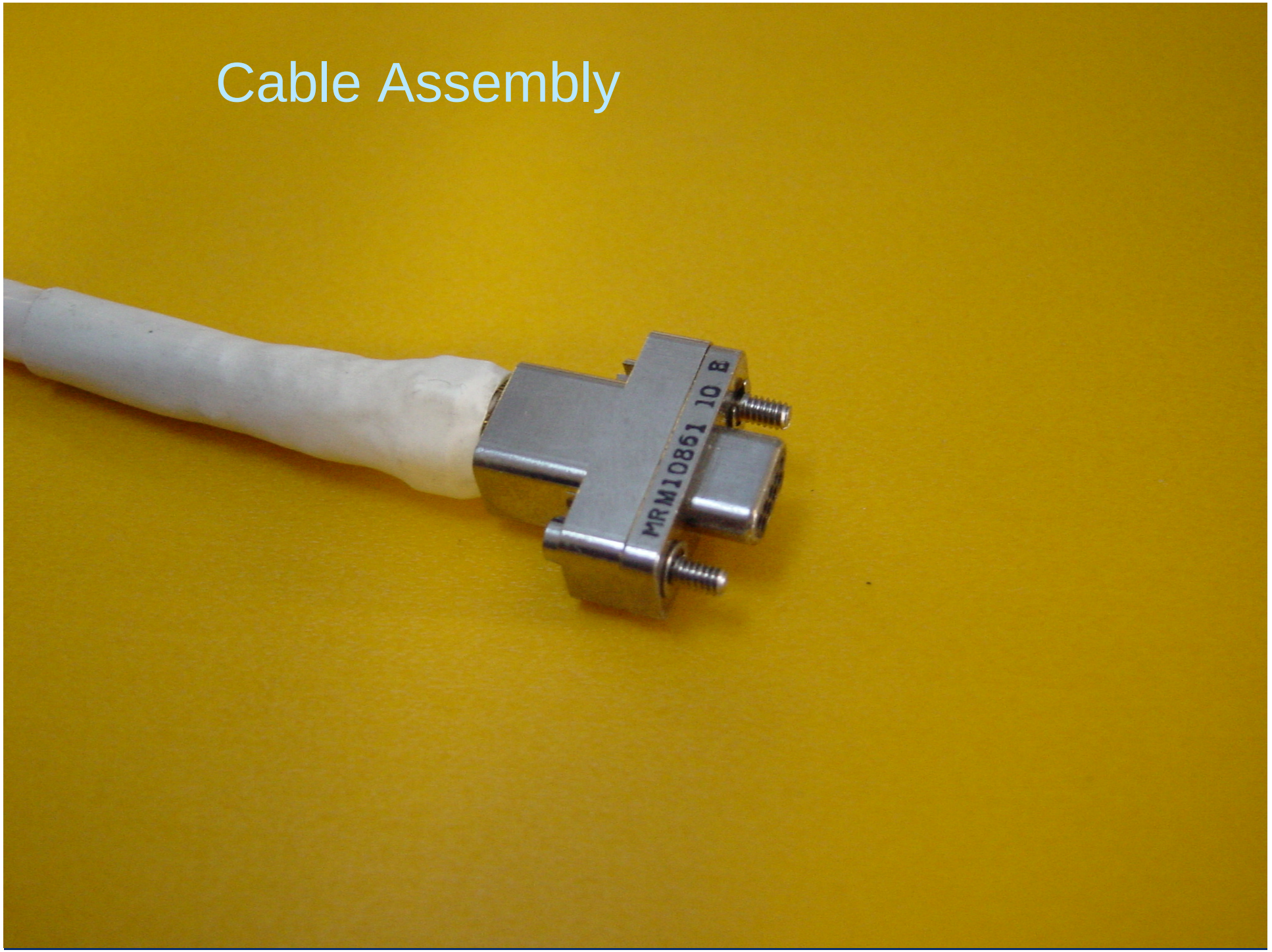
Filler

Binder

Outer shield (38AWG)

Outer Jacket

Cable Assembly



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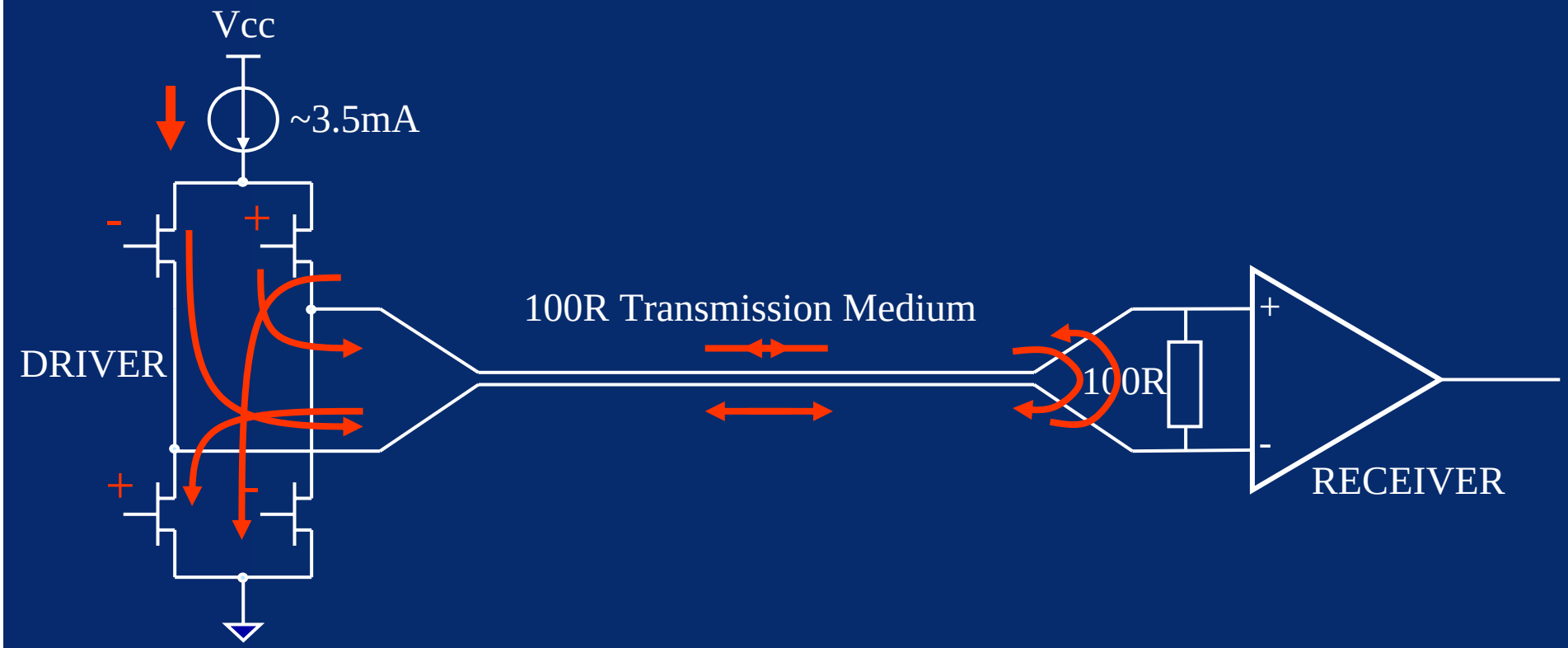
Signal Level

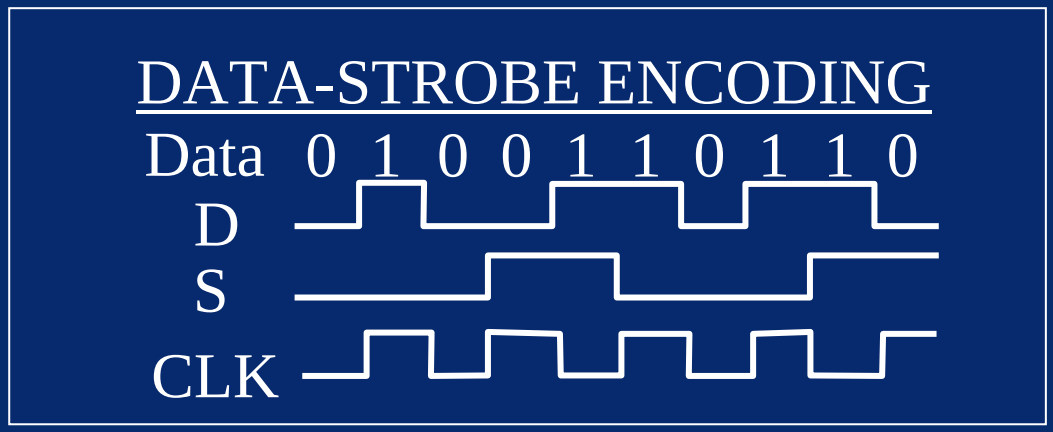
- Low Voltage Differential Signalling (LVDS)
- Signal Encoding - Data/Strobe Encoding

LVDS Driver and Receiver



Data Encoding

- SpaceWire uses Data-Strobe (DS) encoding
  - Data values transmitted directly
  - Clock encoded with data to form strobe
  - XORing data and strobe recovers clock
  - Provides improved jitter/skew tolerance compared to data clock encoding



- D and S transmitted differentially using LVDS

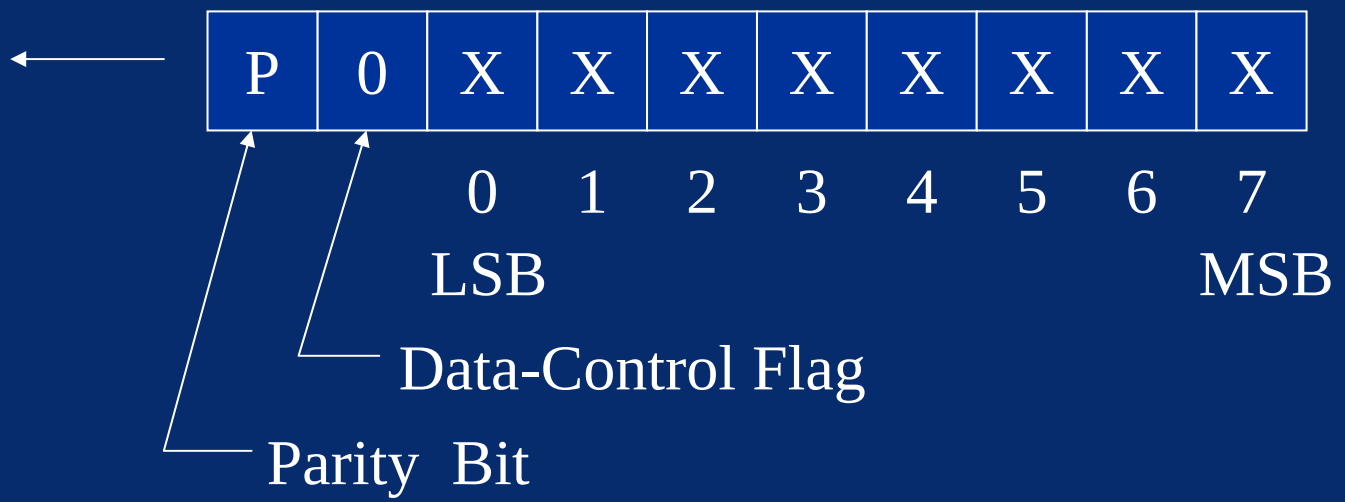
Data Signalling Rate

- Minimum data signalling rate
  - 2 Mbits/s
- Maximum data signalling rate
  - Depends on skew/jitter and attenuation
  - >> 100 Mbits/s
- Operational data signalling rate
  - Any rate 2 Mbits/s to maximum
  - Rx and Tx can operate ad different rates
  - Tx rate may be altered at any time after link connection made
- Initial data signalling rate 10 +/- 1 Mbits/s

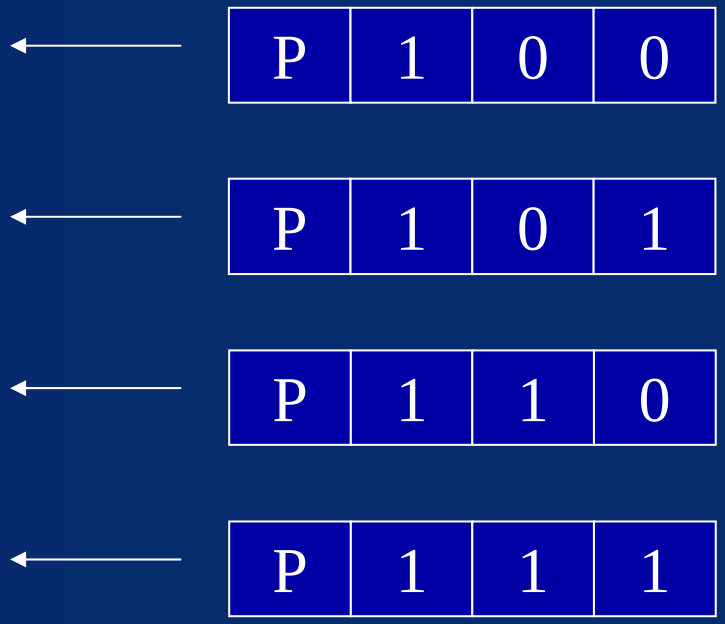
Character Level

- Character level defines
  - Data characters
    - Used to transfer data
  - Control characters
    - Used to manage flow of data across link
- Two types of character
  - L-char
    - Concerned with link operation
  - N-char
    - Used to carry data and delimit packets

Data Characters



Control Characters



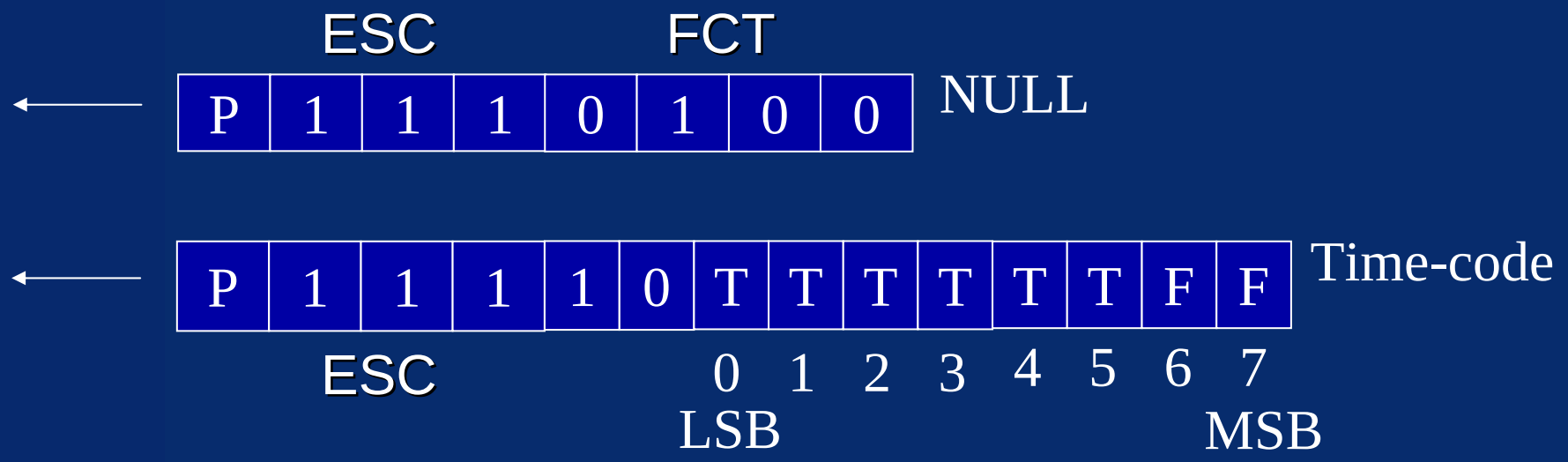
FCT Flow Control Token

EOP Normal End of Packet

EEP Error End of Packet

ESC Escape

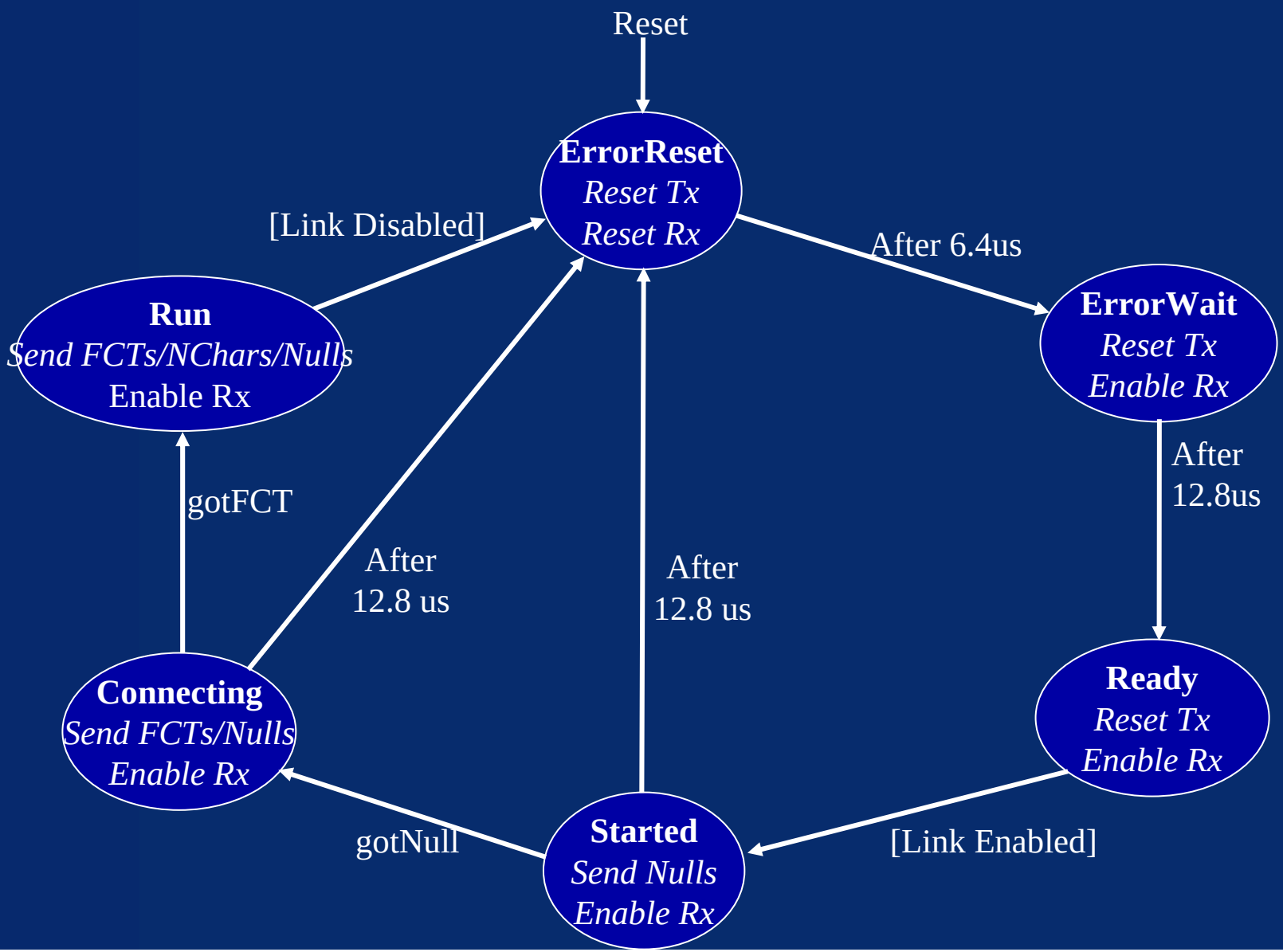
Control Codes



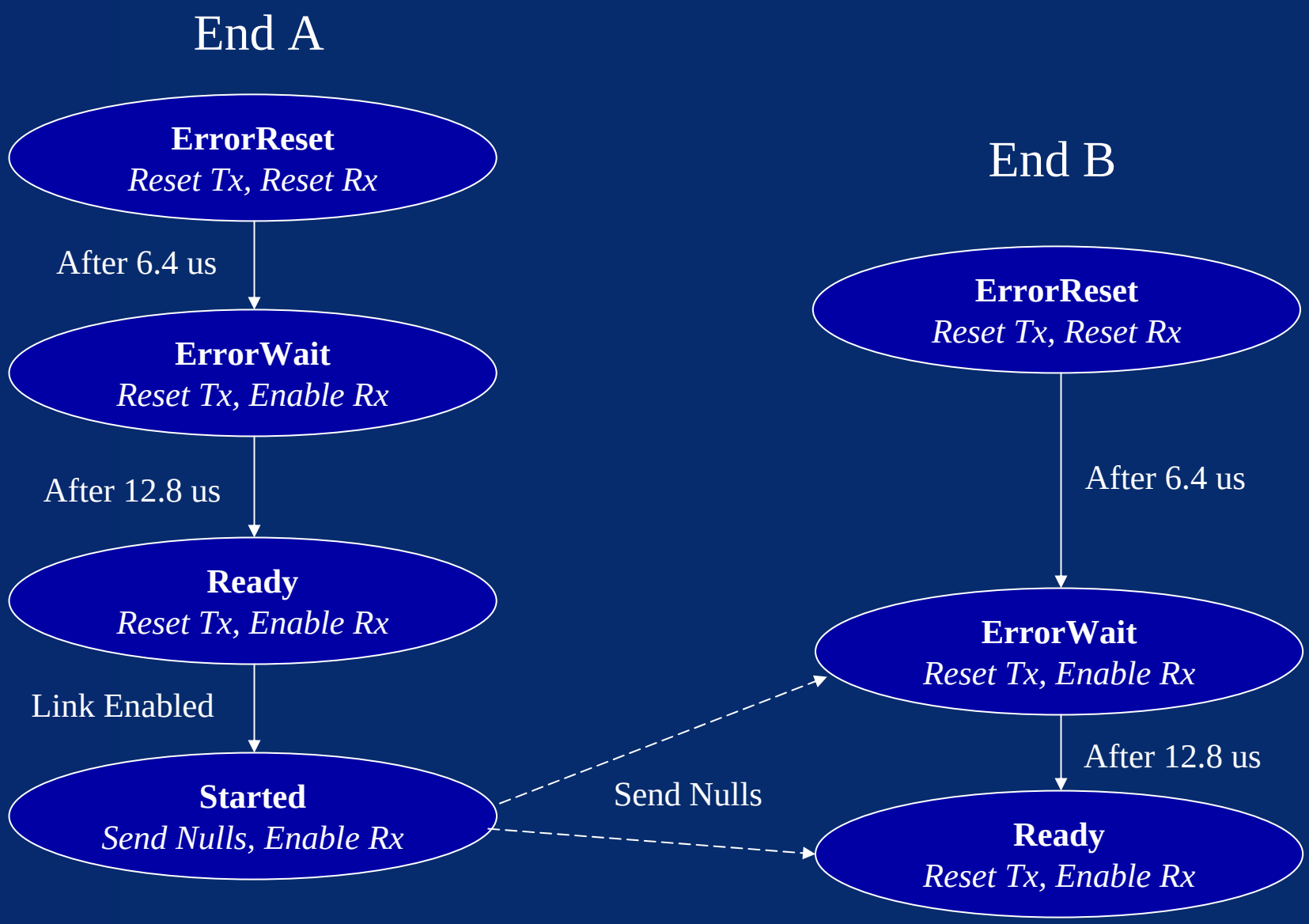
Exchange Level

- Exchange Level Protocol defines
  - Link initialisation
  - Flow control
  - Detection of link errors
  - Recovery from link errors

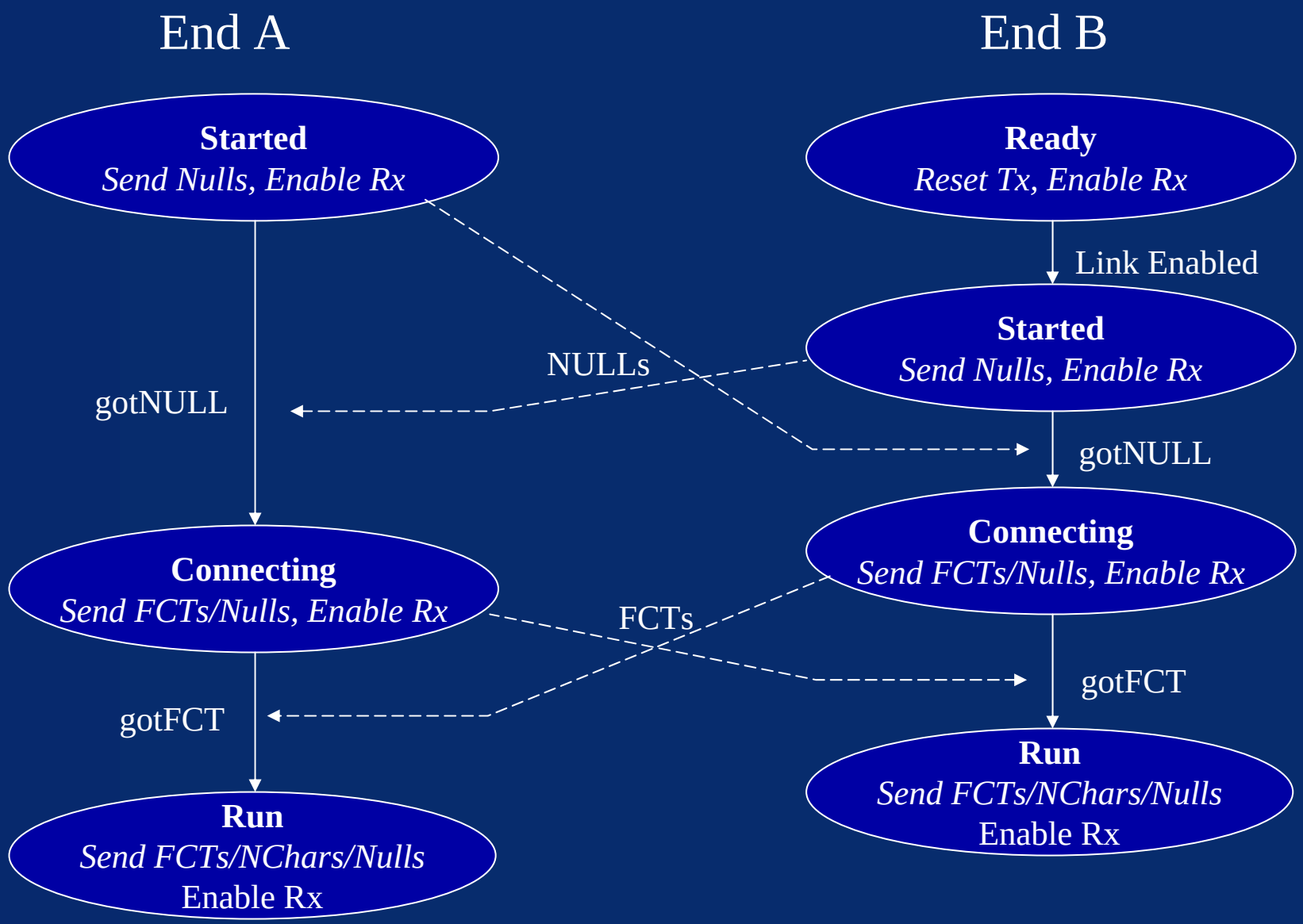
Basic State Machine



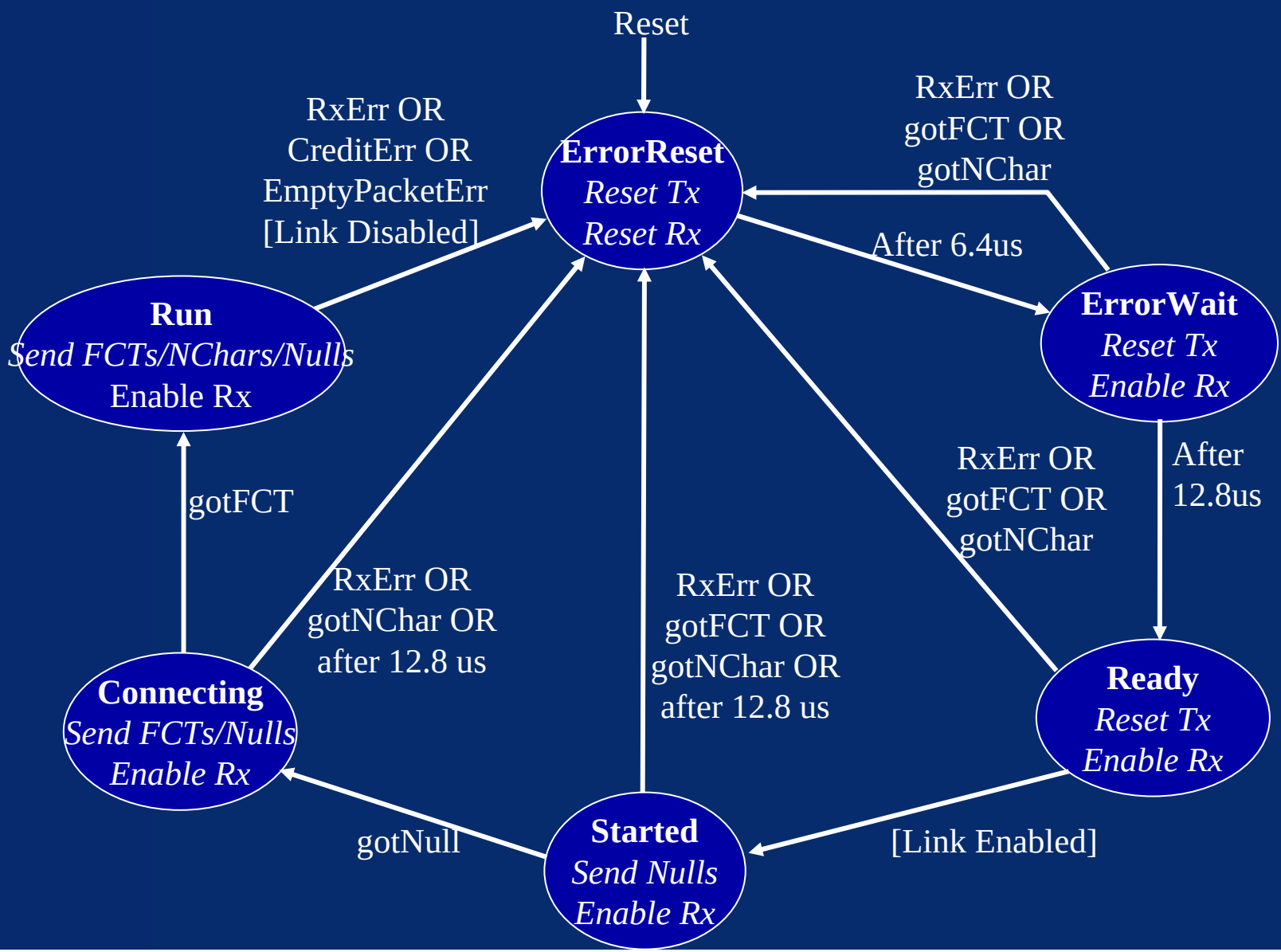
Link Initialisation (1)



Link Initialisation (2)



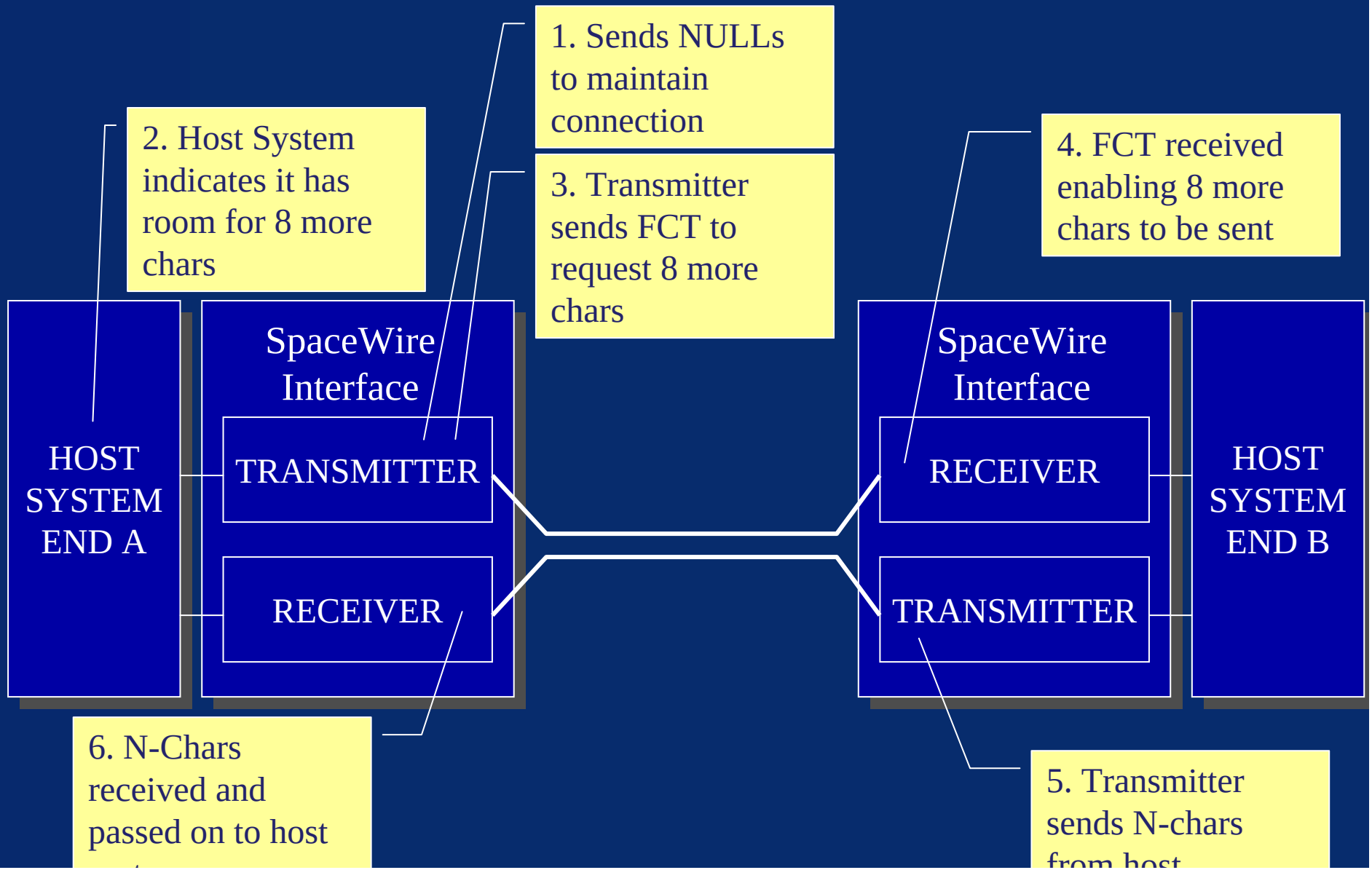
Full State Machine



Flow Control

- Flow control used to avoid overflow of host receive buffer
  - Use flow control tokens (FCTs)
  - Send FCT from end A to end B
  - when end A can accept 8 more N-Chars.
  - This enables end B to send up to 8 more N-Chars.
  - Multiple FCTs can be sent if there is more room in buffer.
- FCT is exchanged for 8 N-Chars
- TX and RX must keep count of credit.

Normal Operation



Error Detection

- Disconnect Error
  - No RX clock transition for more than 850 ns
- Parity Error
  - Parity bit
- Escape Error
  - ESC should only be followed by
    - FCT to form a Null
    - Data to form a time-code
- Credit Error
  - If there is no room in host RX buffer for data received then an error must have occurred that affected the FCTs
- Empty Packet Error
  - EOP/EEP followed by another EOP/EEP

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Packet Level

- Packet Level Protocol
  - Defines packet structure

SpaceWire Packets

- Packet formal
  - <DESTINATION><CARGO><EOP>
- Destination
  - Represents path to or identity of destination node
- Cargo
  - Data or message to be transferred from source to destination
- EOP
  - Indicates end of packet

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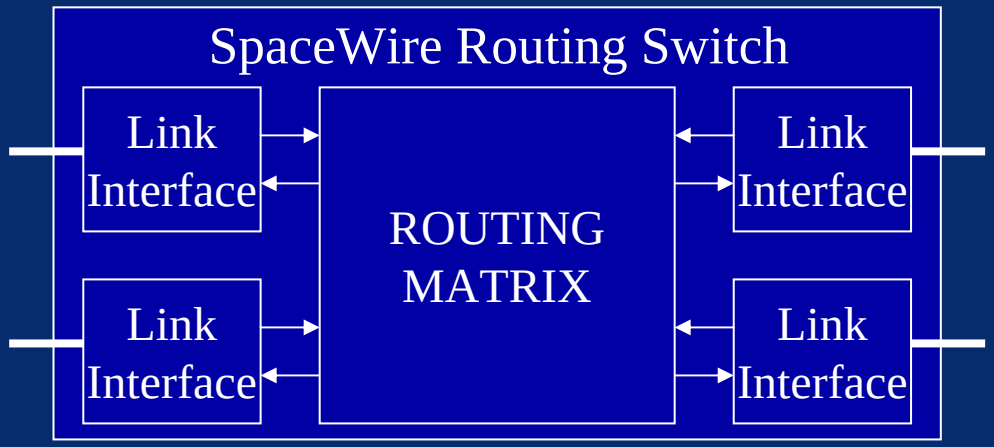
SpaceWire Routing Switches



- Several link interfaces interconnected via a switching matrix.
- Wormhole routing.
- Path and Logical addressing.
- Priority addressing.
- Group adaptive routing.

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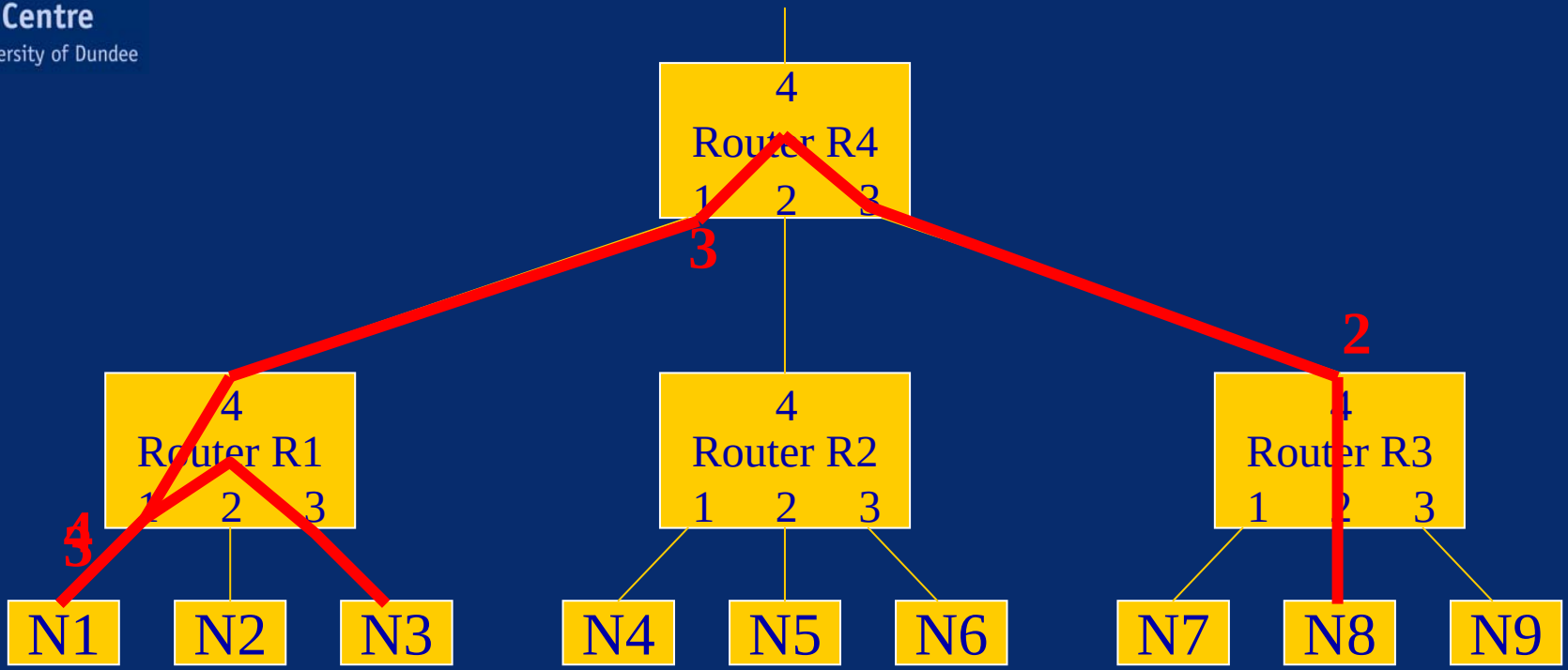
Path Addressing

- Destination is specified as router output port number
- Node 1 to node 3 <3><cargo><EOP>
- Node 1 to node 8 <4><3><2><cargo><EOP>



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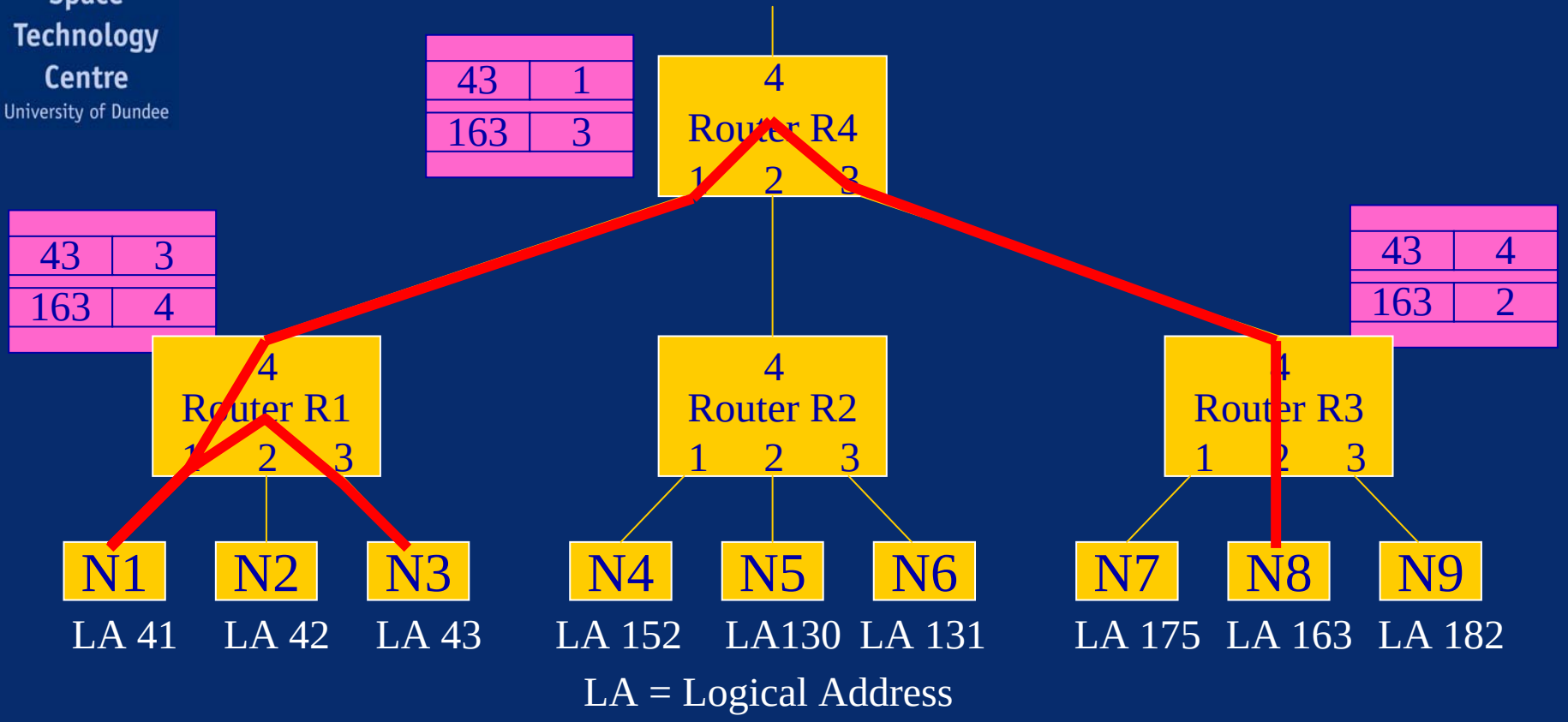
Logical Addressing

- Each destination has a unique logical address
- Each router has a list of which port(s) to send data out for each possible destination
- Node 1 to node with logical address 43 <43><cargo><EOP>
- Node 1 to node with logical address 163 <163><cargo><EOP>



Routing Table

	Address	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	1	0	0	0	0
Path Addressing	1	0	1	0	0	0
	2	0	0	1	0	0
	…					
Logical Addressing	32	0	1	0	0	0
	33	0	0	1	0	0
	34	0	0	0	0	1
	…					
Reserved	255	0	0	0	0	0

Priority

- Arbitration in Router
  - Fair arbitration
  - Priority based
- SpaceWire header contains address only
- Assign priority to logical addresses

Priority

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	…						
Logical Addressing	32	0	0	1	0	0	0
	33	1	0	1	0	0	0
	34	0	0	0	0	0	1
	…						
Reserved	255	0	0	0	0	0	0

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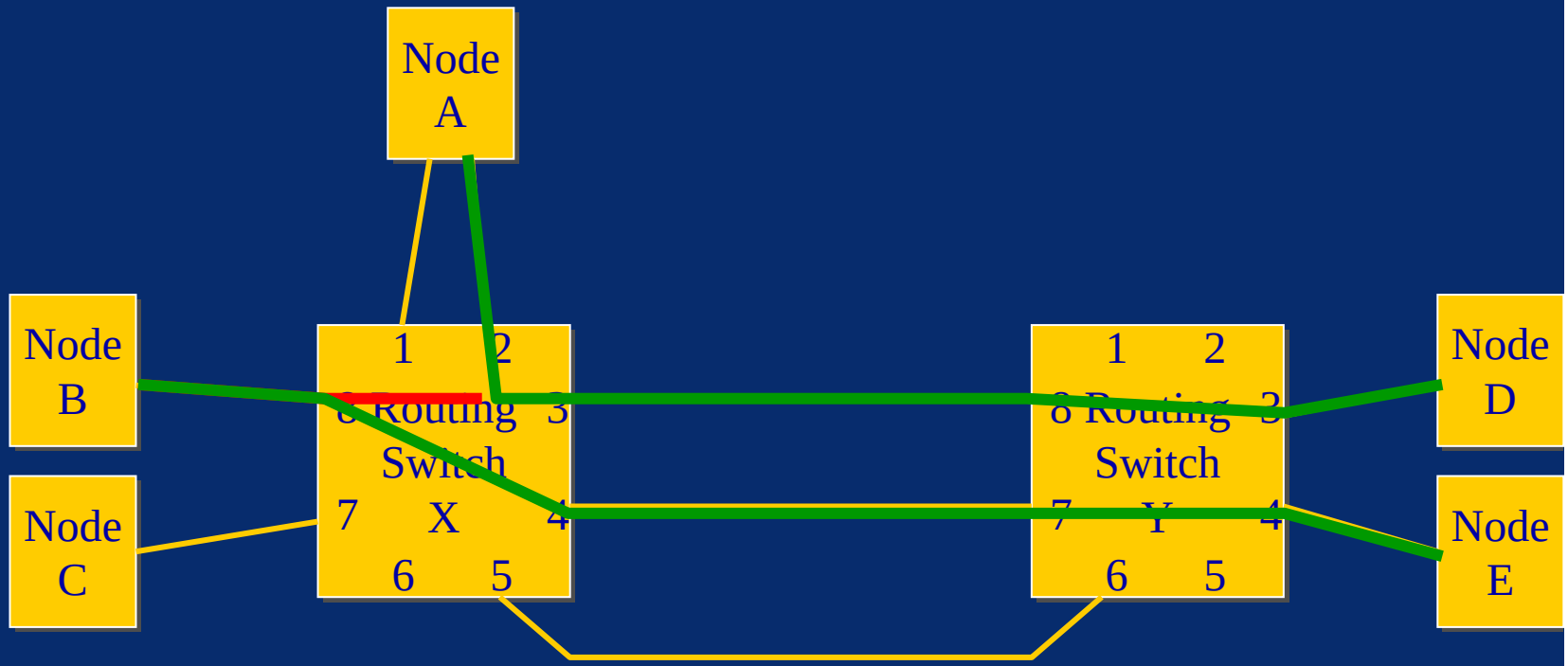
Group Adaptive Routing



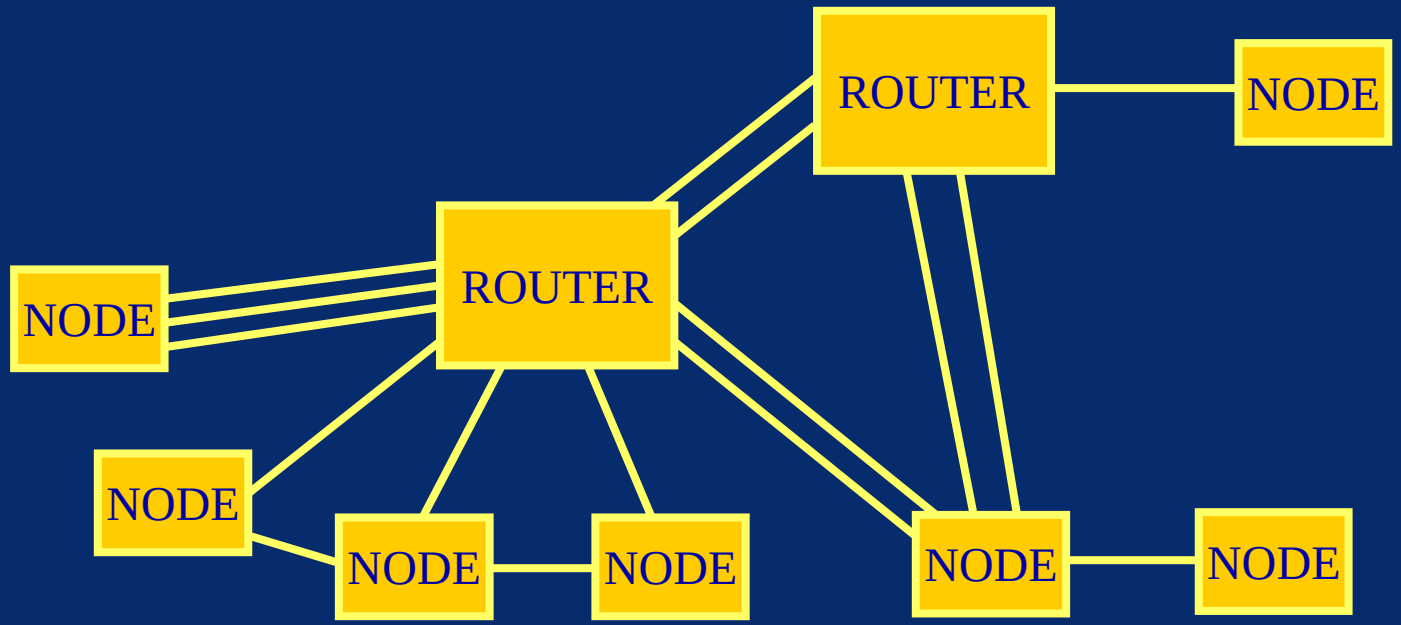
- Node B to Node E can use any of three possible links between router X and router Y
- Shares available bandwidth
- Provides support for fault tolerance

Group Adaptive Routing

	Address	Priority	Port 0	Port 1	Port 2	Port 3	Port 4
Configuration	0	0	1	0	0	0	0
Path Addressing	1	0	0	1	0	0	0
	2	0	0	0	1	0	0
	…						
Logical Addressing	32	0	0	1	1	0	0
	33	1	0	1	1	0	0
	34	0	0	0	0	1	1
	…						
Reserved	255	0	0	0	0	0	0

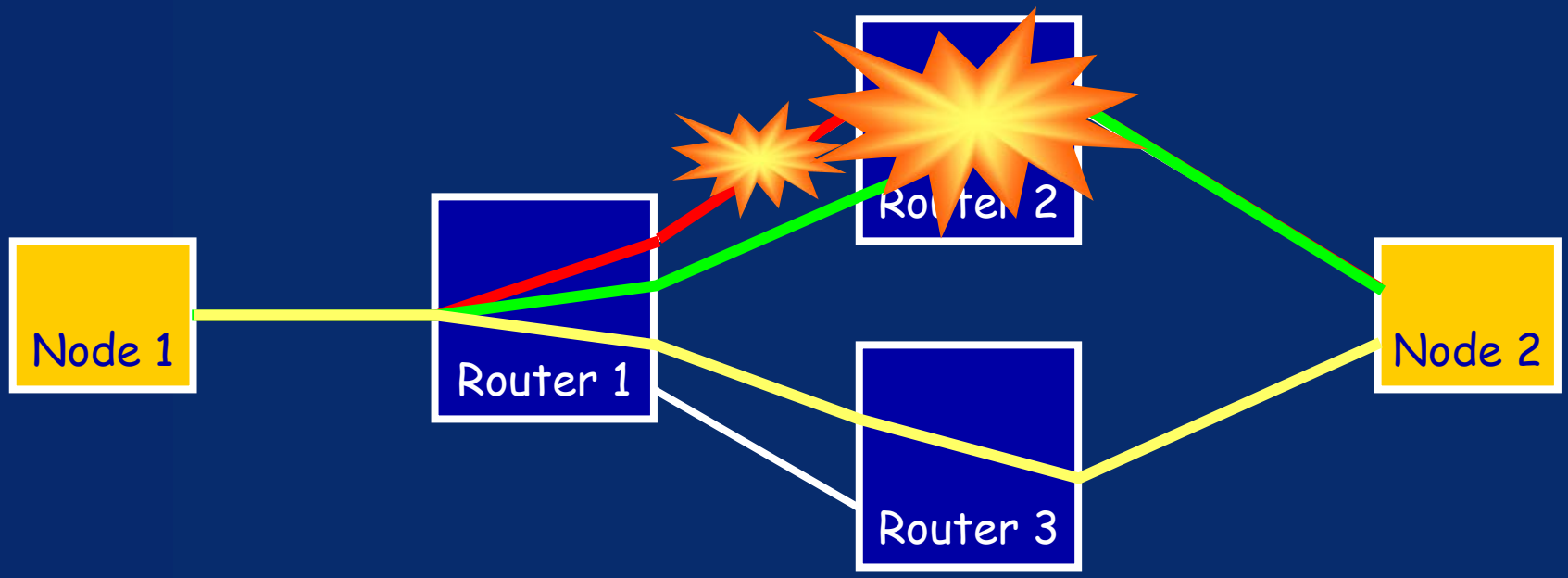
SpaceWire Network

- Two or more SpaceWire nodes
- Zero or more SpaceWire routing switches
- Interconnected with SpaceWire links



- Add bandwidth where required
- Add redundant links where required

Fault Tolerant Network



Time-codes

- Low latency broadcast of time information
- 6-bit time-value
- 2 flag bits
- Can be used for:
  - Time distribution
  - Event signalling
  - Isochronous communications

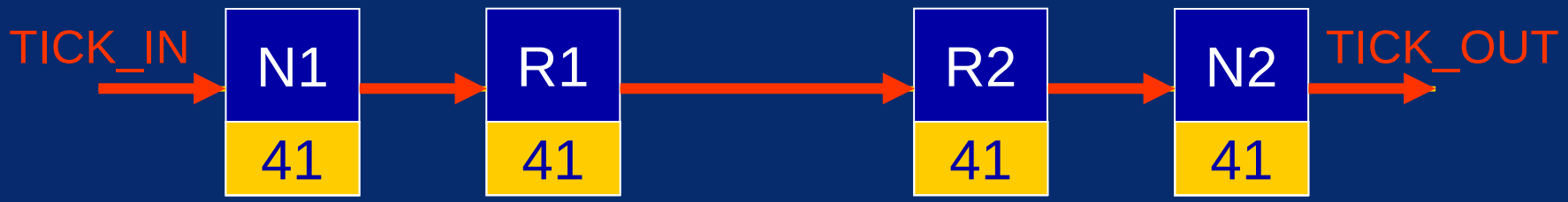
Nodes and Routers

- Each node or router has a 6-bit time counter
- Link interfaces have TICK_IN and TICK_OUT signals
- Asserting TICK_IN causes
  - Time counter to be incremented
  - New time-code to be transmitted
  - With value of time counter
- TICK_IN used by only one, time-master node
- When valid time-code received
  - Time counter is incremented
  - TICK_OUT is asserted

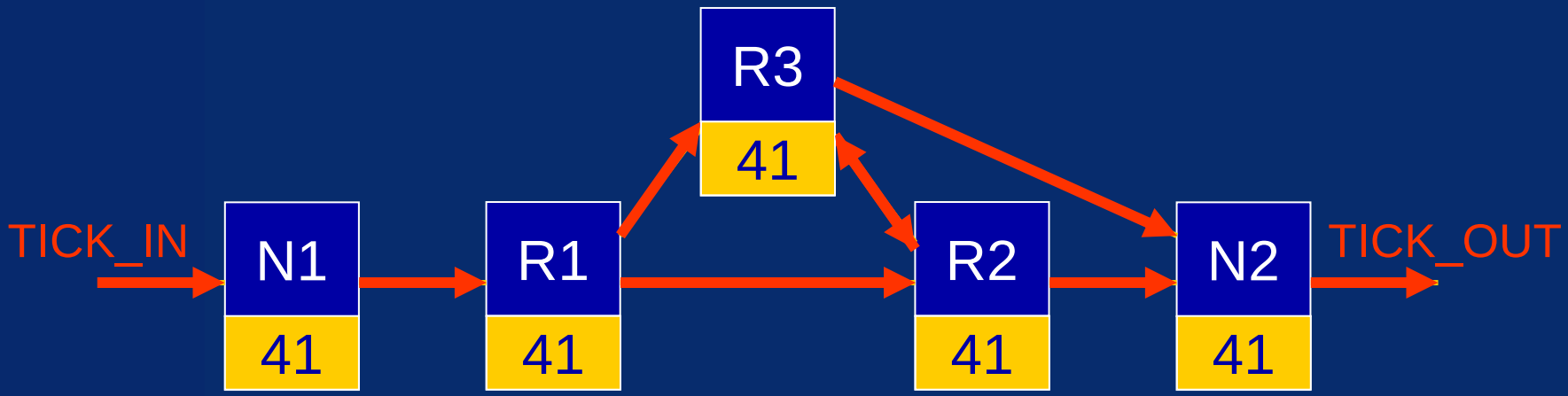
Nodes and Routers

- Valid time-codes have
  - Value of one more than time-counter
  - At the receiver
- If valid
  - Set time counter to new time-code value
  - Propagate time-code
- IF NOT valid
  - Set time counter to new time-code value
  - Do NOT propagate time-code

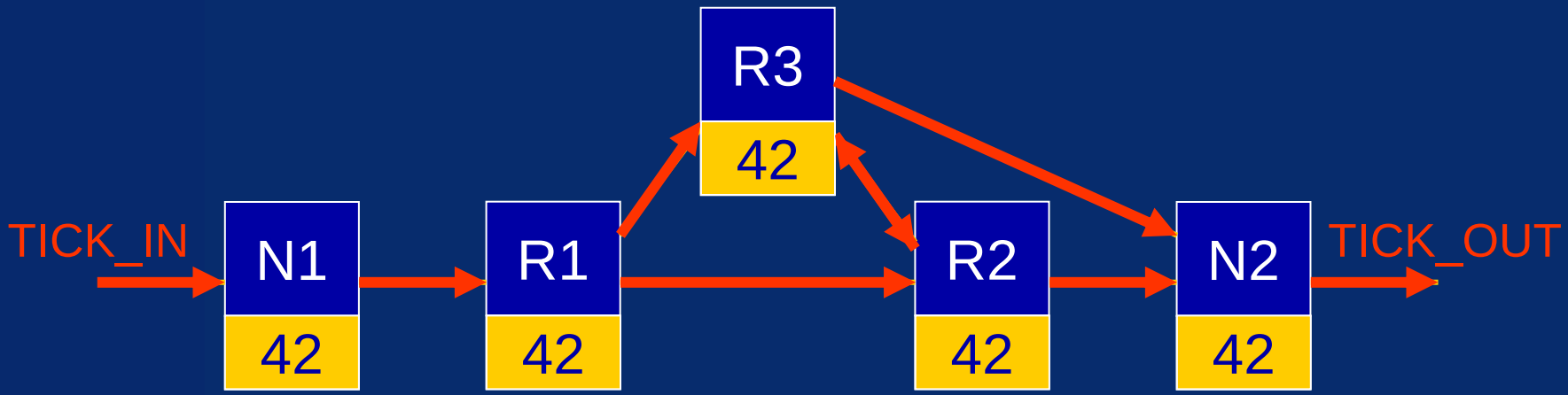
Time Distribution



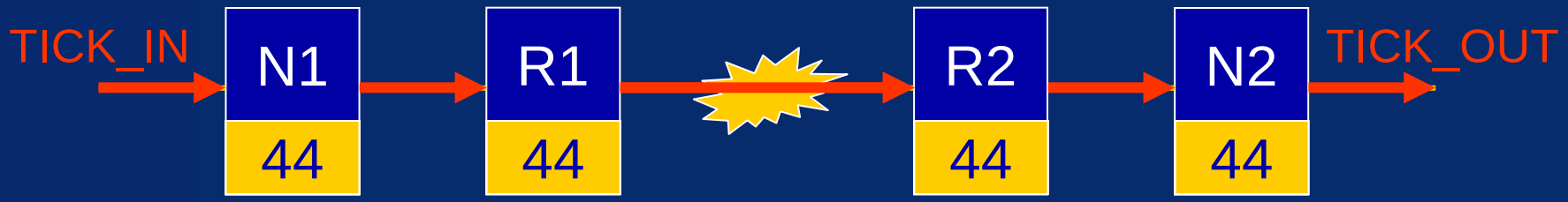
Time Distribution



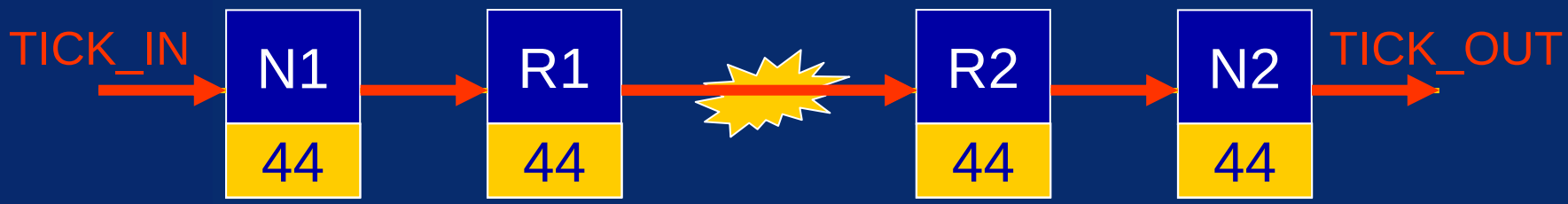
Time Distribution



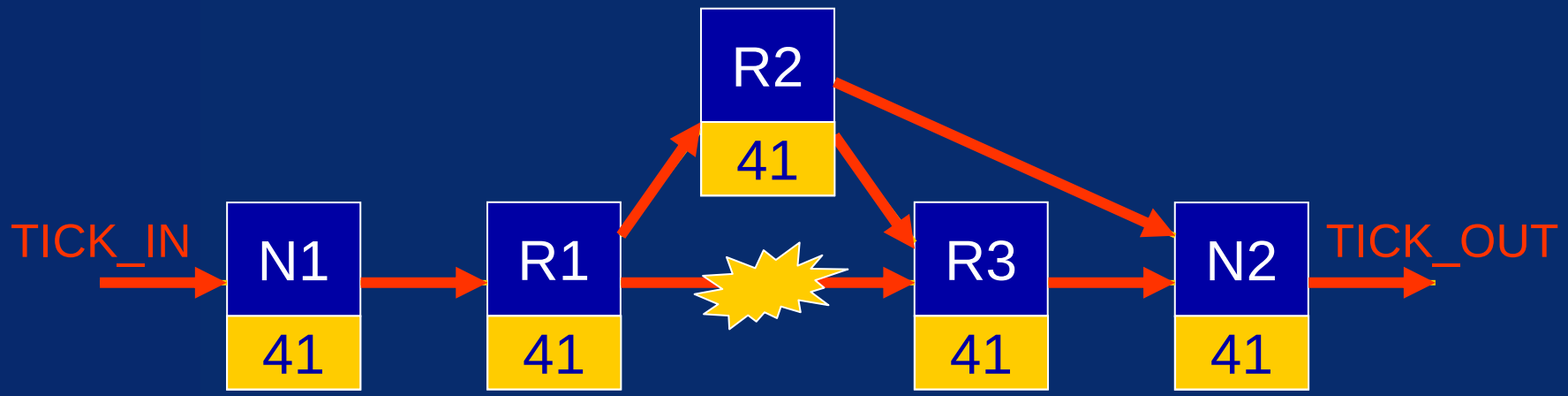
Time Distribution Error



Time Distribution Error



Time Distribution Error



Time-Code Latency

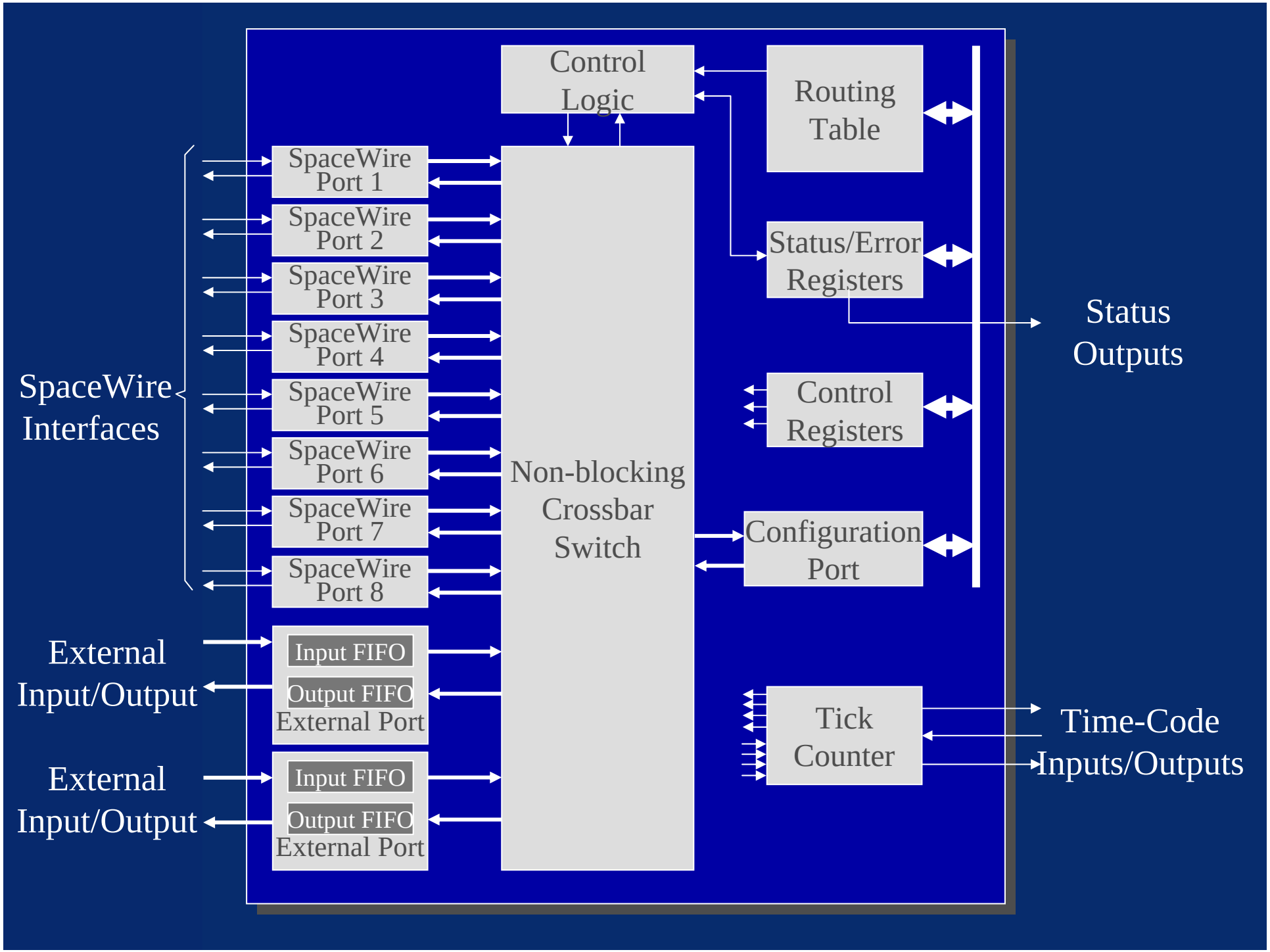
- Latency depends on
  - Number of links over which time-code travels
  - Operating rate of the links
  - Delay at time-code source
  - Delay at each router
  - Delay at each receiving node

SpaceWire IP

- SpaceWire CODEC
  - Configurable VHDL core
  - Suitable for ASIC and FPGA implmentation
  - Developed University of Dundee
  - Distributed by ESA for European space projects
  - Available from UoD for other applications
- SpaceWire Routing Switch
  - Configuratble VHDL Router
    - Generics for
      - Number for SpaceWire Ports
      - Number of External Ports
  - Developed by University of Dundee
  - Available from UoD under licence

SpaceWire Devices

- Radiation tolerant FPGA implementations
- SMCS332SpW
  - 3 SpaceWire ports
  - Interface to processor and memory
- SMCSLiteSpW
  - 1 SpaceWire port
  - Interface to peripherals
  - E.g. DAC, ADC, FIFO, UART, GPIO
- Remote Terminal Computer
  - LEON SPARC processor
  - With SpaceWire and CAN bus interfaces
- SpaceWire Router


Control Logic
Routing Table
SpaceWire Port 1
SpaceWire Port 2
SpaceWire Port 3
SpaceWire Port 4
SpaceWire Port 5
SpaceWire Port 6
SpaceWire Port 7
SpaceWire Port 8
Status/Error Registers
Status Outputs
SpaceWire Interfaces
Control Registers
Non-blocking Crossbar Switch
Configuration Port
External Input/Output
Input FIFO
Output FIFO
External Port
Tick Counter
Time-Code Inputs/Outputs
External Input/Output
Input FIFO
Output FIFO
External Port

Router ASIC Technology

- ASIC
  - Implementation in Atmel MHR1RT gate array
  - Max gate count 519 kgates (typical)
  - 0.35 µm CMOS process
- Radiation tolerance
  - Up to 300 krad
  - SEU free cells to 100 MeV
  - Used for all critical memory cells
  - Latch-up immunity to 100 MeV

Router ASIC Performance

- Performance
  - SpaceWire interface 200 Mbits/s
  - Low latency < 1µs
  - LVDS drivers/receivers integrated on chip
- Power
  - 4 W power with all links at maximum data rate
  - Single 3.3 V supply
  - Power saving modes
- Package
  - 196 pin ceramic Quad Flat Pack 25 mil spacing

SpaceWire Key Features

- Serial, bi-directional, full duplex
- High data rate (> 200 Mbits/s)
- Distance of 10 m +
- Low gate count
- Can be implemented in FPGAs
- Scalable
- Low error rate
- Good EMC performance
- Fault tolerant support
- Radiation tolerant components

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Higher-Level Protocols

- Remote Memory Access Protocol
- SMCS Configuration Protocol
- CCSDS SOIS Protocol

SpaceWire Protocol Identifier

Logical Address with Protocol ID

Path Address with Protocol ID

RMAP

- Remote Memory Access Protocol
- Provides a means of
  - Writing to
  - Reading from
  - Registers or memory on a SpaceWire node
  - Registers are considered to be memory-mapped
- Simple
- Flexible
- Encompasses diverse applications

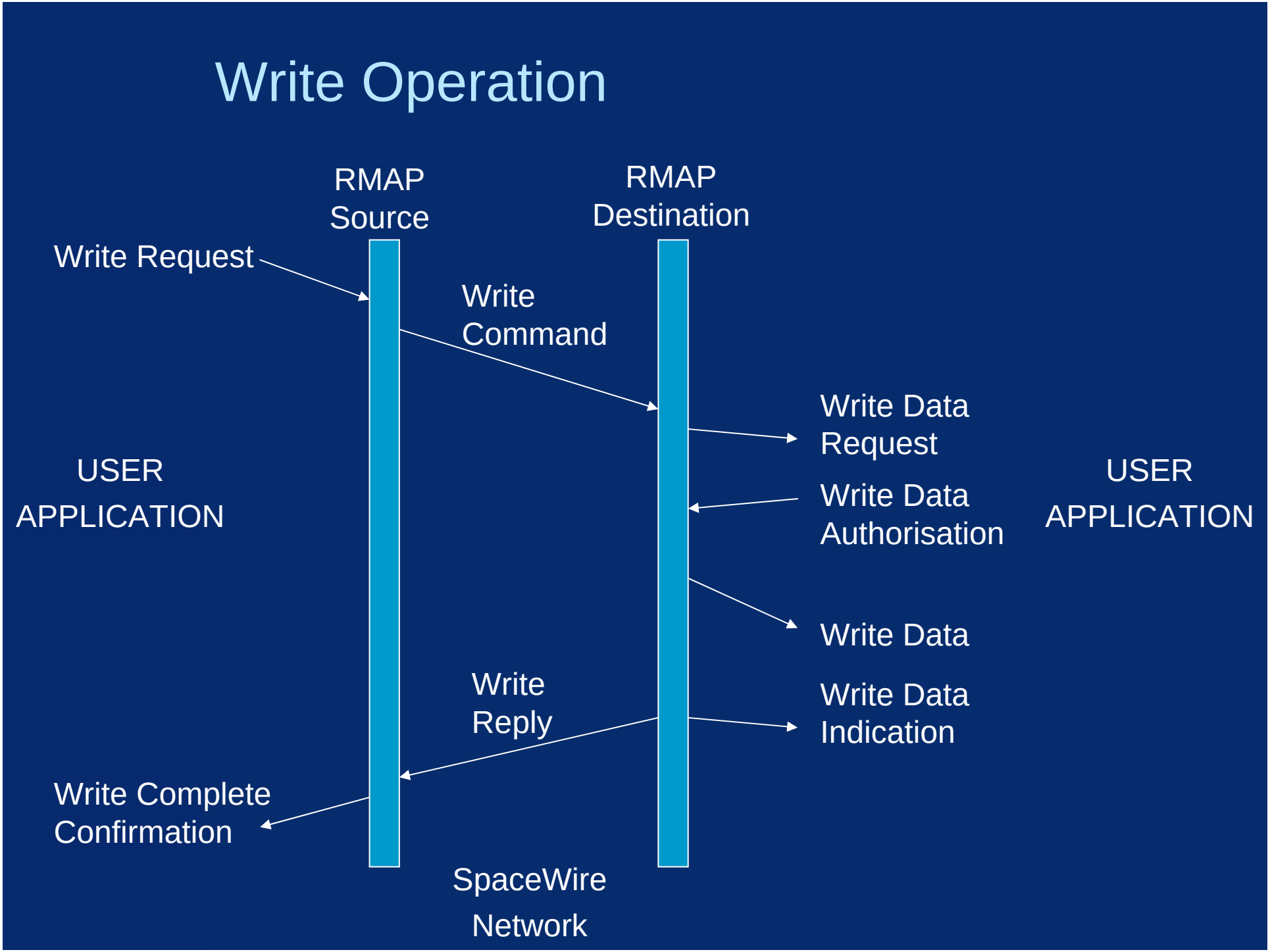
Write Command

First byte transmitted

Destination Logical Addr.	Protocol Identifier	Packet Type, Command, Source Path Addr Len	Destination Key
Source Logical Address	Transaction Identifier	Transaction Identifier	Extended Write Address
Write Address (MS)	Write Address	Write Address	Write Address (LS)
Data Length (MS)	Data Length	Data Length (LS)	Header CRC
Data	Data	Data	Data
Data	Data	Data	Data
Data	Data CRC	EOP	

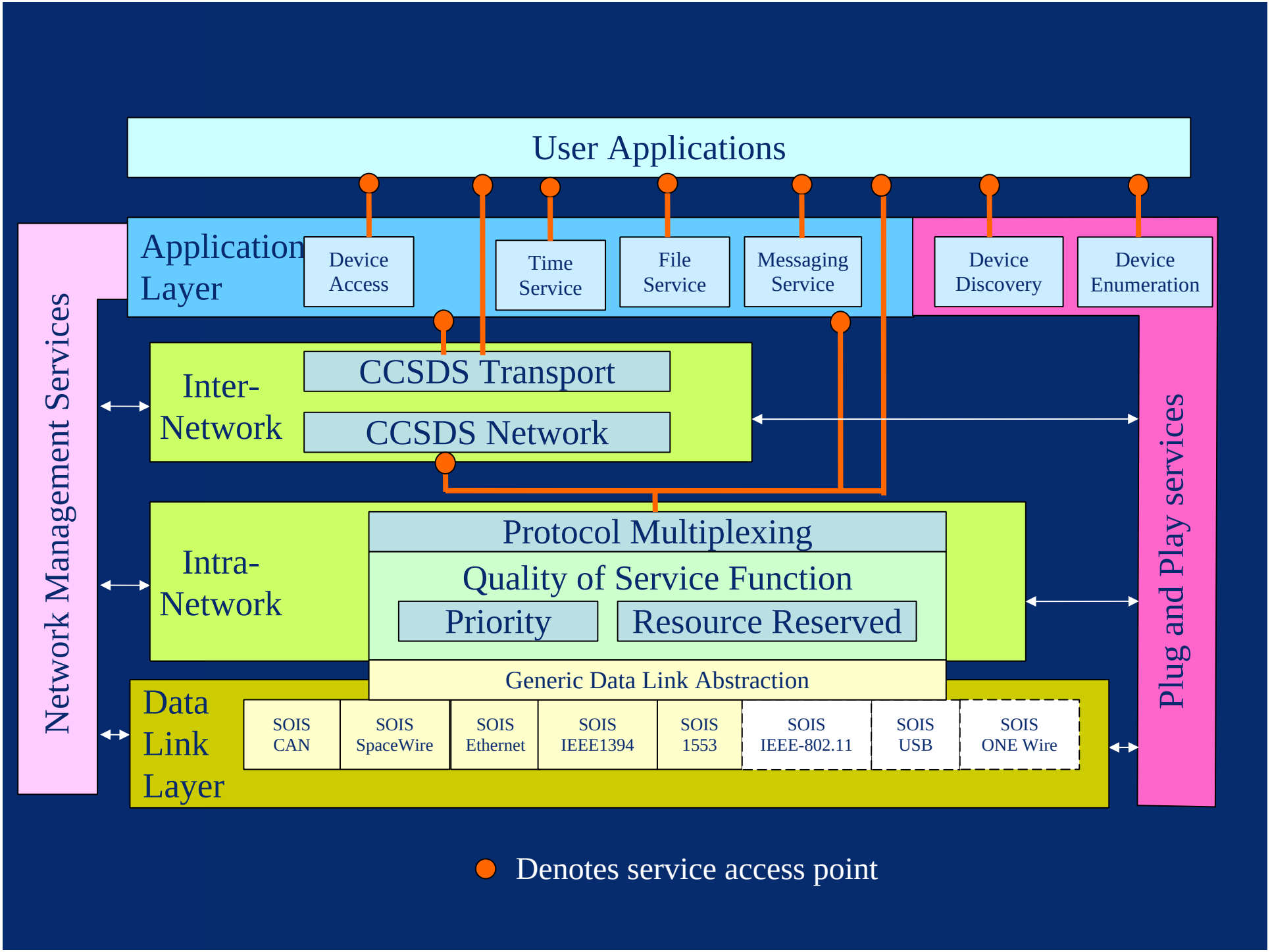
Last byte transmitted

Write Operation



CCSDS SOIS

- Architecture that provides:
  - Uniform interface for communicating over various underlying buses
    - Scheduled
    - Asynchronous
  - Comprehensive QoS for onboard applications
    - Priority
    - Reserved / non-reserved
    - Retry / try once
  - Can be implemented in many different ways
  - Can make use of features of underlying buses
    - E.g. retry mechanism of IEEE1394
    - E.g. group adaptive routing of SpaceWire


User Applications
Application Layer
Device Access
Time Service
File Service
Messaging Service
Device Discovery
Device Enumeration
Network Management Services
Inter-Network
CCSDS Transport
CCSDS Network
Intra-Network
Protocol Multiplexing
Quality of Service Function
Priority
Resource Reserved
Generic Data Link Abstraction
Data Link Layer
SOIS CAN
SOIS SpaceWire
SOIS Ethernet
SOIS IEEE1394
SOIS 1553
SOIS IEEE-802.11
SOIS USB
SOIS ONE Wire
Plug and Play services
Denotes service access point

Conclusion

- SpaceWire designed specifically for space applications
  - Low gate count
  - Low power
  - High performance
  - Standard
- IP cores available
- Devices
- Higher-level protocols