Fifth SpaceWire WG Meeting 15. - 17.11.2005

SpaceWire based On-Board-Computer

On Board Computer Concept

OBC Concept -Aims-

- Based on ERC32 32-bit processor cores

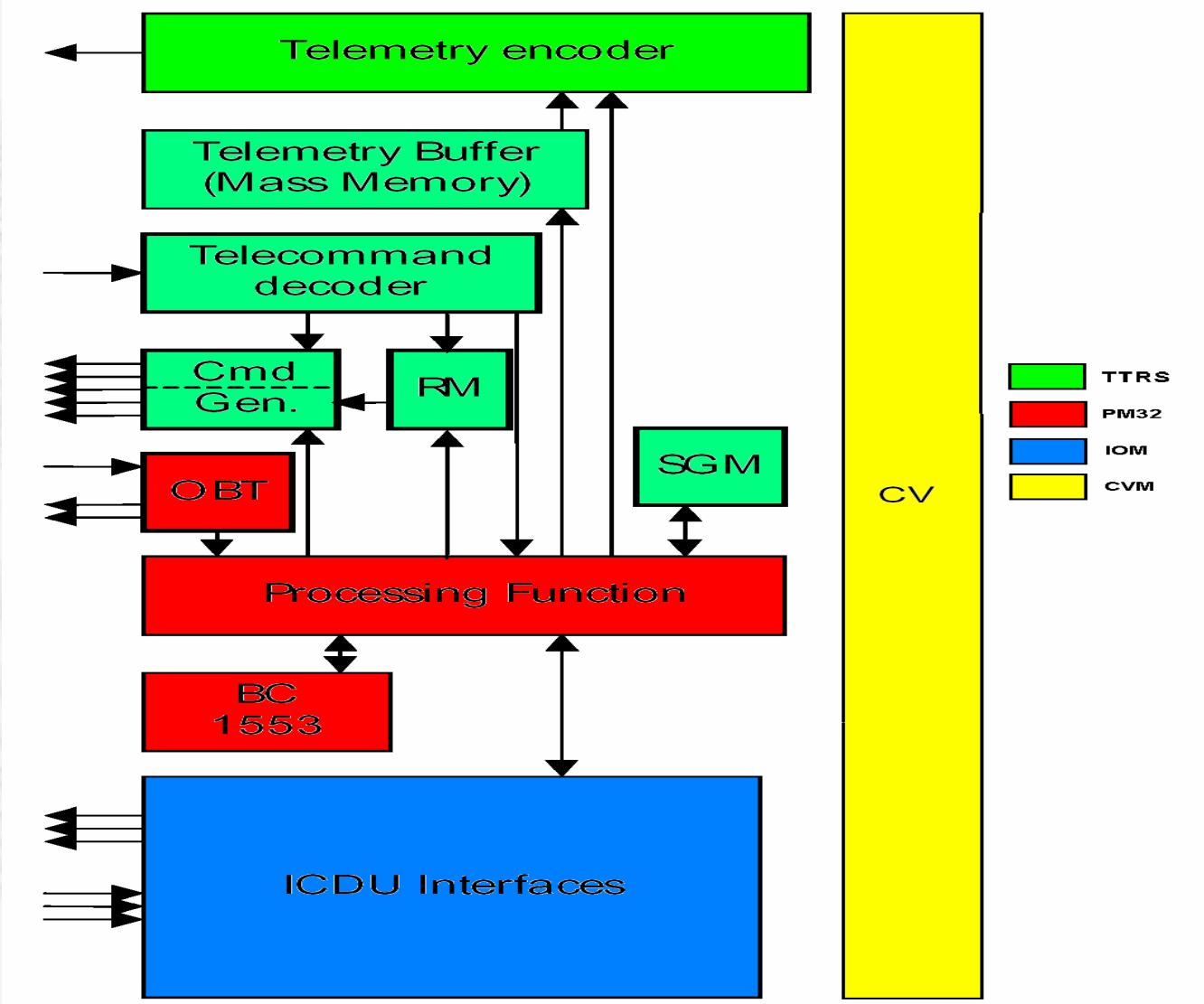
- Fully redundant
- Each function provided in two independent electrically and mechanically separated modules
- Point-to-Point SpaceWire/1355
- Modular design to allow easy adaptation to customer requirements
- Redundancy concept allowing to switch between individual functions or switch-over of complete computer function

- Single-Point Failure free
- High reliability for e.g. 15 years GEO Missions

- Integrated high speed test interface (Service I/F) SIF

OBC Concept -System Architecture-

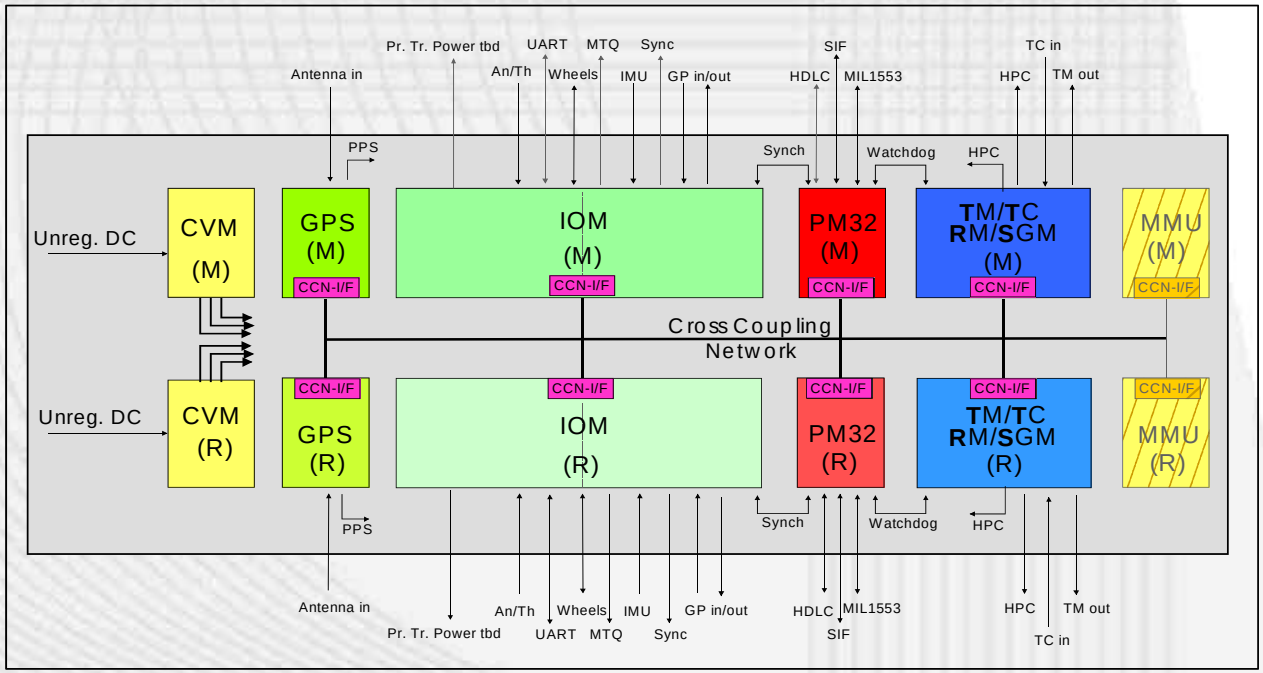
Core Functional Overview



OBC Concept -System Architecture-

Module Overview

- PM32: Processor Module
- TTRS: Telecommand / Telemetry / Reconfiguration / Safeguard Memory Module
- IOM: Actuator / Sensor Interface Modules
- MMU: Mass Memory Units (optional)
- GPS: GPS Receiver Module (optional)
- CVM: Power Converter
- Cross Coupling Network (CCN)

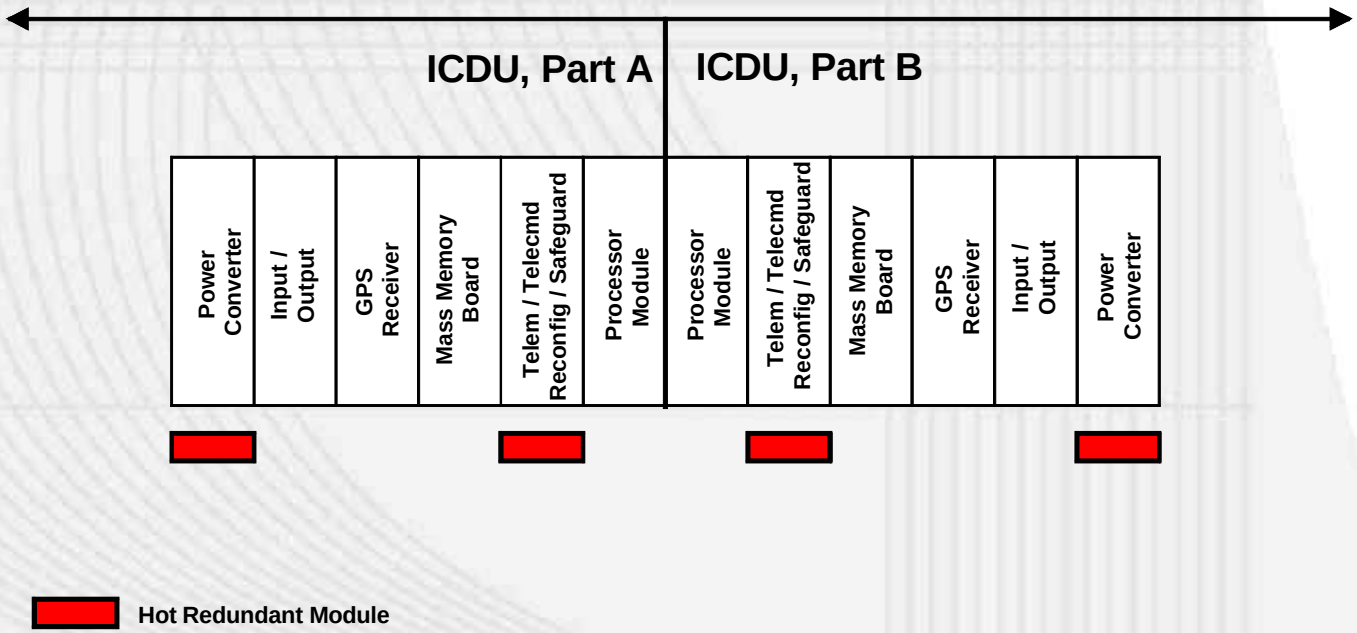


OBC Module Overview

OBC Concept -System Architecture-

Redundancy

- The arrangement of the box is such, that the main and redundant part of the modules are separated
- Hot redundant modules are not located next to each other
- The box separation is optimised regarding number of interfaces between modules (maximum between TTRS and PM32), thermal issues and backplane flex structure
  ⇨ maximum of power lines at outer end of the box, maximum of signal lines in inner part of the box



OBC Concept -Mechanic-

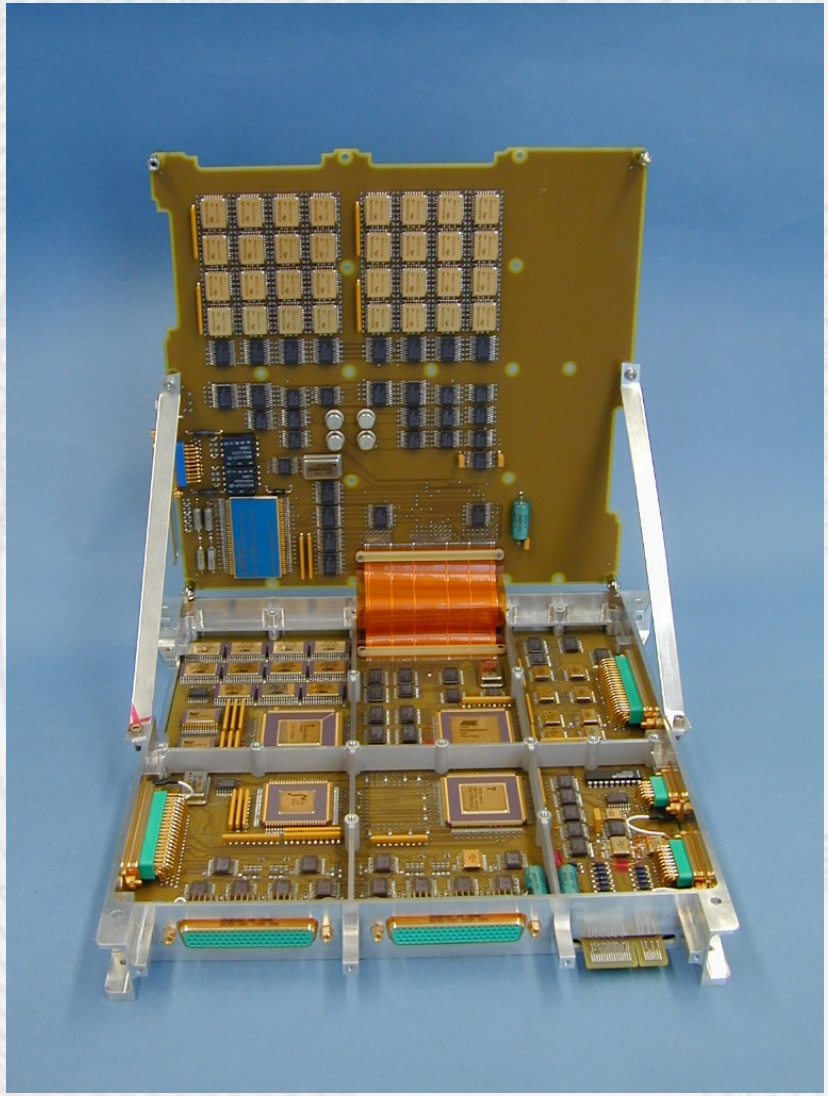
Overview

- Modular approach
- Several modules connected to each other on the front and back sides
- Left and right side modules carry additional plates to close the box
- A top plate covers the box internal cross-coupling network
- Each Module is screwed to the S/C structure to achieve a maximum thermal connection of each module to the structure

⇨ By this design every module can be treated (almost) as a thermal and mechanical self-standing system with reduced cross-coupling effects.

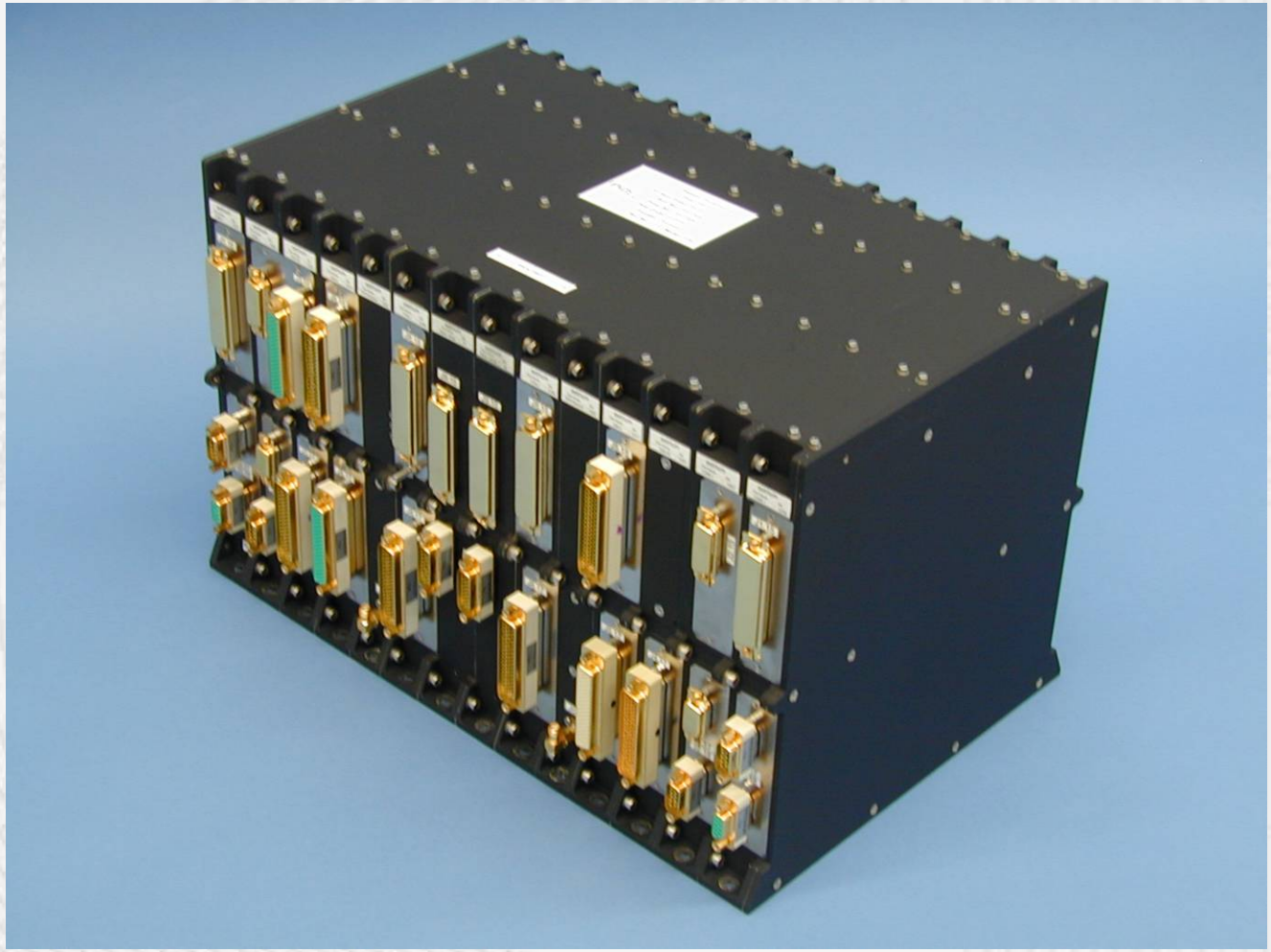
OBC Concept -Mechanic-

Module Frame



PCB Example (PM32)

OBC Concept



TerraSAR-X OBC

Processor Module PM32

PM32 -Functions (1)-

- **Sparc V7 based 32-bit RISC Processor (ERC32/TSC695F)**
- **Memory**
  - non-volatile start-up PROM
  - SRAM
  - non-volatile EEPROM in flight program-able
  - Dual Port RAM (DPRAM)
- **Clocks**
  - 40 MHz crystal oscillator ⇒ appr. 12 - 16 MIPS@SYSCLK 20MHz, 10 MIPS required at least
  - Timer
  - External Watchdog trigger (“alive” signal)
- **Input/Output**
  - full-duplex HDLC interfaces
  - multiplexed half-duplex HDLC interfaces
  - Reset

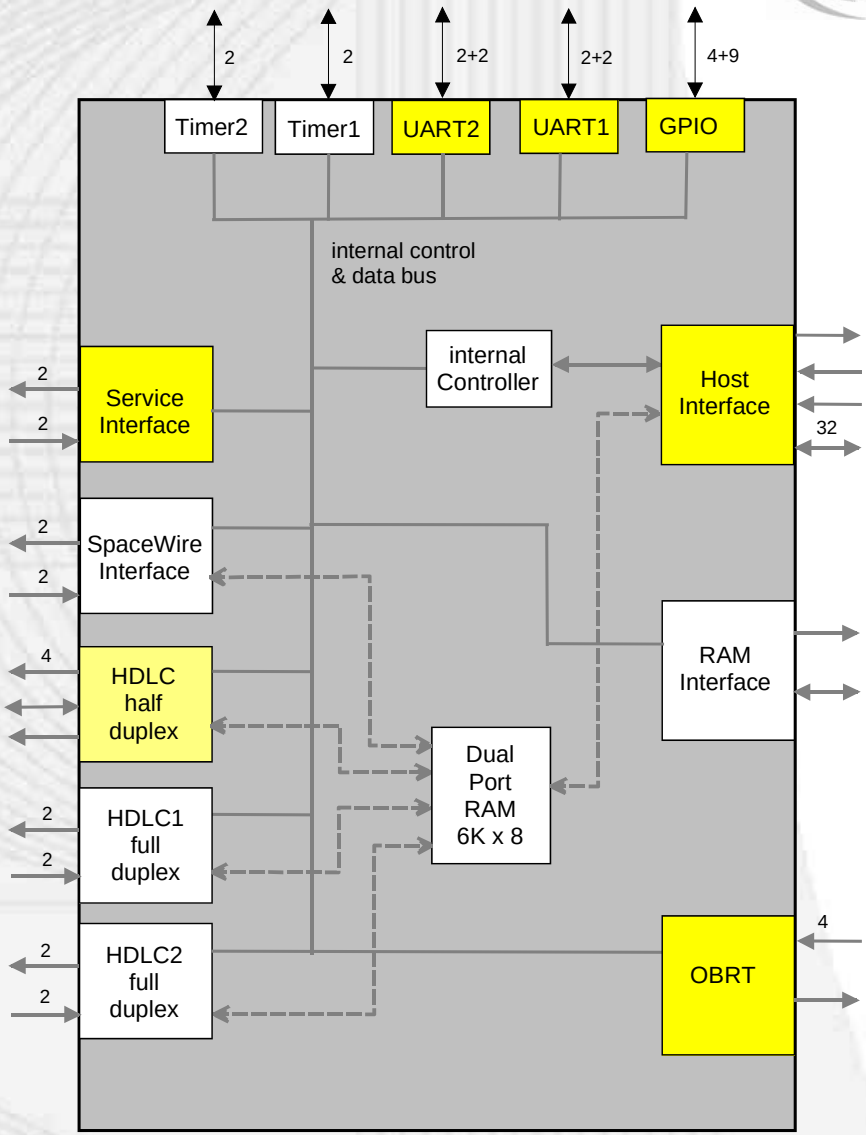
PM32 -Functions (2)-

- **Input/Output cont.**
  - 1355 interfaces
  - SpaceWire links
  - PPS
  - Synchronization
  - 1MHz precision clocks
  - MIL-STD-1553B bus
  - Separation
  - ERC32 -UART
  - Power
  - Select signals (out)
  - Timer
- **Test and maintenance**
  - Service-interface SIF
  - PM-PM interface

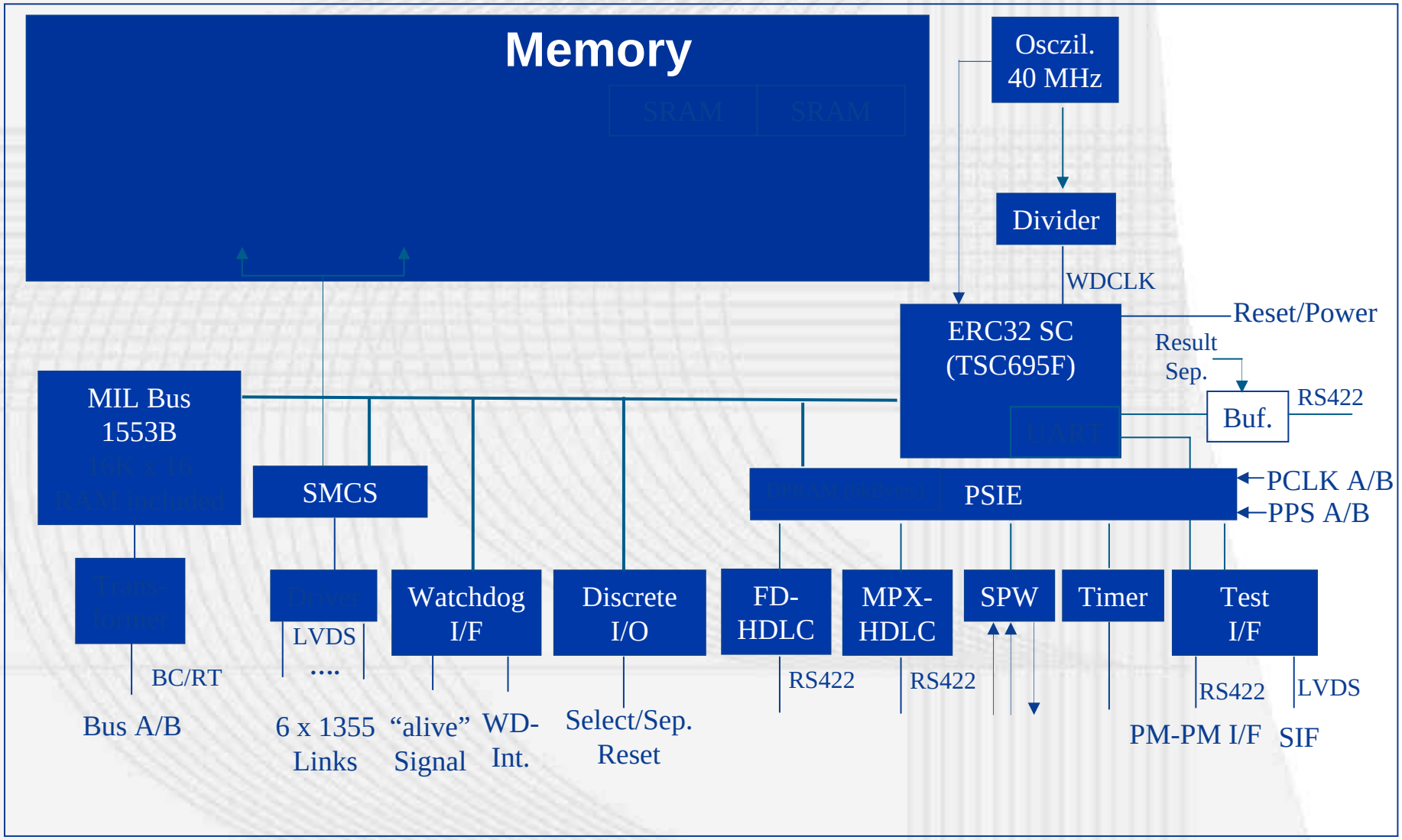
PM32 -PSIE-

- PSIE in Master Mode

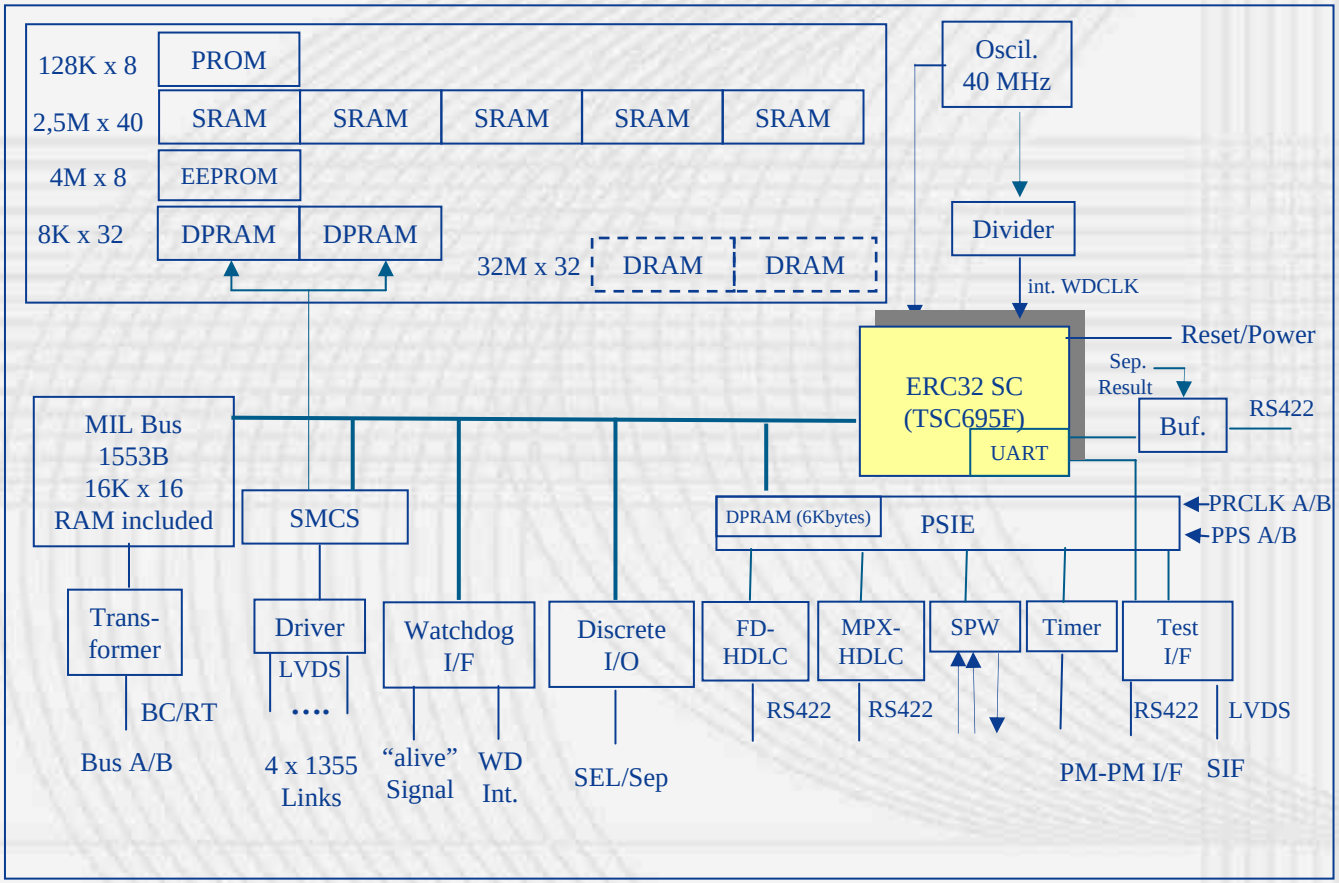
- SpaceWire
- RAM interface
- UART interface
- JTAG (IEEE 1149.1)
- General purpose I/O
- Timer / Event Counter
- Service Interface
- Half-duplex HDLC
- Full-duplex HDLC
- Host Interface
- OBRT generation



PM32 -Block Diagram Discrete-

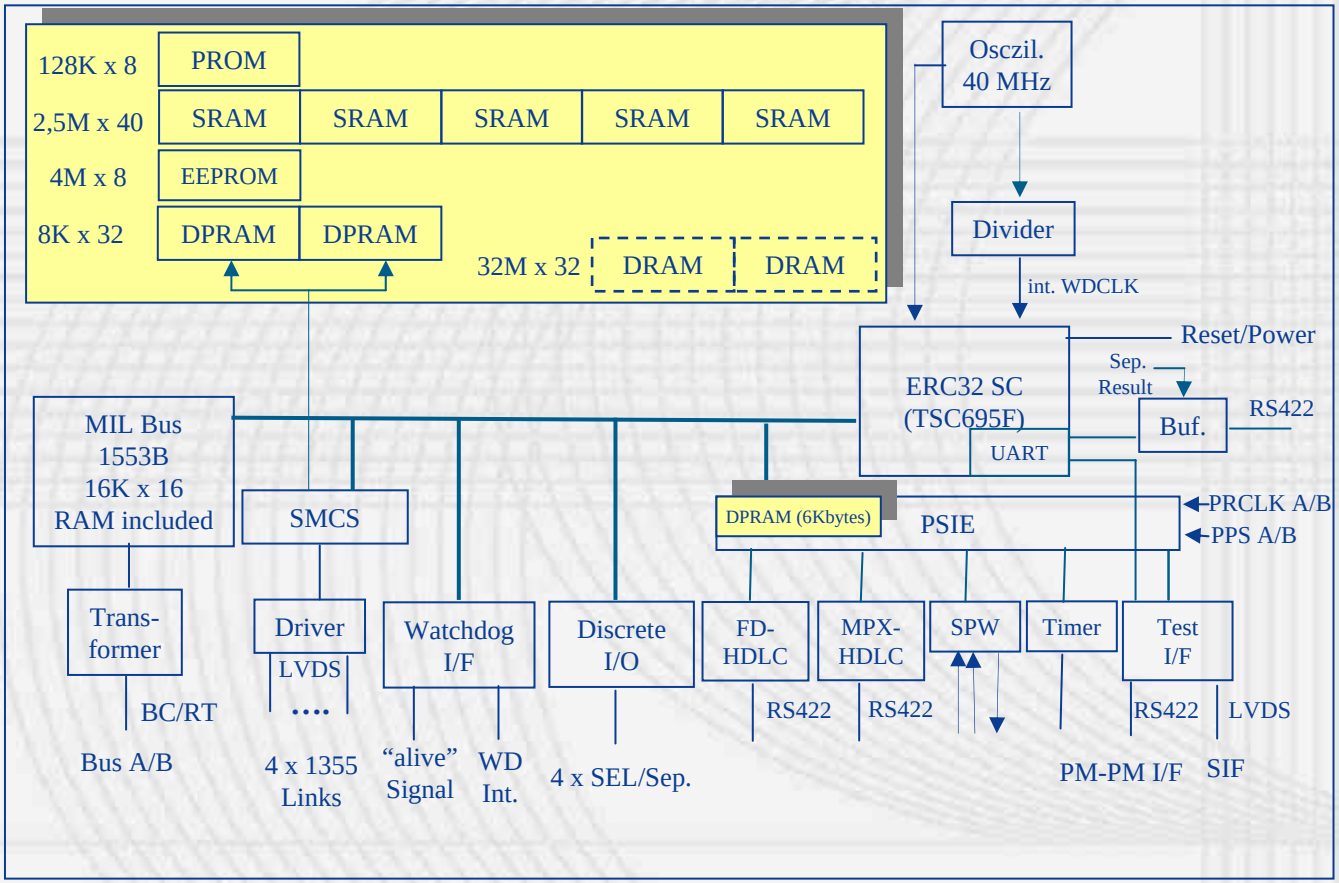


PM32 -Processor Functions-



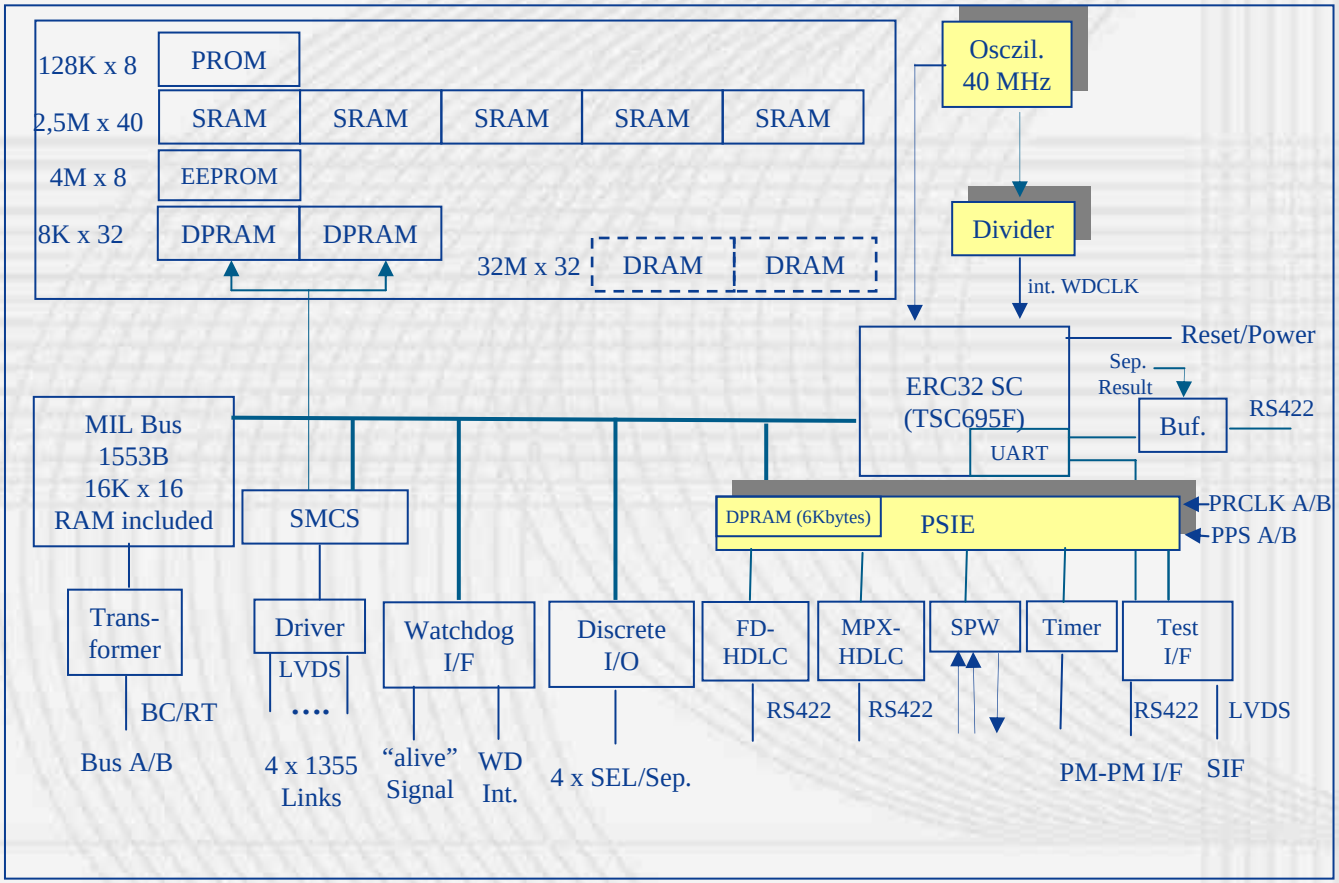
- ERC32 SC SPARC V7 RISC µProcessor
- 5 x User Interrupts
- 1 x non-mask able Interrupt
- 2 x UARTs
- Internal Watchdog
- EDAC and Parity
- Timers
- JTAG
- …

PM32 -Memory-



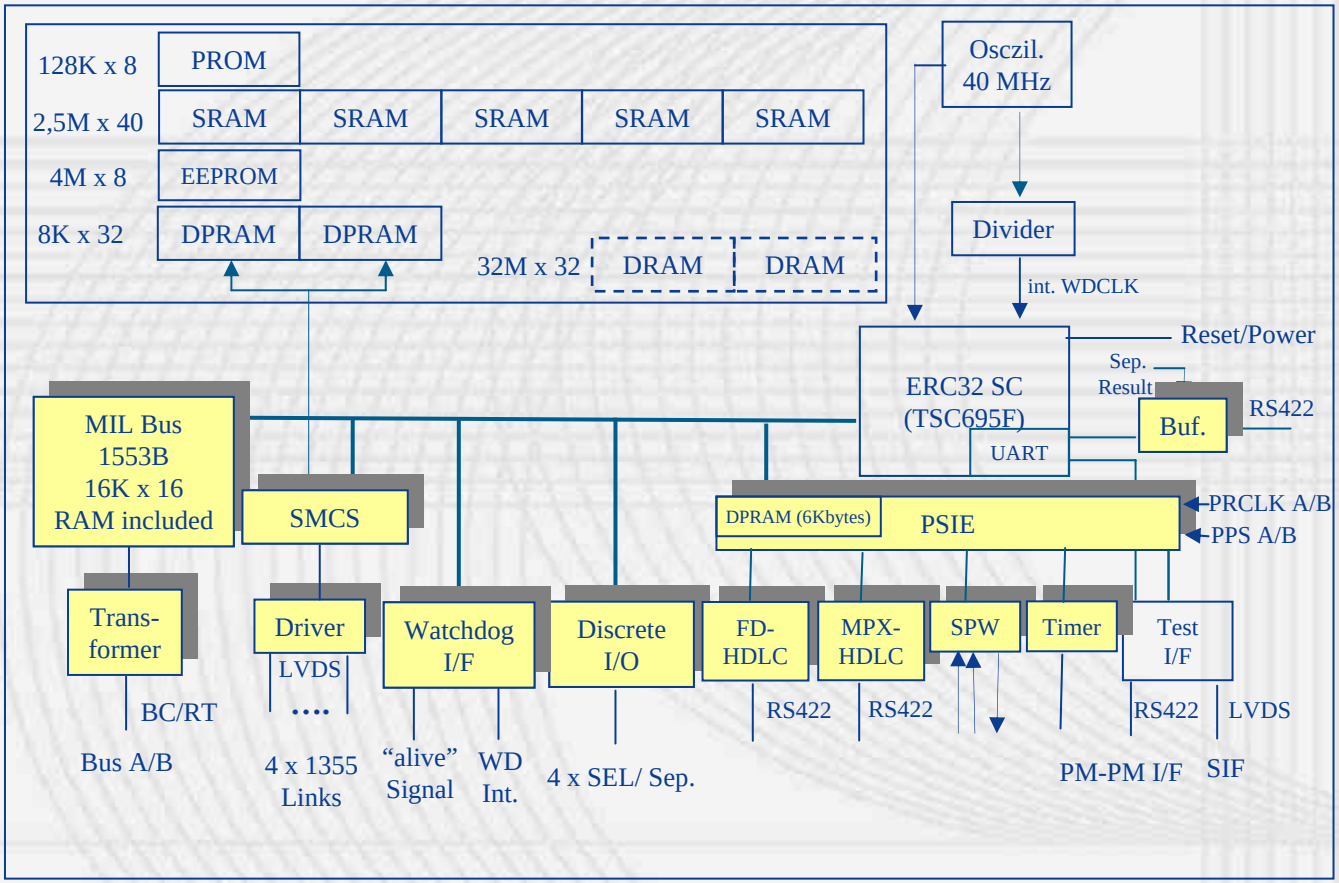
- Up to 128K x 8 Startup-PROM
- Up to 2M x 40 EDAC protected SRAM organized in 4 banks; 0 Waitstates
- 0,5M x 40 EDAC protected SRAM as redundant bank
- 32M x 32 protected DRAM (MCM)
- Up to 5M x 8 EEPROM organized in 2 separate banks.
  - each bank is power-switch able separately
  - enable for in flight programming by ground command
- 8K x 32 DPRAM for data-transfers with the SMCS
- 6Kbytes PSIE internal DPRAM

PM32 -Clocks-



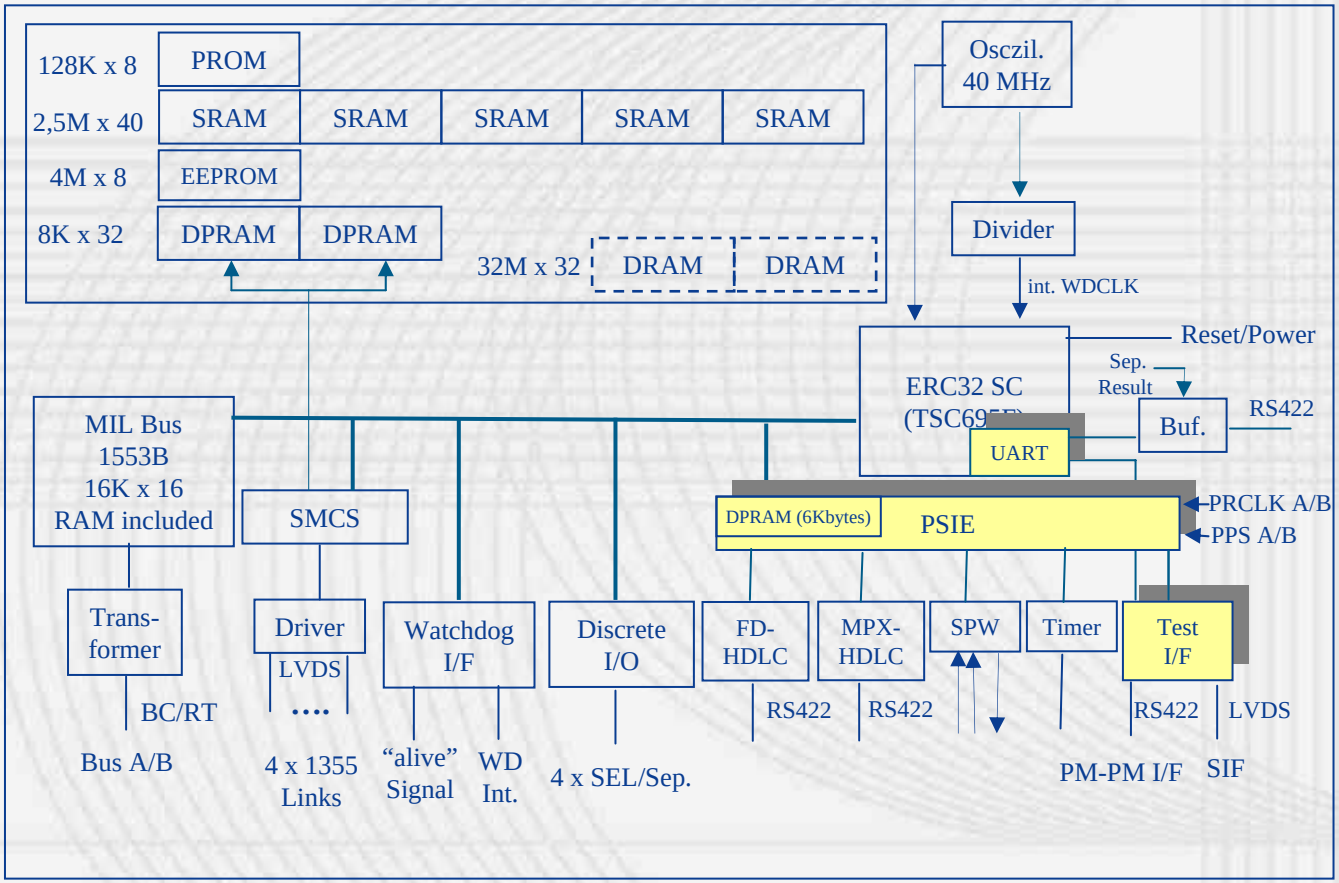
- 40MHz oscillator
- Divider by 10 for using the internal Watchdog (not baseline)
- Switching logic with select-and status information for determining the clock source (Intern or PCLK-A or PCLK-B) realized in the PSIE
- 2 PPS Inputs (RS422)

PM32 -Input / Output-



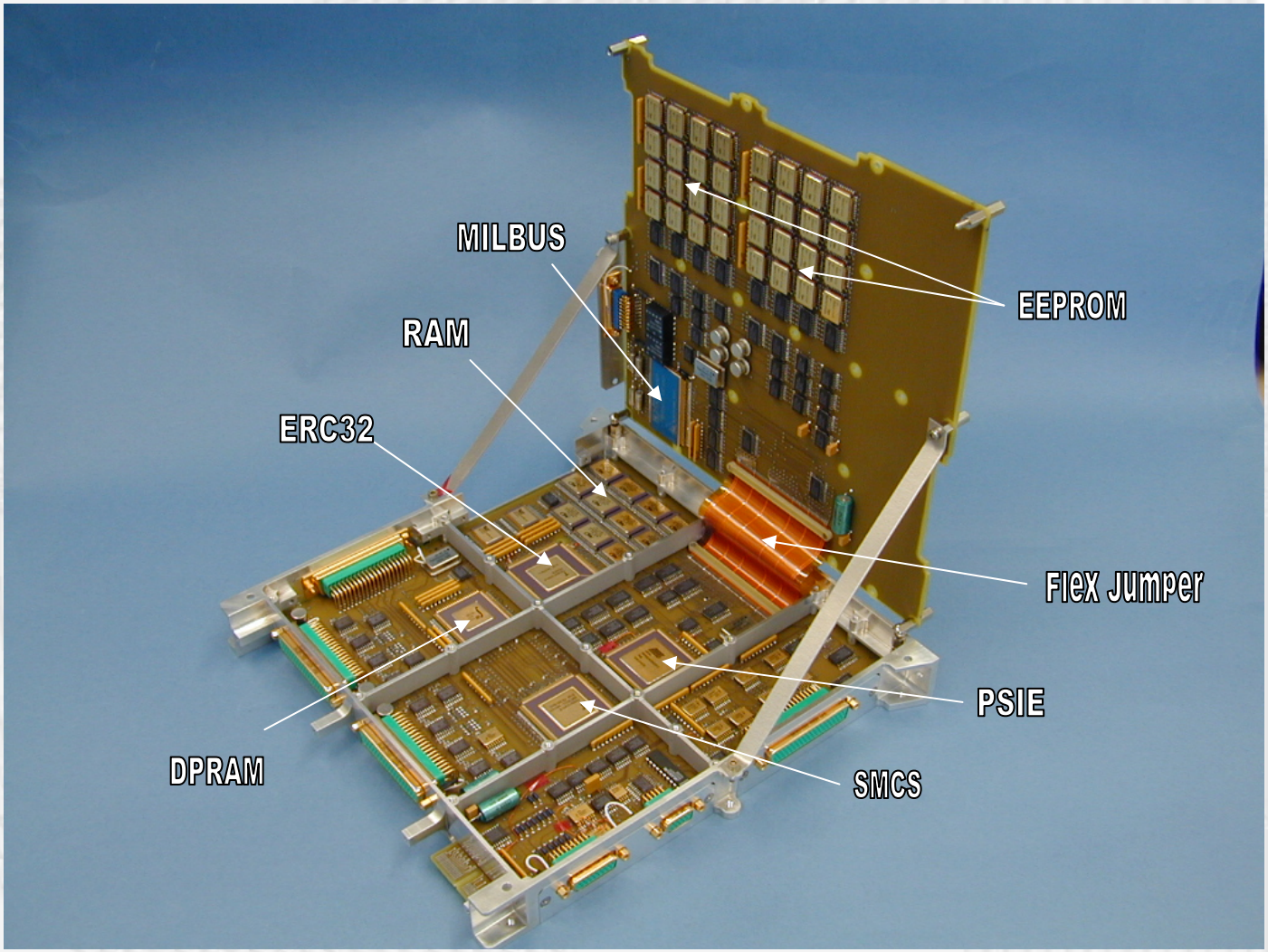
- Mil-STD-1553 Controller
  - with isolation transformer in long-stub configuration
  - BC/RT/BM feasibility
  - dual redundant buses
  - Internal Communi-cation RAM
- 6 x 1355 Links with LVDS
  - 2 links hot-redundant
- Discrete Outputs
  - 4 x Select outputs
  - 3 x Separation inputs
- Watchdog I/F sends out the "alive" signal and receives a ext. WD-interrupt
- 1 x ERC32-UART enabled by the separation result
- 2 full-duplex HDLC I/F
- 8 half-duplex-multiplexed HDLC I/F
- 2 "cold-redundant" SpaceWire with LVDS
- 2 Timers (PSIE)

PM32 -Test Interface-



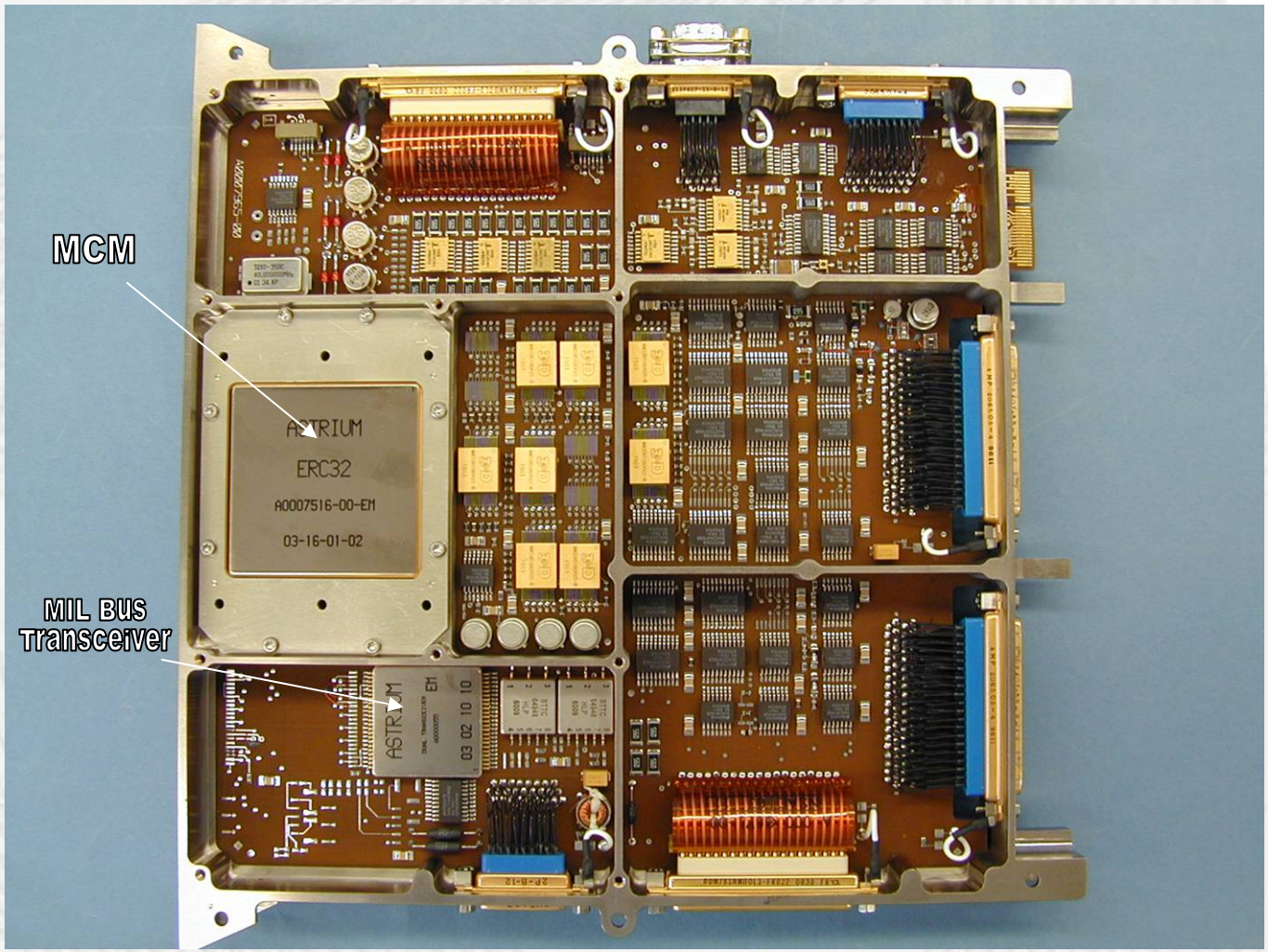
- PM-PM I/F for interchanging data's between the two PM-Modules. (One Module is on control and the other module is in Testmode)
- In Testmode all I/F are disabled, except the PM-PM I/F and the MIL-Bus in RT-configuration
- SIF (Service Interface)
  - Downloading
  - Debugging
  - Monitoring
  - galvanically isolated (realized in the SIF-box)
  - hot plug-able
  - 1 x ERC32-UART (used for test-software)
  - disabled, when no connector is plugged-in
- Hardware Debug

PM32 -Pictures (1)-



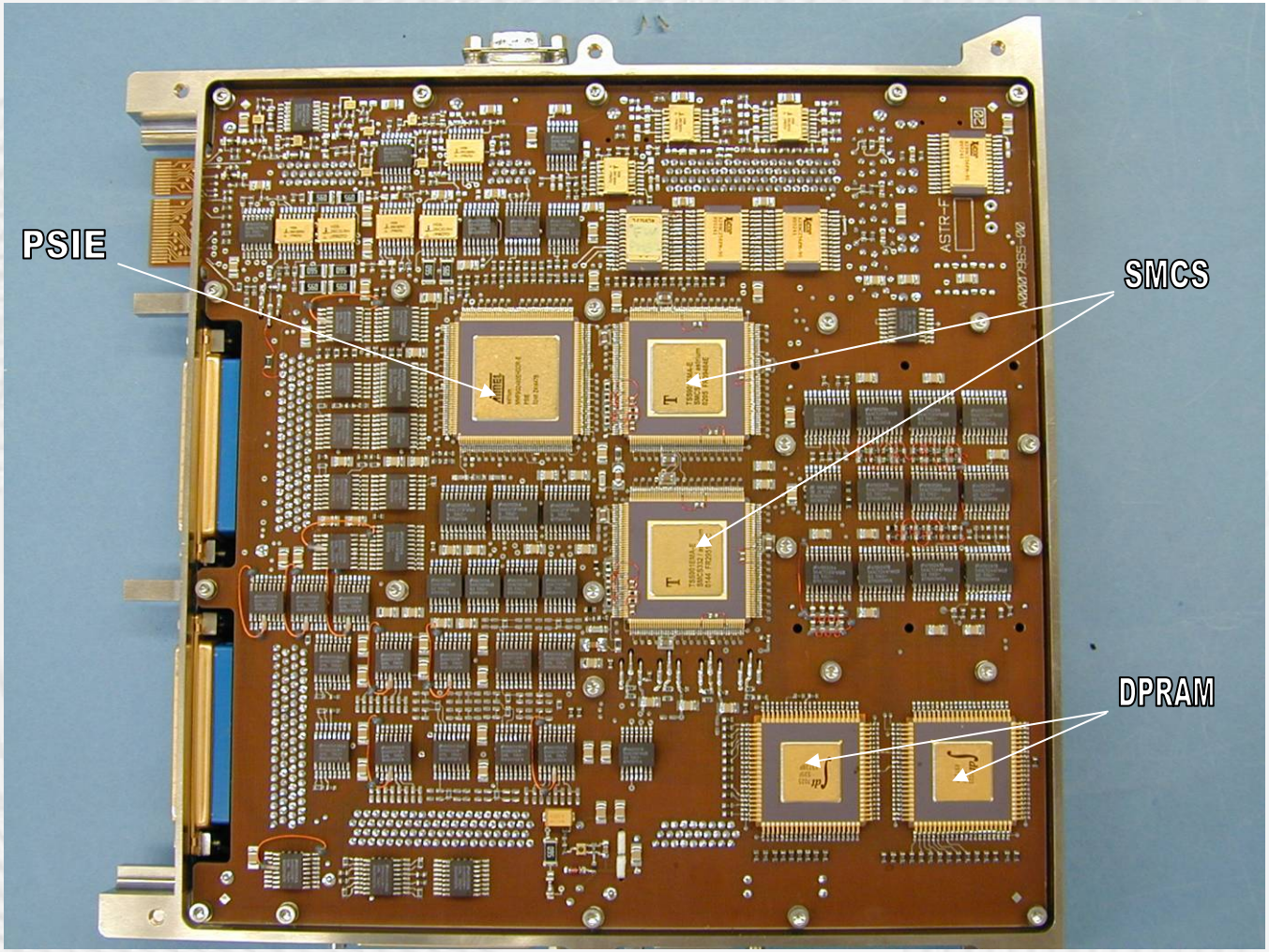
Discrete PM32: Top View LP1/LP2

PM32 -Pictures (2)-



MCM PM32: Top View

PM32 -Pictures (3)-



MCM PM32: Bottom View

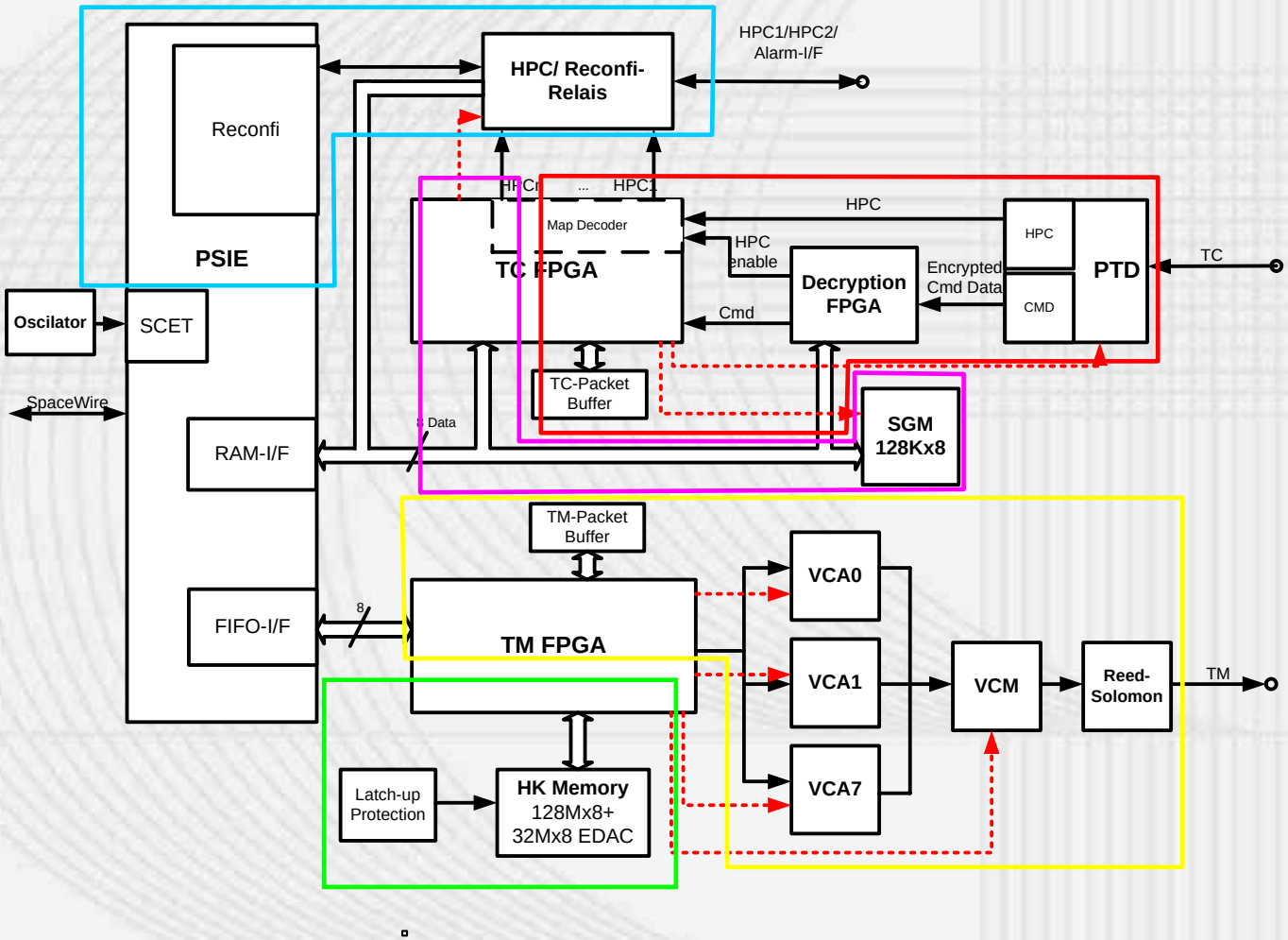
Telecommand/Telemetry/Reconfiguration/ Safeguard Memory Module TTRS

TTRS: Function

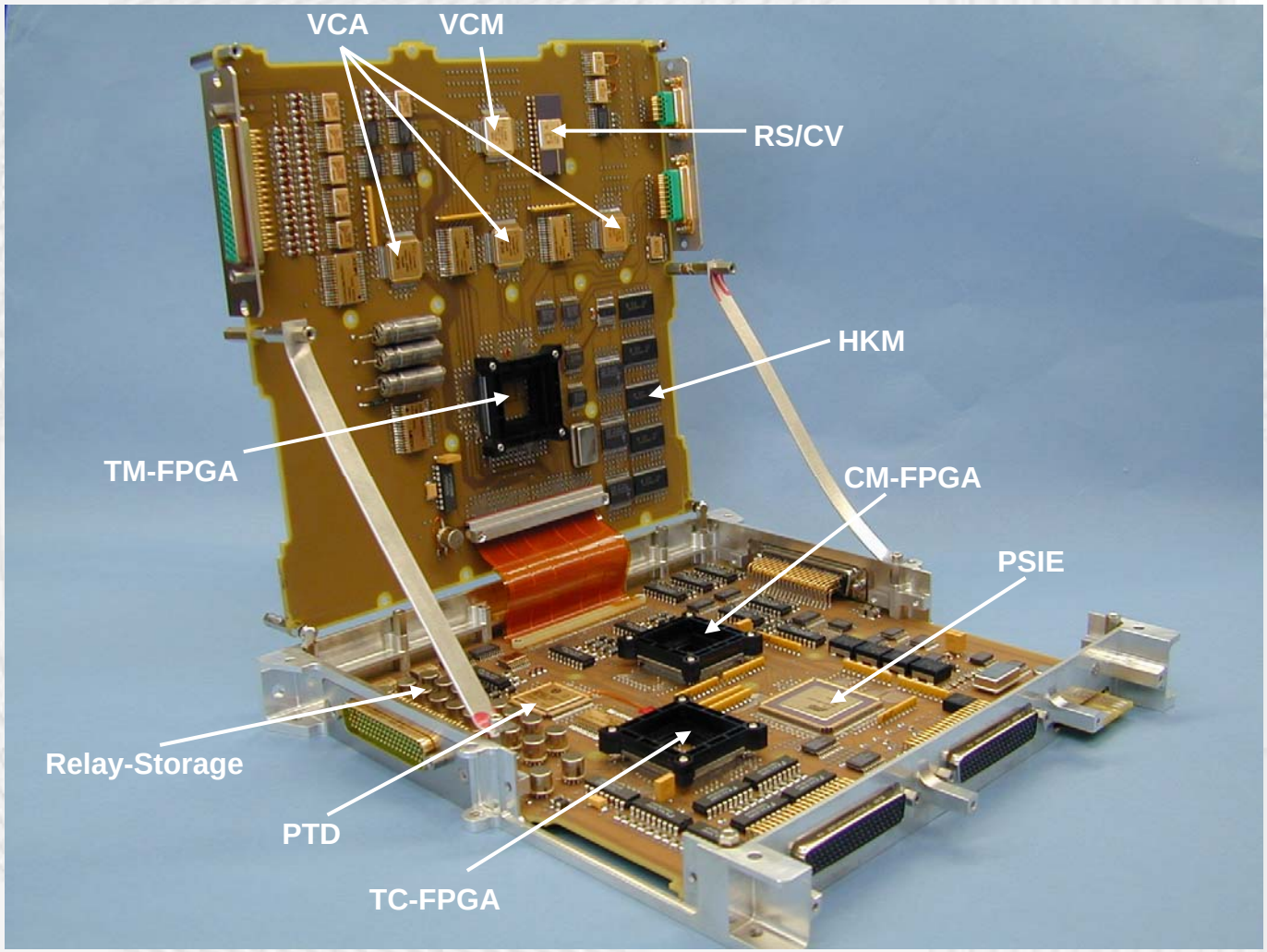
- Receive telecommands, generate packets to be sent to the PM32
- Generate High Priority Commands (HPC) by telecommands or PM32
- Telemetry data coming from active/inactive HK memory or PM32
- Provision of surveillance and reconfiguration logic
- Safe Guard Memory
- Housekeeping Memory
- Space Craft Elapsed Timer (SCET)

- Prevention of Single Point Failures (SPF) guaranteed by HW design

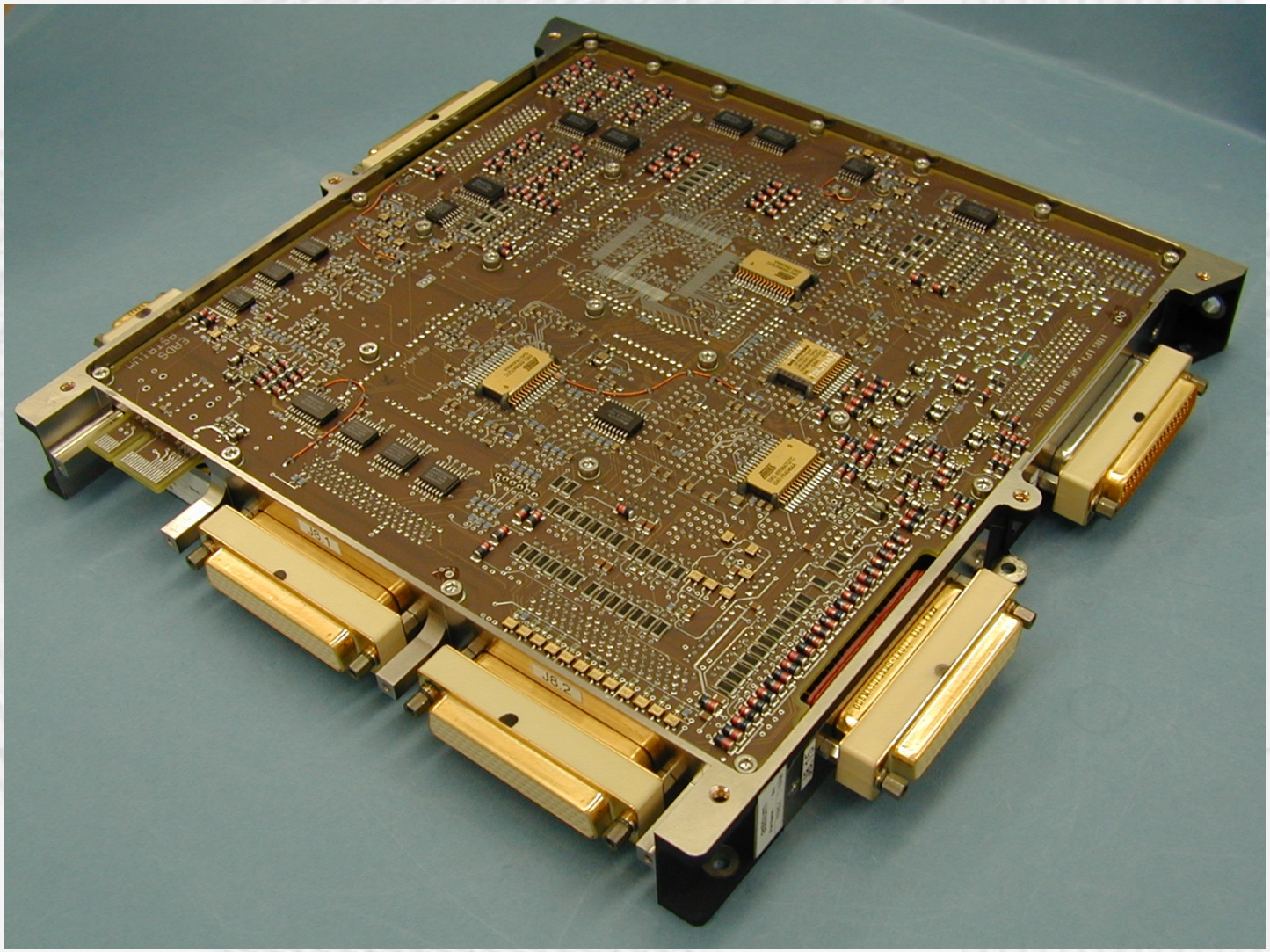
TTRS Overview



TTRS-EM-Module



TerraSAR-X FM Module



Input- Output Module IOM

IOM -Overview-

- **Two independent redundant IOMs**
- **Provides all interfaces between the OBC internal CCN and the**
  - **AOCS**
  - **Data-Handling**
  - **scientific equipment.**

- **The IOM is physically divided into 2 modules**
  - Analog
  - Digital

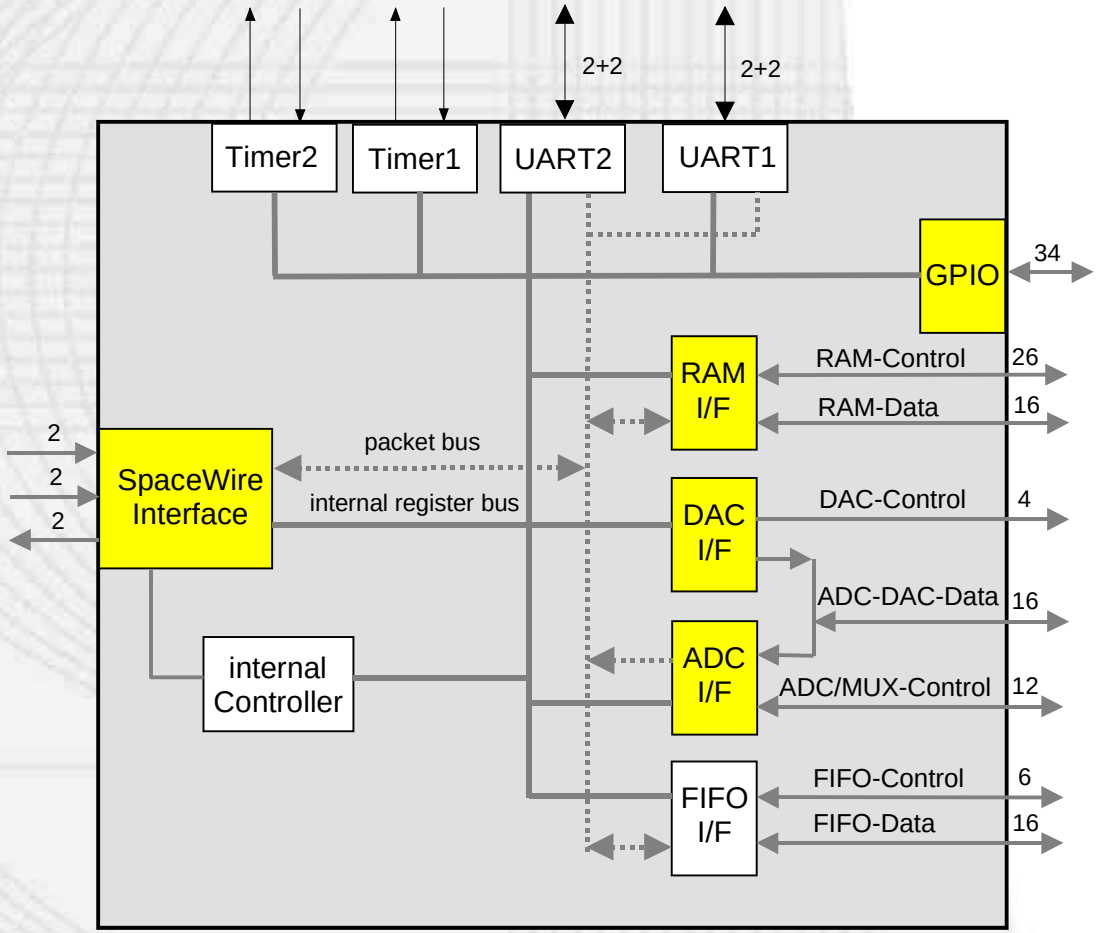
IOM -Function-

- Following capabilities are implemented:
  - Serial Asynchronous UART Interfaces
  - Synchronization Interface
  - Serial IMU interface (reduced SDLC protocol)
  - RS422 Input/output Interface
  - Relay Status Interface
  - Magnetorquer Interface
  - Analogue Input Interface
  - Thermistor and Coarse Earth Sun Sensor Interface
  - Wheel Interface

IOM -PSIE-

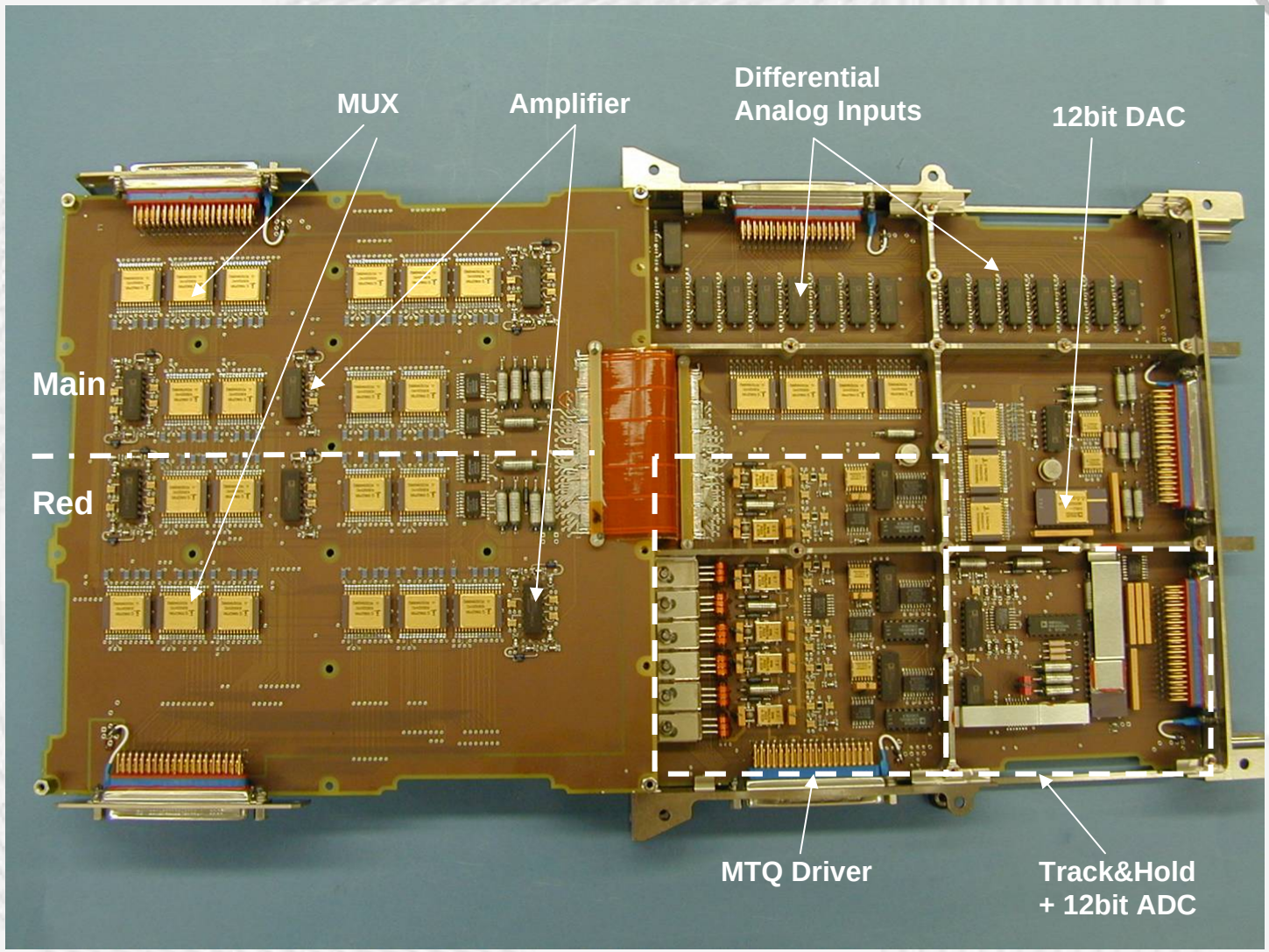
PSIE in SpaceWire-Remote-Mode

- SpaceWire
- FIFO interface
- ADC interface
- DAC interface
- RAM interface
- UART interface
- JTAG (IEEE 1149.1)
- General purpose I/O
- Timer / Event Counter



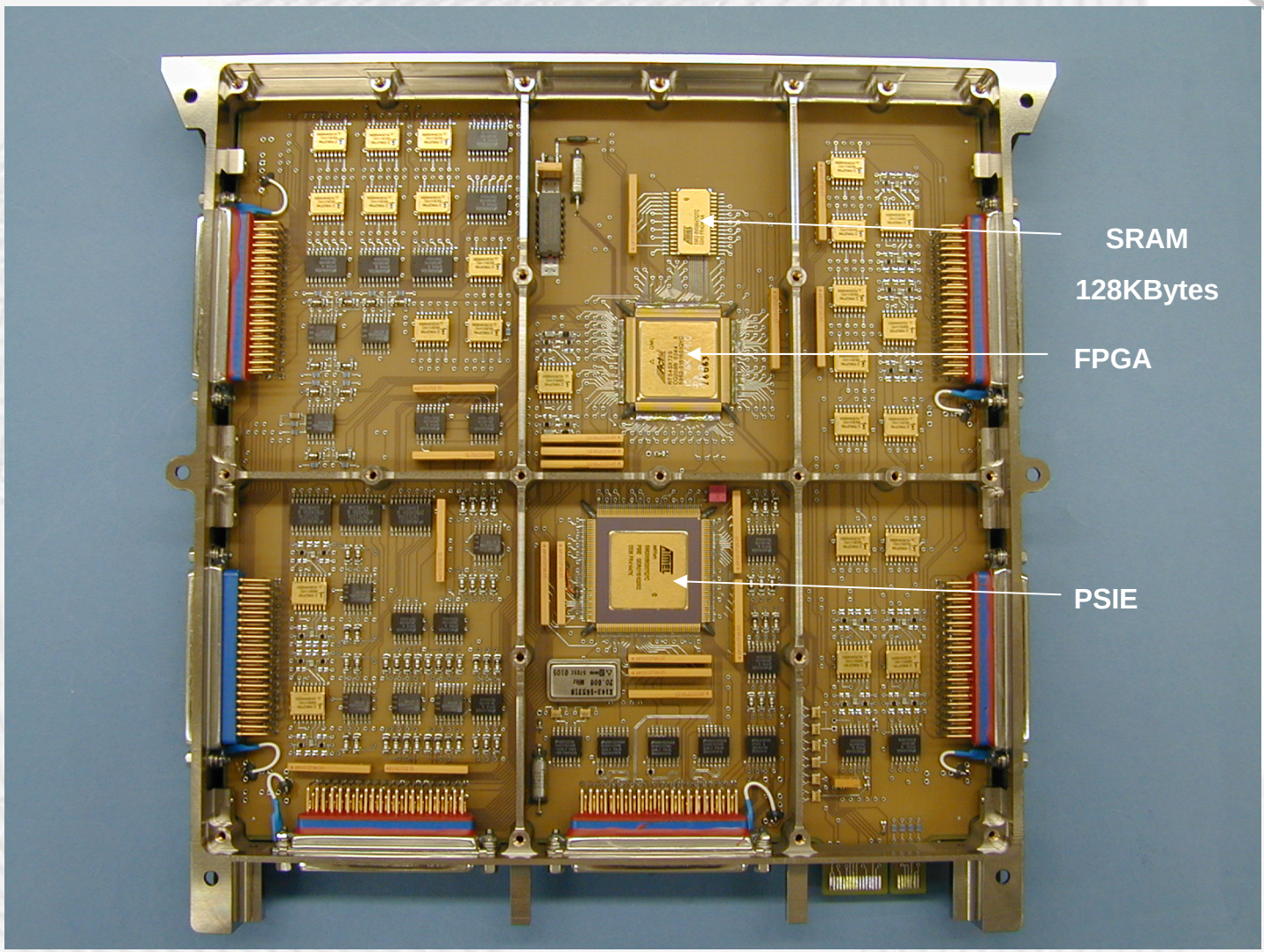
MODE: Remote SpaceWire

IOM-A -Picture-



IOM-A: LP1 and LP2

IOM-D -Picture-



IOM-D: LP1

Converter Module CVM (Power Converter)

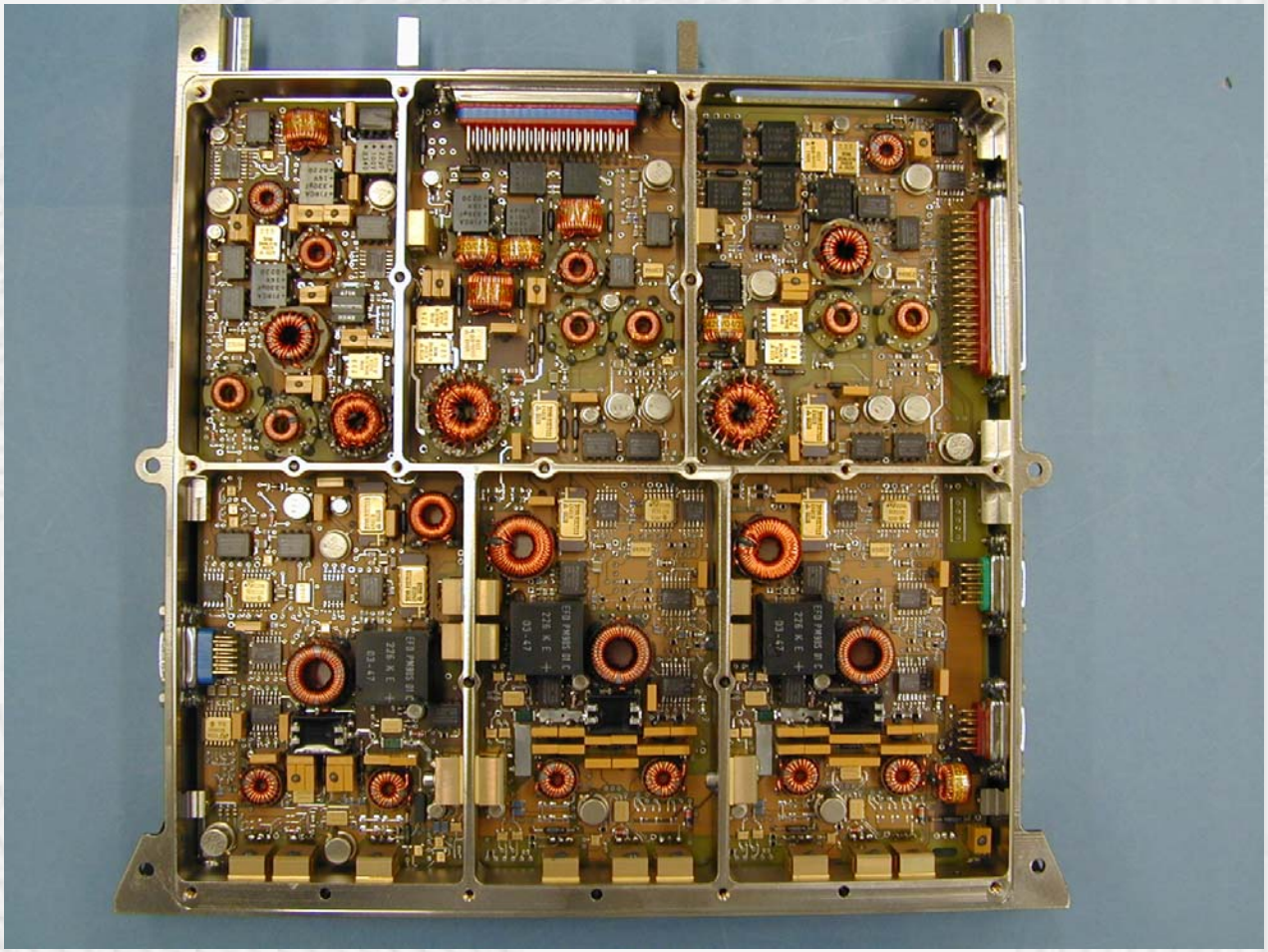
Converter Module CVM

- The CVM power module consists of 3 independent power converters
- Each power converter is dedicated to one box module (TTRS, PM32, IOM)
- 2 Converters (PM32, I/O) can be switched on/off by TTRS- Commands via latch-relays. Relays status signals are generated and is be monitored by the I/O module.
- The TTRS module Converter is hot redundant, not switchable.
- Wide input voltage range 18 V to 50 V DC.
- Operating temperature range - 45 °C to + 80 °C
- separation I/F with 2 of 3 voter for TTRS and PM32-Converter

Converter Module CVM

- Compensation of SEE especially SET effects included in design
- Control loop stability verified by worst-case analysis and supported by measurement
- Output & input impedances of different converter stages matched to avoid oscillations (e.g. input filter – main converter)
- Parts de-rating according to ECSS-Q-60-11 A

FM Module



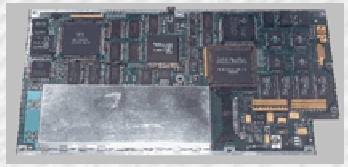
GPS Receiver Module GPS Rx

GPS Rx -Features-

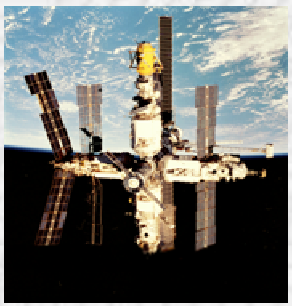
- Low cost single board GPS L1 C/A code receiver for space applications
- Part of a modular spacecraft AOCS or stand-alone usage
- Acquiring and tracking up to 8 GPS satellites
- Configurable for LEO, MEO, and GEO
- Software based signal processing
- Processes weak signals
- Dynamic navigation solution provides PVT even with less than four GPS satellites
- Synchronization to GPS time by a one Hertz Time Mark Pulse
- Based on Mosaic020 DSP technology with radiation tolerant, hi-rel components
- Single or fully redundant configuration
- Next receiver generation will be compatible to Galileo and modernized GPS.

GPS -Heritage-

Airborne GPS/GLONASS Rx



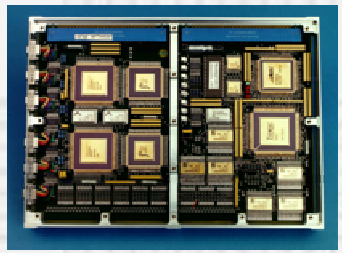
ASN-22



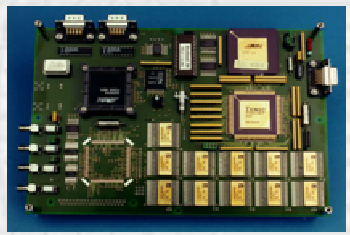
ASN-22 has been flown on MIR
Photo NASA

Experience

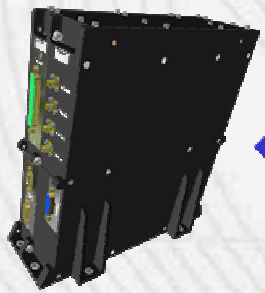
Radiation tolerant DSP board



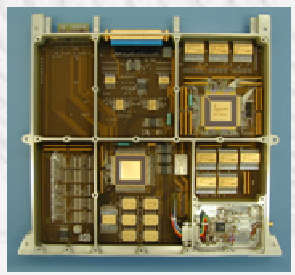
Mosaic020



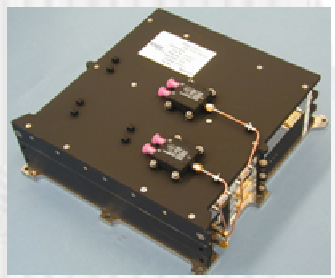
MosaicGNSS Rx DM



GPS/AODS Demonstrator

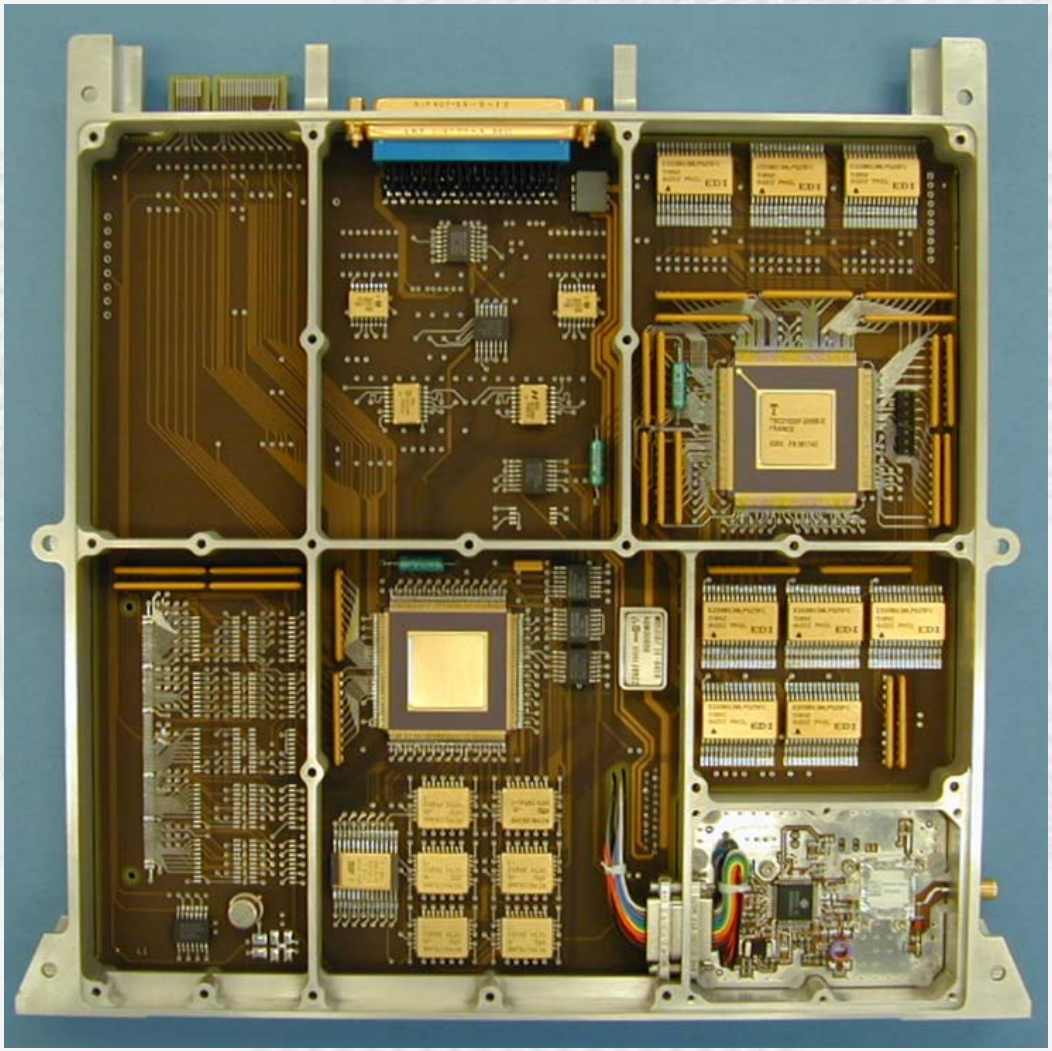


MosaicGNSS Rx FM Slide-In Module for TerraSAR-X



MosaicGNSS Rx FM Stand-Alone Box for SAR-Lupe & ADM-Aeolus

GPS Rx for TerraSAR-X



Test	AvNG I/O	PM DSP
Ext. Conn.	GPS PSIE ASIC EEPROM	DM RF FE