Video Processing Chain VPC2

SpaceWire Networking Protocol Meeting 4

19-20-21 July 2005

Summary

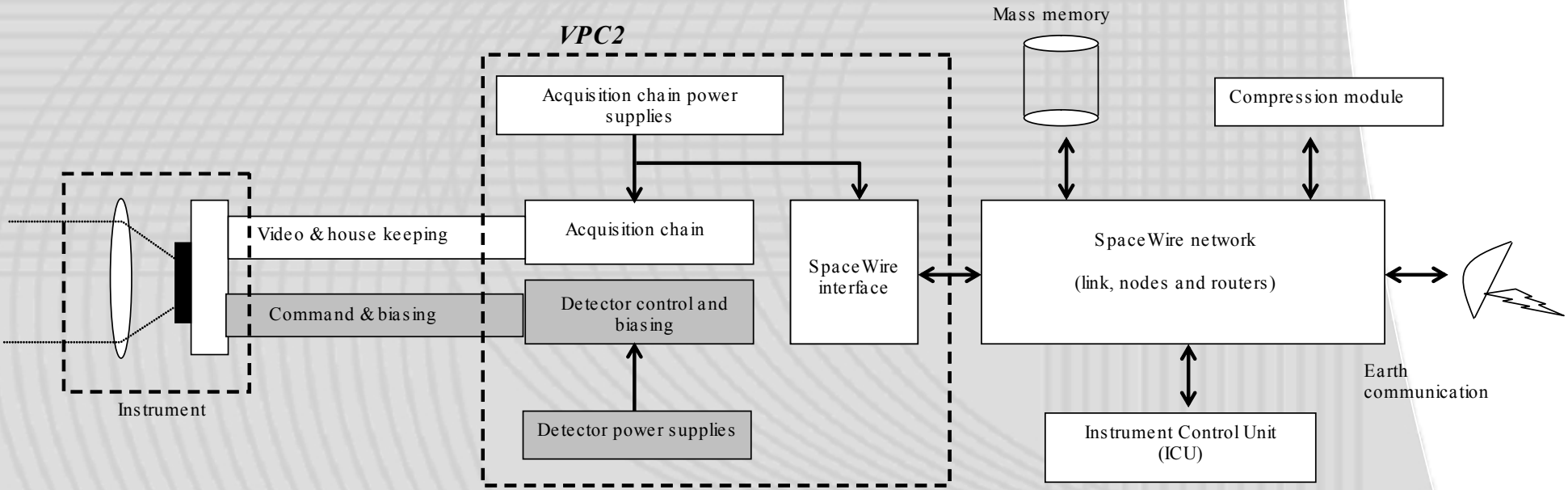
- VPC2 and SPADA_RT Activity
- VPC2 Architecture Data Exchange
- VPC2 RMAP
- Implementation Issue
- FPGA Implementation Issue
- Expected Performances Issues

VPC2 Activity

- The VPC2 is dedicated to earth observation science mission.
- It shall provide fully characterized and standardized ready to use functions to interface electro-optical detector in one end and a standardized SpaceWire network on the other end.
- Main motivation of the VPC2 development is to reduce development effort following the mission requirement without impacting performances:
  - Analog treatment supported by a general ASIC (SPADA_RT).
  - External ADC and DAC.
  - Fully autonomous running during image acquisition.
  - Fully standard network and protocol (SpaceWire / RMAP)

VPC2 Activity : General block diagram

→***Separate detector dependent and independent parts.***



White blocks: re-used whatever the mission

Grey blocks: Optimized following the mission

VPC2 Activity : Performances

Parameter	Objective	Remark
Pixel frequency	100KHz / 3MHz	100KHz of granularity
Accuracy	14 bits	
ENOB	≥ 12	At maximum gain
Missing codes	None	
Differential non linearity	± 0.5LSB of 12bits	
Integral non linearity	± 1LSB of 12bits	
Basic video signal processing	• Differential input. • DC restore (CCD case) or direct coupling (APS & HgCdTe) • CDS (CCD detector) or single sampling (HgCdTe detector) • Programmable gain. • Offset correction.	
Gain span	From 1V/V to 8V/V	
Gain granularity	1V/V	
Number of detector input	≥ 2 (3 as objective)	Each input is read sequentially
Number of house keeping signals	4	
I/O control	Space wire	
Input dynamic	≥ 2V	
Gain error	<1%	
Gain stability	<400ppm	On the complete thermal range
Offset error	<125ppm	Defined for the maximum output range
Offset stability	<125ppm	On the complete thermal range
Power consumption	1.7W	Detector independent part
Operational temperature range	0°C / 30°C	
TID	30KRad	
Latch-up threshold	>70Mev/mg.cm²	
Effective LET	<1E-7	At saturation level

SPADA_RT

- The SPADA_RT (Signal Processing ASIC for Detector Array _Radiation Tolerant) ASIC is an analog front end, dedicated to CCD or APS detector.

- This project has been initiated after a first VPC contract during which a first SPADA ASIC was developed but not manufactured due to technology disappearance (DMILL). Several performances have been improved.

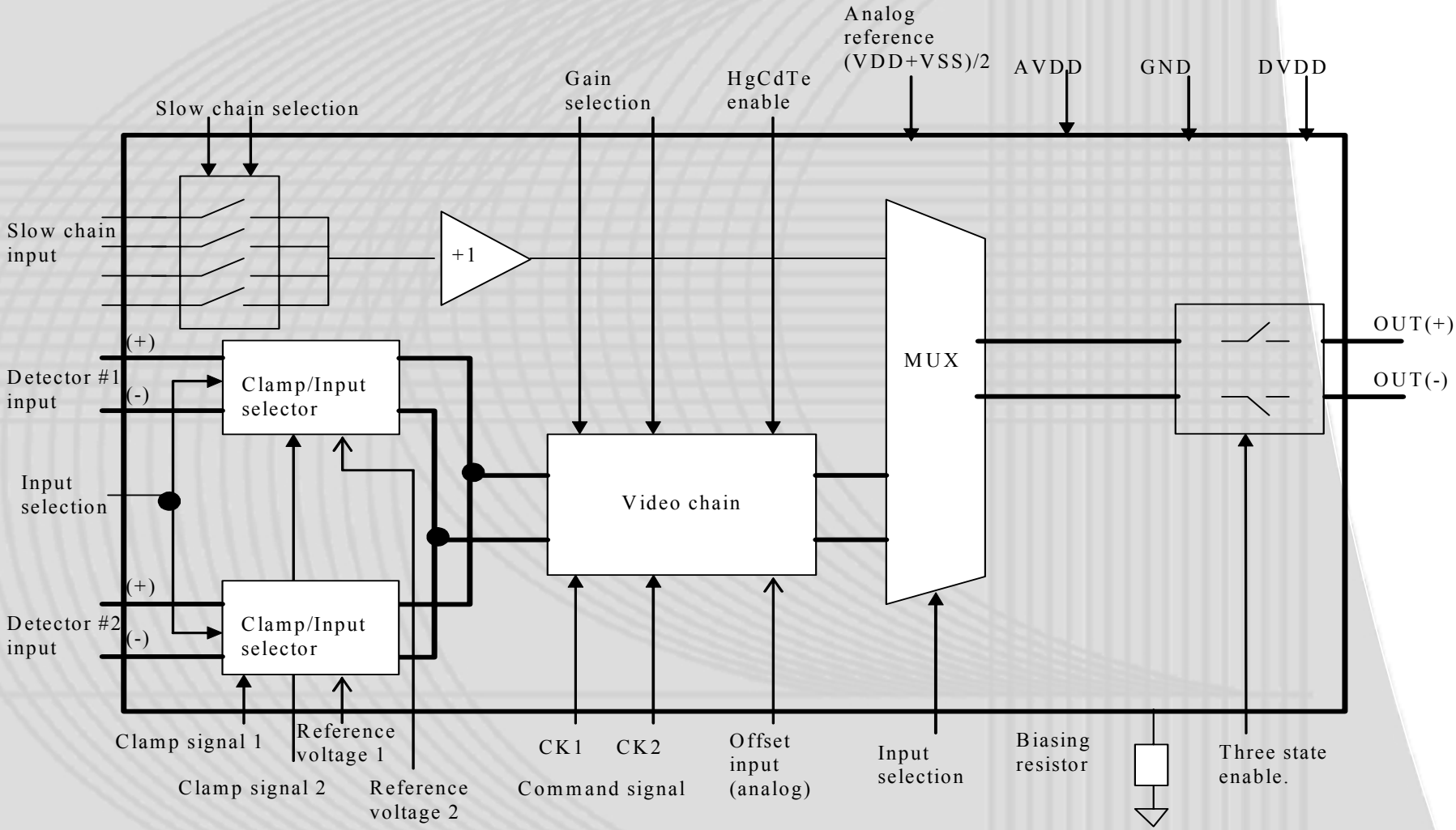
- Technology chosen shall be a commercial European one. Thus the SPADA_RT development includes hardening tasks.

SPADA_RT functional specifications

- The SPADA_RT ASIC contains all facilities to:
  - Performs analog treatment needed by CCD or APS detector (2 inputs):
    - CDS or single sampling.
    - DC restore (CLAMP at line frequency)
    - Offset injection.
    - Sample and hold.
    - Variable gain (from 1V/V to 8V/V)
  - Ensure buffering of 4 house keeping signals.
  - Be inserted in a multiplexing architecture (analog three state).

- The SPADA_RT is optimized to be used within the VPC2 chain, SpaceWire detector module.

SPADA_RT preliminary block diagram



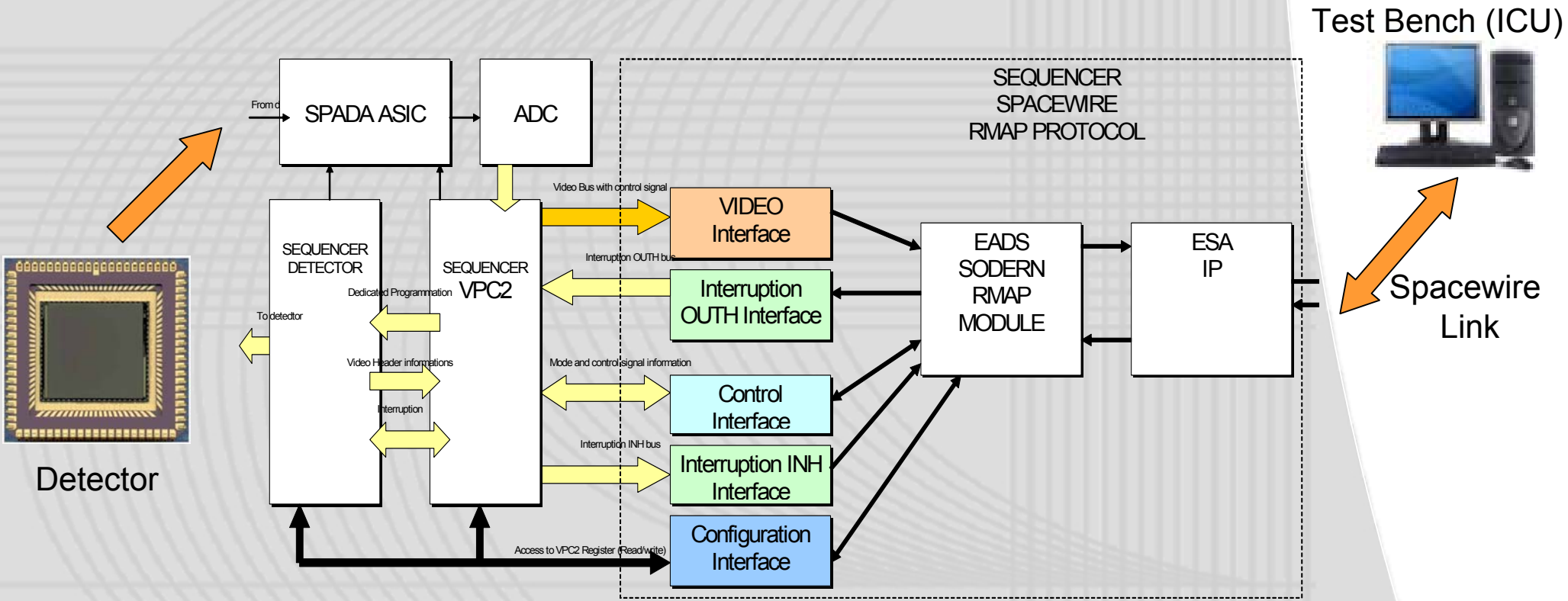
VPC2 Architecture Data Exchange

- Data organization reflect the hardware one: three independent sequencing level:
  - SpaceWire sequencer.
  - VPC2 sequencer.
  - Detector sequencer.
- Once again, our approach is to propose modules, ready to use and easy to modify without impacting the others.
- All inputs and outputs data uses the same SpaceWire link.

VPC2 Architecture Data Exchange: Characteristics

- Spacewire ECSS-E-50-12A
- ESA IP core (UoD)
- RMAP protocol
- Spacewire and VPC2 baseline 100 Mbits/s (up to 200 Mbits/s)
- Configuration of VPC2 registers
- Store video samples in memory (ICU Test bench)
- No embedded processor

VPC2 Architecture Data Exchange : Overview



VPC2 SPACEWIRE RMAP:

- Remote Memory Access Protocol : ECSS-E-50-12 Part 2 Draft C 29/03/2005
- ESA IP SPACEWIRE core from UoD
- RMAP core development from EADS SODERN (bridge between Spacewire world and VPC2 world)
- All VPC2 registers and picture acquisition are programmable via SPACEWIRE
- VPC2 writes video samples in RMAP command format directly towards ICU
- RMAP Error management
- All RMAP command supported except Read-Modify-Write

Implementation Issue : FPGA Choice and Hardware Information

- VPC2 requirements :
  - Military or space components => ACTEL
  - Reprogrammable => ACTEL PROASIC
    (Roadmap ACTEL on Rad Tolerant PROASIC3E RTPA3/E)

- Area Sparing : No configuration Prom

- ESA IP with ACTEL PROASIC : 100 Mhz on TX clock
  (limited by ESA IP TX state machine complexity and Actel PROASIC Architecture)

- Driver LVDS : High bandwidth (from AEROFLEX)
- Clocks :Internal PLL used or external AEROFLEX RADCLOCK
- VHDL development

Implementation Issue : Test Bench

- Operating system : Windows XP
- Testbench SpW adapter : SPACEWIRE/USB brick from Star Dundee
- Protocol : SPACEWIRE RMAP
- Mission : validate the digital part of VPC2 board, ICU emulator
- Store Video sample and generate result files
- Housekeeping data storage (temperatures, voltages)
- Error checking
- Time code handling

Implementation Issue : Test Bench Overview

VPC2 PC
test bench

USB cable

SPACEWIRE
USB BRICK

Spacewire Cable

VPC2
BOARD

STAR-Dundee

SpaceWire-USB Brick.

The SpaceWire-USB Brick is a small USB 2.0 box which provides an interface between a host PC and SpaceWire. It is powered from the host PC via the USB cable. The SpaceWire-USB Brick provides two SpaceWire interfaces each operating at up to 200 Mbits/s. Drivers for Linux and Windows are available. The linux driver supports TCP/IP over SpaceWire. These units have been designed for simple interfacing of host PCs to a SpaceWire network and to support high, continuous data rates into PC user memory.

Currently available, CE/FCC certified.

FPGA Implementation Issue : Logic Gates

- IP ESA + RMAP in different technology *:

- ACTEL ProaASIC3E A3PE600 : 2987 tiles (30 %)
- ACTEL ProaAsic Plus APA300 : 4613 tiles (56%)

*: synthesis result with Leonardo Spectrum

FPGA Implementation Issue : CRC

- CRC implemented in Hardware
- Based on : IEEE A symbol Base Algorithm for Hardware Implementation of Cyclic Redundancy Check (CRC) Rajesh Nair, Gerry Ryan and Farivar Farzaneh

- Results :

- ACTEL PROASIC plus APA300 : 82 gates (167 Mhz)
- ACTEL RTAX1000 : 93 gates (116 Mhz)

Expected Performances Issues : Network Load

Full Acquisition					
Useful pixels	**12000**	12000	12000	12000	12000
ADC Conversion time, Pixel period (ns)	**MAX SPEED 330**	660	1000	5000	10000
Header RMAP size (bytes)	**16**	16	16	16	16
Video data Paquet size (bytes)	**256**	256	256	256	256
SpaceWire coding(bits)	**10**	10	10	10	10
End of paquet (bits)	**4**	4	4	4	4
SpaceWire Link (Mbit/s)	**100**	100	100	100	100
total bits to send	**5284**	5284	5284	5284	5284
Nb of paquets by second	**18925**	18925	18925	18925,	18925,
Pixel rate (Msample/s)	**4,84**	4,84	4,84	4,84	4,84
VPC2 Complete Useful acquisition in (ms)	**3,96**	7,92	12	60	120
paquet duration (without RMAP header) in us	**84,48**	168,96	256	1280	2560
video data Paquet duration on SPaceWIRE in us	**52,84**	52,84	52,84	52,84	52,84
SpaceWire Network charge (%)	**62,54***	**31,27**	**20,64**	**4,12**	**2,06**

* : at 200Mbits/S the Network Load becomes 31.2%

Expected Performances Issues : Frequencies

- IP ESA + RMAP in different technology *:

	Sys	Rx	Tx
• **ACTEL ProaASIC3E A3PE600**	: 135	347	143
• **ACTEL ProaAsic Plus APA300**	: 57	120	115
• ACTEL RTAX1000	: 54	170	105

*: synthesis result in MHz, SDR

Conclusion

- VPC2 is a very versatile video chain with a specific analog Rad tolerant ASIC
- SpaceWire RMAP gives secure and adaptable data exchange for video processing chain
- SpaceWire RMAP is easy to implement in Hardware with no need of using embedded processor.