SpaceWire
Remote Terminal Controller

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SpaceWire RTC contract

- ESA study
- Prime Contractor: Saab Ericsson Space
- Subcontractor: Gaisler Research
- Foundry: ATMEL, ATC18RT 0,18µ process, multi-project wafer run

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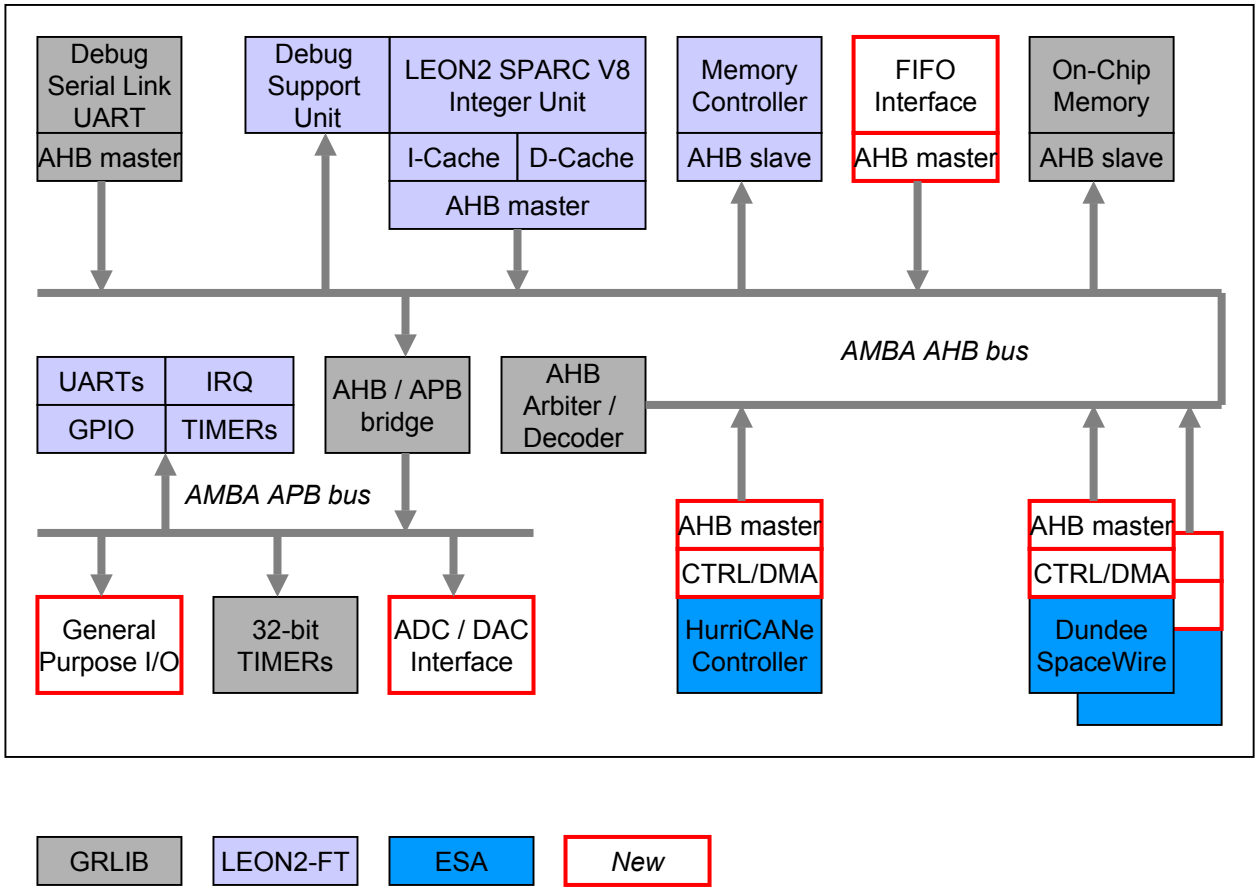
SpaceWire RTC overview



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Processor and Memory

- LEON-2 FT VHDL model
- Cache sizing:
  - 4 kbyte instruction, 4 kbyte data
- On-chip memory sizing:
  - 64 kbyte EDAC protected
- External memory sizing:
  - 4 Mbyte PROM (8-bit wide, EDAC)
  - 8 Mbyte SRAM (8, 16 or 32 bit, EDAC)
  - 2 Mbyte IO

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FIFO Interface

- Interface: 9-bit / 18-bit data,

  read & write strobes,
  full, half-full, empty,
  programmable wait states

- Function: stand-alone FIFO interface with active control of external FIFO devices

- On-chip: AMBA AHB master with DMA

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SpaceWire Functions

- SPW CODEC IP used
- RMAP support (Read & Write block)
- Rx and Tx Channels, separate from RMAP
- Time Code, Receive and transmit
- 200 Mbit/s capability, @ 100MHz SPWClock, i.e. DDR only
- I/F to AMBA bus
- Local CPU Support for:
  - Packet handling (multiple packet, buffer limits, alignment, debug)
  - Sending RMAP commands (separating header and data, CRC generation, ..)
  - Transparent reception of Transfer protocols not supported in HW.

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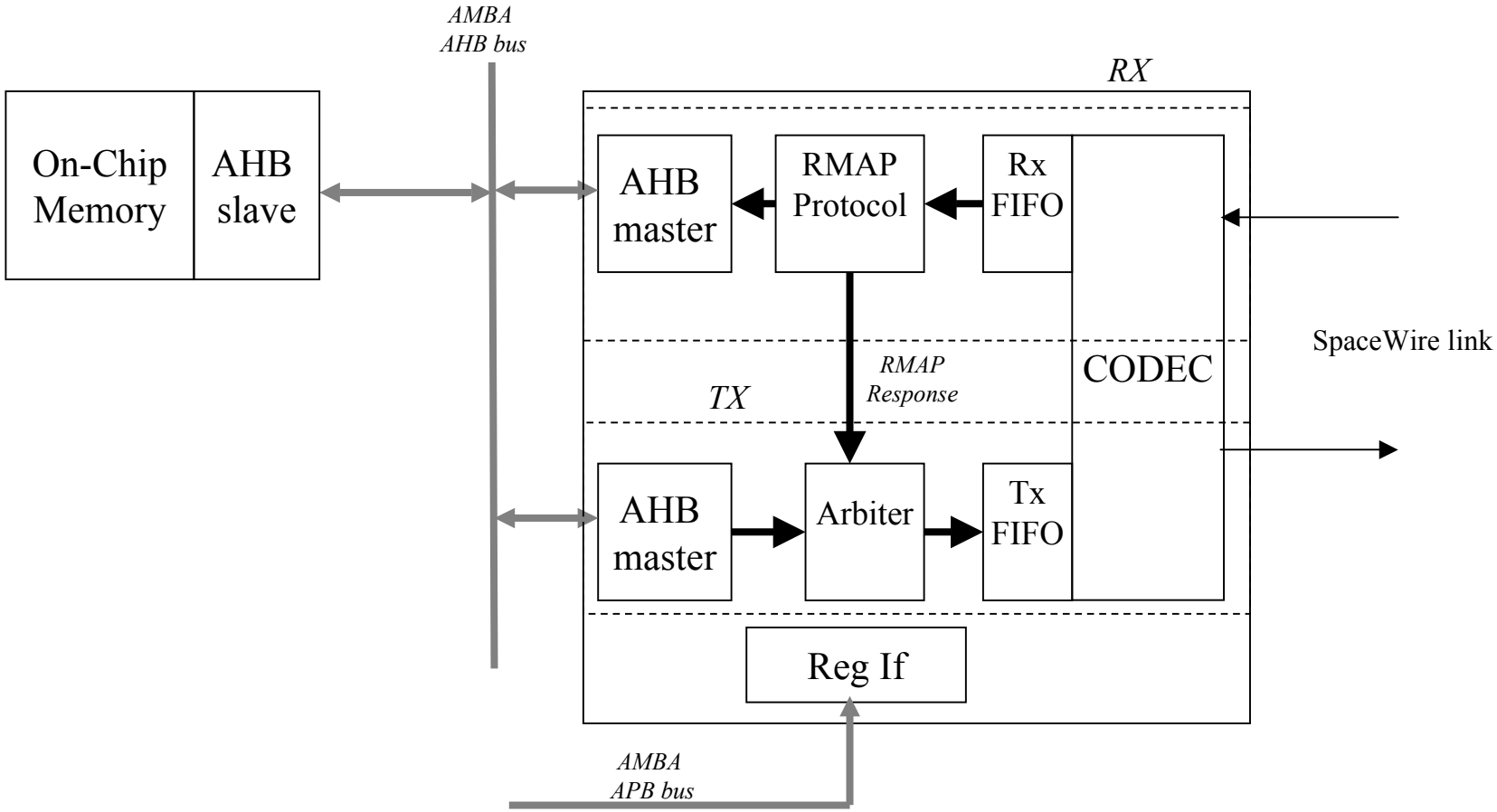
SpaceWire block diagram



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Rx Functions

- Two Rx Channels, Rx(0) reserved for RMAP, (each separated by unique DLA)
- RMAP: protocol identification, Command interpreter and Error handling,
- MemoryBuffer structure, individual buffers for each Rx Channel. RMAP uses its buffer only for Responses and unsupported Commands.
- CRC8 Checker in HW, for RMAP packets only
- AHB Master (Write only)
- High speed, over clock region transfers
  >200MBit/s Data transfer rate using 64bit blocks
  @ 30MHz BusClk and 100MHz TxClk.

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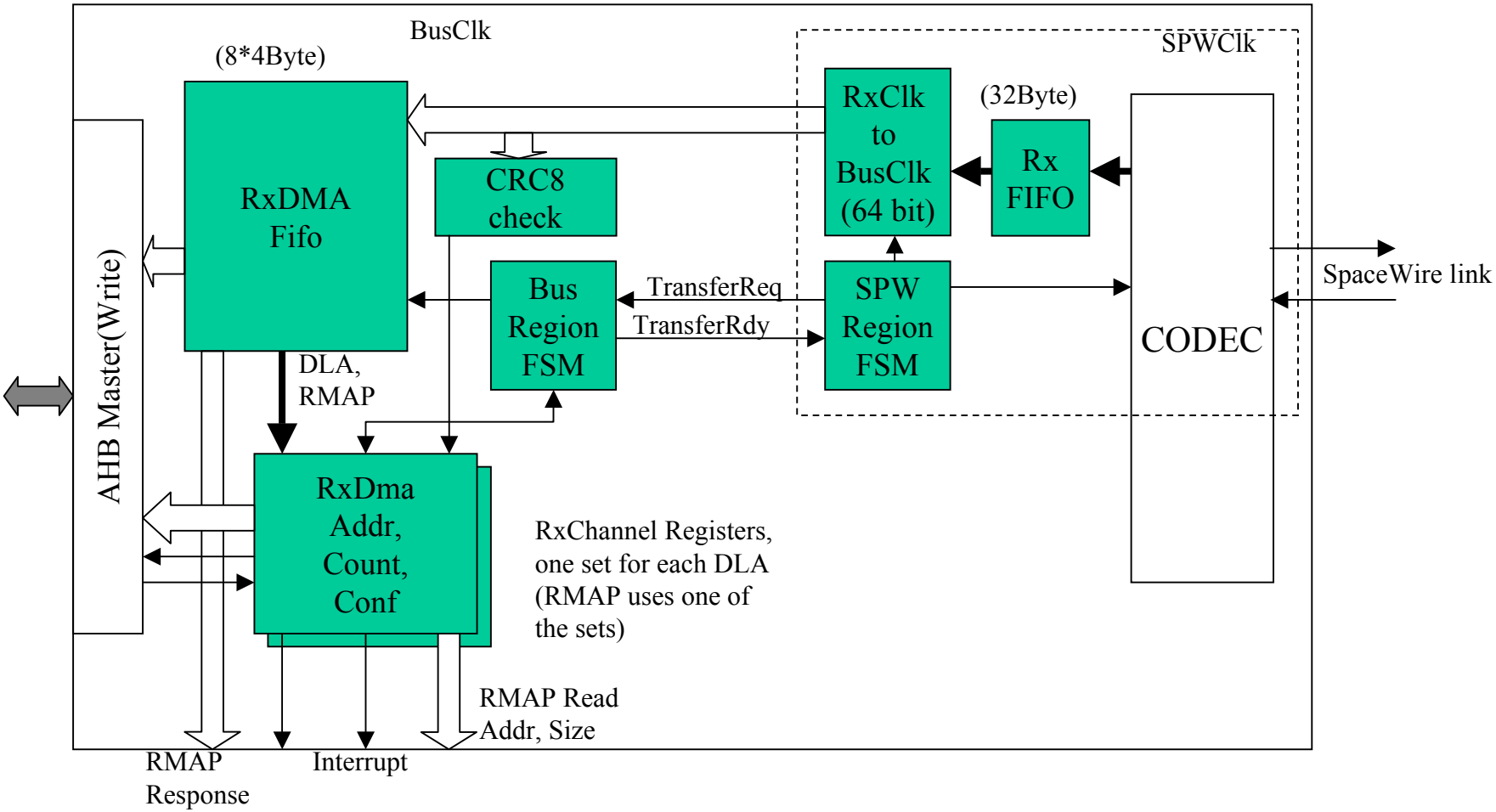
Rx Functions (block diagram)



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Tx Functions

- Two Tx Channels, Tx(0) reserved for RMAP)
- Arbiter, RMAP TxChannel has highest priority
- Send list memory structure, up to 255 entries for each
  Tx Channel sendlist structure allows separate handling of header and raw data.
- CRC8 Generation in HW, for RMAP packets only
- AHB Master (Read only)
- High speed, over clock region transfers
  >200MBit Data transfer rate using 64bit blocks
  @ 30MHz BusClk and 100MHz TxClk

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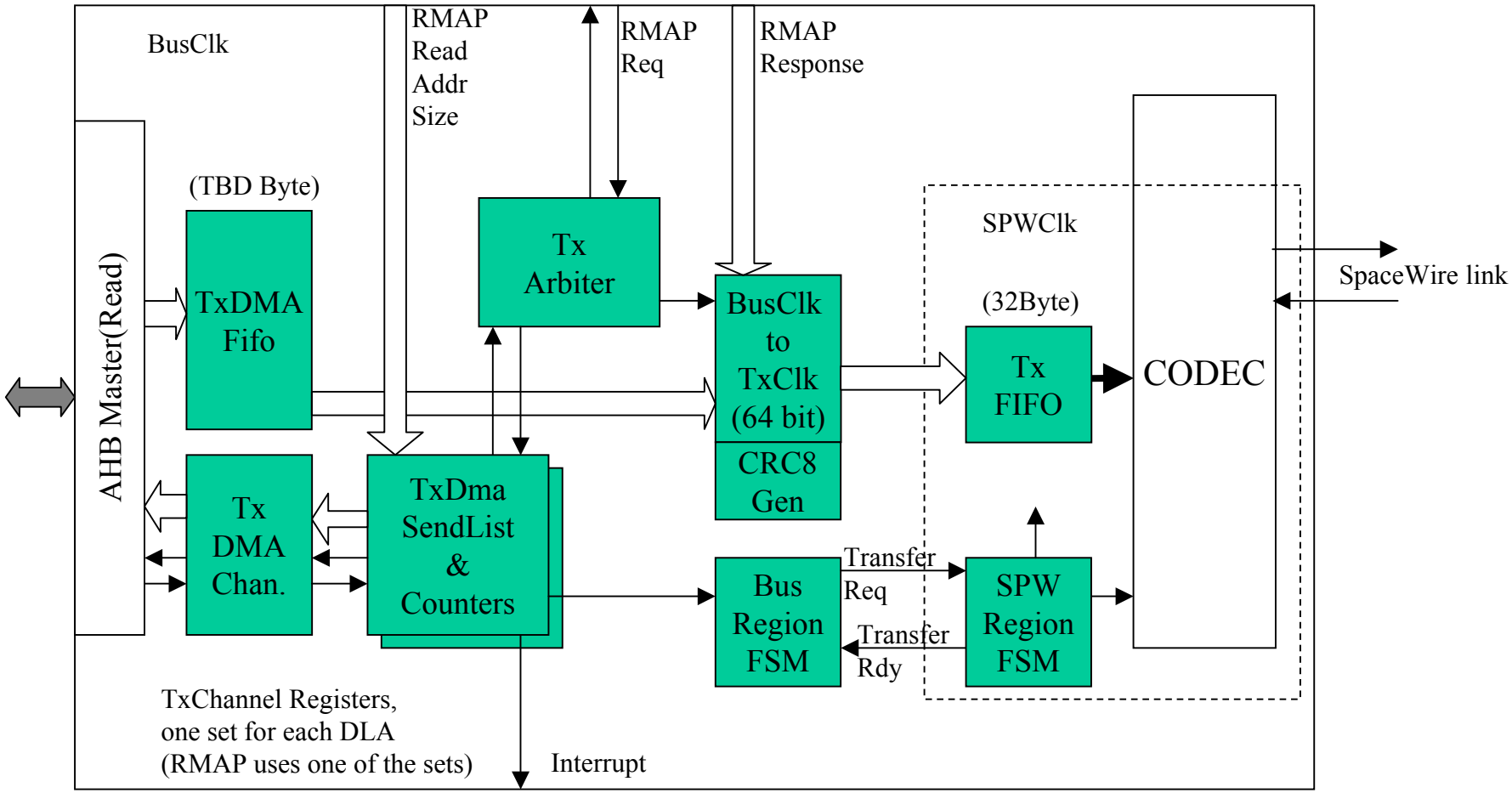
Tx Functions (block diagram)



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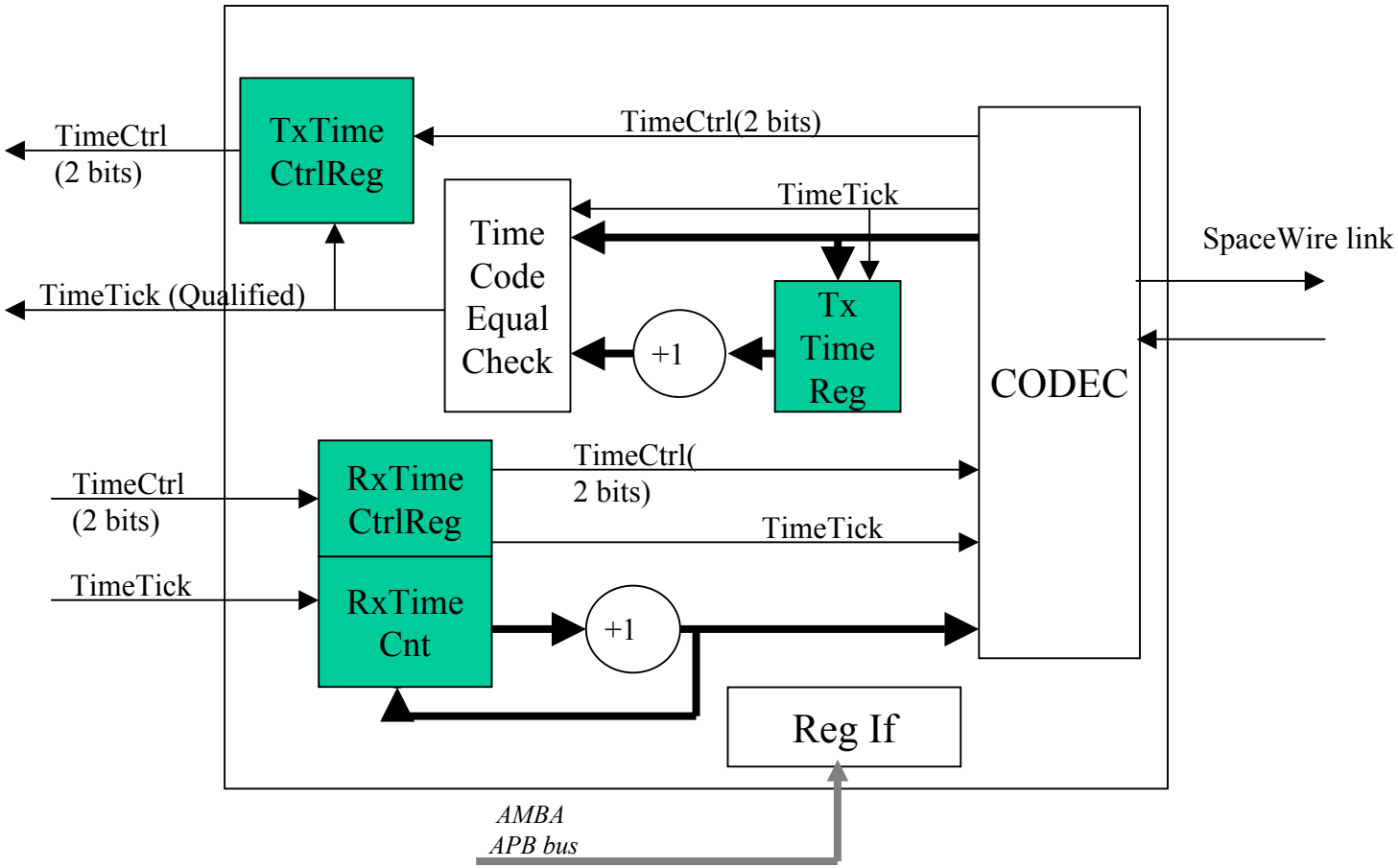
TimeCode



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