NASA SpaceWire Status

SpaceWire Working Group Meeting
July 19-21, 2005

Presented by
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Agenda

- Projects using SpaceWire
- Protocol Development
- Physical Layer Development
- Implementations

Projects using SpaceWire

- Swift
- JWST
- LRO
- GOES-R
- Base-lined for various formulation missions

Protocol Development

- **Three projects are developing SpaceWire upper layer protocols**
  - JWST
  - LRO
  - GOES-R
- **JWST protocol development was complete before Protocol ID field was introduced to the standard**
  - Commanding is done by using CCDS packets tunneled through SpaceWire
  - Science Data packet is optimized for implementation specific requirements
- **Lunar Reconnaissance Orbiter (LRO) investigated using the SnP Rmap protocol but chose to use CCSDS tunneled through SpaceWire**
- **GOES-R is using CCDS tunneled through SpaceWire with project developed Reliable Delivery protocol**
  - Reliable Delivery protocol may be used to replace MIL-STD-1553 for other missions
- **CCDS is the native format for the software bus for many NASA GSFC missions and therefore it is a natural packet format to tunnel through SpaceWire**

Physical Layer Development

- Clock recovery is challenging to prove by analysis using FPGA designs for DS encoded signals
- This forces designs using DS encoding that require moderate to high data rates to use ASIC implementations
- JWST is developing a Physical (PHY) Layer ASIC chip to solve the DS clock recovery challenge for FPGA based designs
  - DS clock recovery
  - LVDS Receiver
  - LVDS Transmitter
- PHY layer ASIC may possibly be made commercially available by vendor

Implementations

- **Chip Solutions**
  - BAE SpaceWire ASIC will have engineering units delivered by November 2005 for GOES-R project
    - Developed to provide possible solution for GOES-R users
    - Details presented at last working group
      - 4 port router
      - Micro-controller
      - 2 PCI buses
  - Multiple protocol FPGA solutions for LRO and JWST are being base-lined using the PHY Layer ASIC
    - RTAX2000S implementing a 4 port router
      - JWST
      - LRO
    - RT54SX72S implementing a point-to-point link (CODEC)
      - JWST only
- **Board Solutions**
  - Two board level products are being developed by BAE SYSTEMS based upon the BAE ASIC for the LRO project
    - Single board Computer (SBC)
    - Solid State Recorder (SSR)
  - LRO will develop 3 different boards using the RTAX2000S and PHY Layer ASIC solution
  - JWST will develop 3 different boards using the RTAX2000S and PHY Layer ASIC solution
  - JWST will develop 4 different boards using the RT54SX72S and PHY Layer ASIC solution