SpaceWire activities in Japan

M. Nomachi Osaka University
S. Ishii MHI
H. Hihara NT space
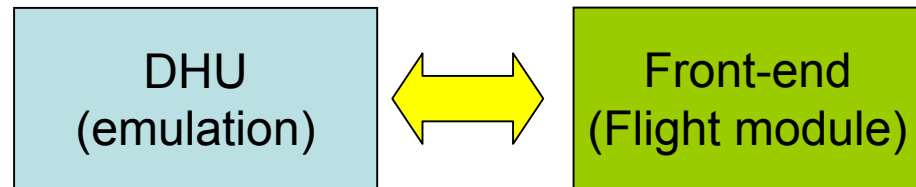and
JAXA

SpaceWire

- **Establishment of "Modular Structure"**
  - Good for development
  - Good for debugging
  - Good to maintain

SpaceWire

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    - Good for development
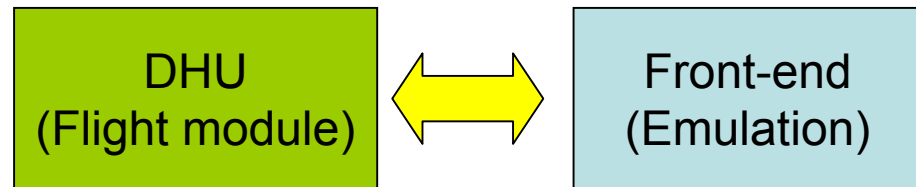   - Good for debugging
    - Good to maintain

| DHU (emulation) | ⟷ | Front-end (Flight module) |

Development of Front-end modules

SpaceWire

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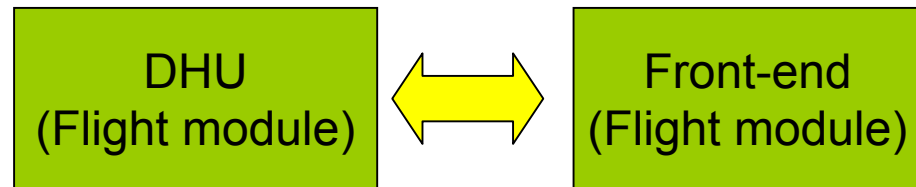   - Good to maintain

DHU (Flight module)	⟷	Front-end (Emulation)

Development of DHU modules

SpaceWire

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| DHU (Flight module) | ⟷ | Front-end (Flight module) |

Space Cube

Space Cube is a tool designed for the development.

VR5500CPU
(MIPS)

PCI

PCI Bridge(PCI9054)

ALTERA
Cyclone
EP1C6F256C6

LVDS   LVDS   LVDS

SpaceWire (3 ports) >100Mbps
t-kernel / LINUX
        (the same kernel is preferable)
IP on the FPGA
        MHI
        NT space

The reference hardware for MMO

- •Purpose
  - – The first space application of SpaceWire will be MMO in Japan. The framework to establish interface compatibility between science equipments and bus system of MMO is the main issue.

- • SpaceCube based reference design framework
  - – SpaceWire interface device IP (Intellectual Property = FPGA macro) and BSP (board support package = software driver) are developed for SpaceCube.
  - – Each PI will develop their own SpaceWire interface with reference to SpaceCube.
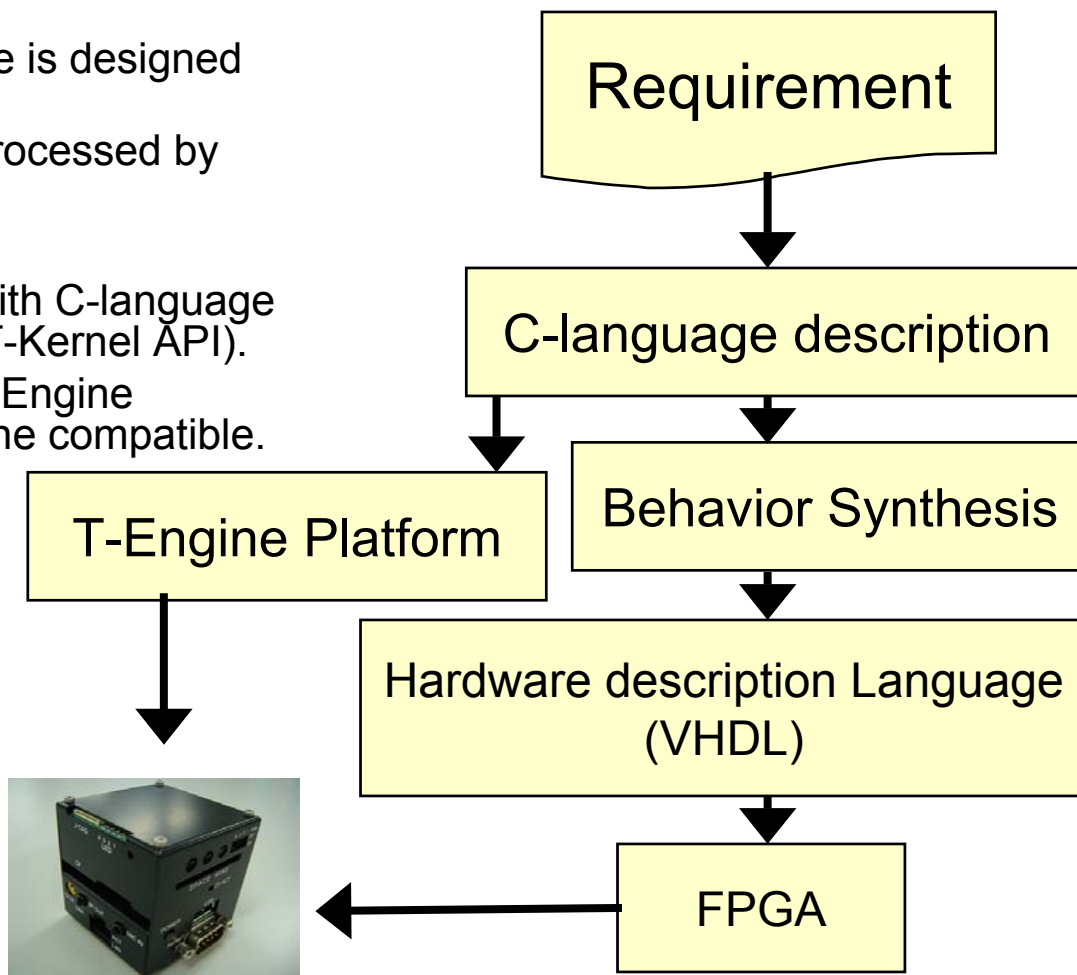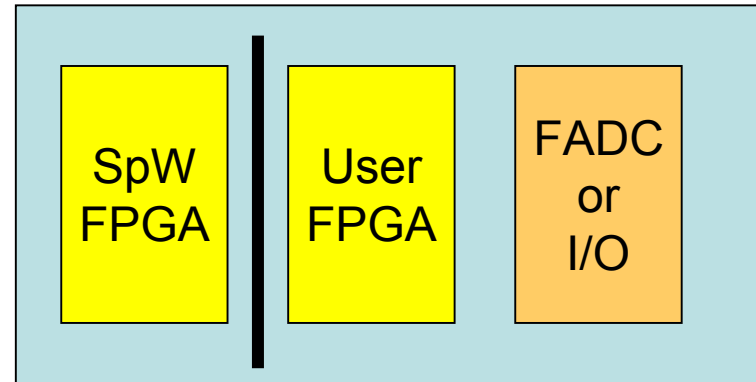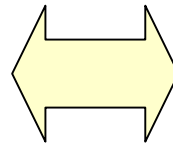
IP and BSP development

- IP development
  - FPGA IP on SpaceCube is designed with C-language.
  - Behavior synthesis is processed by Cyber of NEC.
- BSP development
  - BSP is also designed with C-language on T-Engine platform (T-Kernel API).
  - SpaceCube is one of T-Engine appliances, and T-Engine compatible.

```
Requirement
      |
      v
C-language description
   |        |
   v        v
T-Engine Platform    Behavior Synthesis
   |                    |
   v                    v
[SpaceCube]    Hardware description Language
                       (VHDL)
                        |
                        v
                      FPGA
```

Front-end modules

Local BUS

Space Cube works as DHU emulator
The I/O modules will be the reference module of the front-end modules.

Modules
    14 bit 10MHz FADC
    8 bit 500MHz FADC
    Digital I/O module

ECSC 2005 exposition
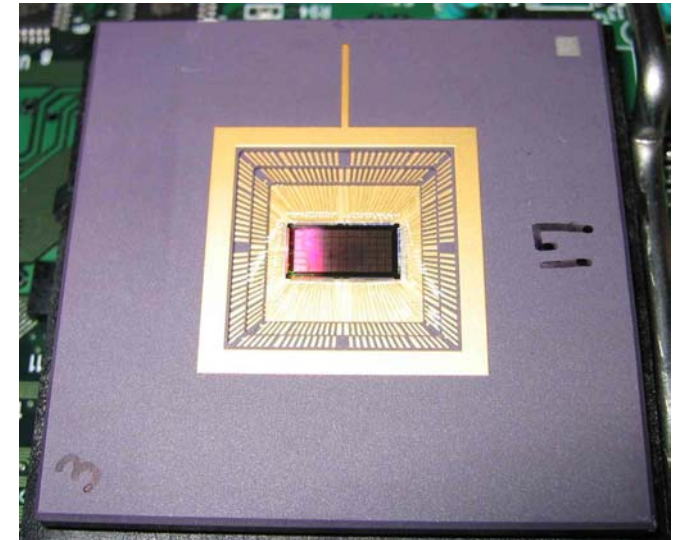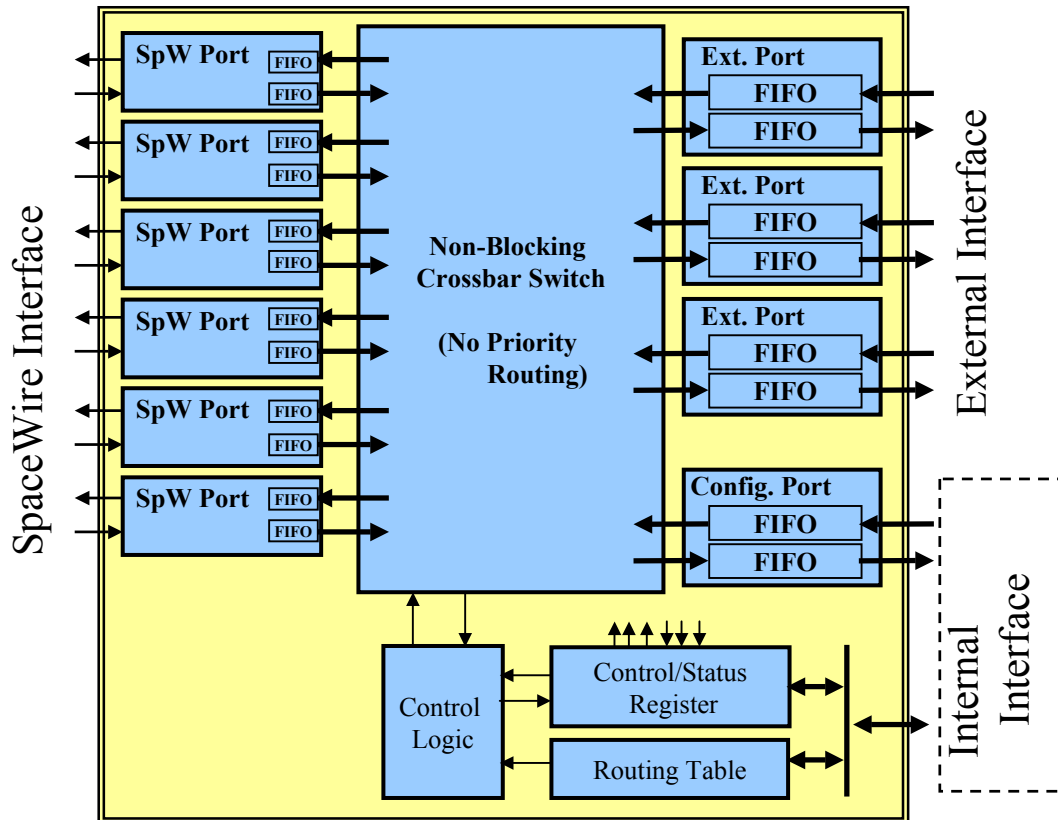

Space Cube

14 bit FADC

Space Cube

NEC/TOSHIBA

SpaceWire-Router ASIC Prototype (1st Step) Development Summary

- ASIC Technology
  - 0.2um SOI-CMOS Process (1.8V supply)
  - Implementation of JAXA/MHI Standard-cell
  - Latch Up Free, SEU: > 45 MeVcm2/mg

SpaceWire-Router ASIC Prototype (1st Step) Development Summary

-SpaceWire Interface
- Six SpaceWire ports
- 2 ~ 100Mbits/s baud-rate

-External Interface
- 9bits wide Three External ports

-Internal Interface
- 9bits wide One Port
- Routing Table, Control/Status registers

- Routing Switch
- Non-blocking Crossbar Switch
- Logical/Region/Path Address
- Group Adaptive

- No Implementations
- Time-code , Priority Routing , RMAP
External LVDS Driver & Receiver

2nd Step

- Time-code,Priority Routing, RMAP
- Up to 200Mbits/s baud-rate

Summary

- Space cube
  - Emulator for the system development
  - Reference hardware
  - Template module/IP is being developed
- SOI ASIC