SpaceWire
Working Group Meeting
NASA
GSFC

February 15 & 16, 2005

SpaceWire Projects

- **NASA Missions**
  - Swift (on-orbit)
  - JWST (Phase B - development)
  - LRO (Phase A – development)
  - GOES-R (Phase A – development)
  - Hubble Robotics Mission (Phase A – development)
- **Several missions in formulation stage proposing SpW**
- **NASA Wallops investigating using SpW for sub-orbital missions**
- **Non-NASA Missions**
  - Lockheed Martin (Sunnyvale) & Honeywell (Clearwater, FL)
    - DOD

Groups Working with SpaceWire

- **NASA**
  - GSFC
  - JPL
- **Industry**
  - BAE SYSTEMS
  - Lockheed Martin
  - Honeywell, Inc.
  - NGST
  - SEAKR
  - Aeroflex
  - Goodrich
  - ATK Mission Research (own design)

Products

- **NASA**
  - Link & Switch (RTL VHDL)
    - Primary/Redundancy logic
    - Multiple time-code
    - Zero time-code jitter
    - No Group Adaptive routing
  - Verification environment with directed & random tests
  - Available via GSFC Commercialization & Technology transfer office
  - Products
    - Commercial cPCI PC board with application software
      - 2 port switch (Xilinx Virtex II Pro)
    - Link design targeted to Actel RT54SX72 (TMR part)
      - Fuse File with Data sheet (max speed 83Mbps)
    - Breadboard JWST Bus Interface Card (BIC)
      - 12 port router with 8 external interfaces
        - cPCI
- **Industry**
  - BAE SYSTEMS ASIC (uses NASA core)
  - ATK Mission Research (Funded by Air Force)
    - 8 port switch GSE board
      - 625 Mbps

Testing

- **Physical Layer**
  - JWST in conjunction with Gore has been testing SpaceWire physical layer
  - JWST will baseline different connector than in SpaceWire Standard
    - 4 connector Twin-axial
      - Used for segmenting cable
      - Replace 9 pin MDM at end of link
  - JWST will baseline different cable
    - AWG # 26 instead of # 28
- **Lab**
  - Compatibility testing performed against
    - 4 Links
    - Star-Dundee
  - Continuous Random Testing in simulation environment

Design and Characterization of a State-of-The-Art High Speed Payload Interface Device for Use on Satellites Using Rad Hard Technology Based on Spacewire

Space Communications Project
GRC Contract NAS3-03086

Access Networks

February 15, 2004

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Goals:

Advance the state of the art for onboard networking technology for distributed communications systems

Objectives:

The objective of this program is to develop low power, miniaturized, high data rate on-board networking technology for distributed communications based on standards that would be beneficial to high data rate programs such as NPOESS,GOES-R, SIM, JWST and others. The resulting technology development would support onboard networks for data rates up to 300 Mbps.

Work Scope Summary:

- Integrate GSFC Spacewire Link and Router design into BAE SYSTEMS R25 ASIC Library
- Augment GSFC Spacewire Design with BAE SYSTEMS System-On-Chip IP Cores to facilitate emerging Spacewire Transport Layer
- Fabricate and Test the ASIC

Accomplishments:

- Implemented GSFC Spacewire Design into R25 ASIC Library
- Developed new Core (RIF Core) to interface GSFC Design to BAE SYSTEMS SOC complex
- Completed logic simulations
- Completed ASIC Physical Design and timing closure
- Ready for fabrication

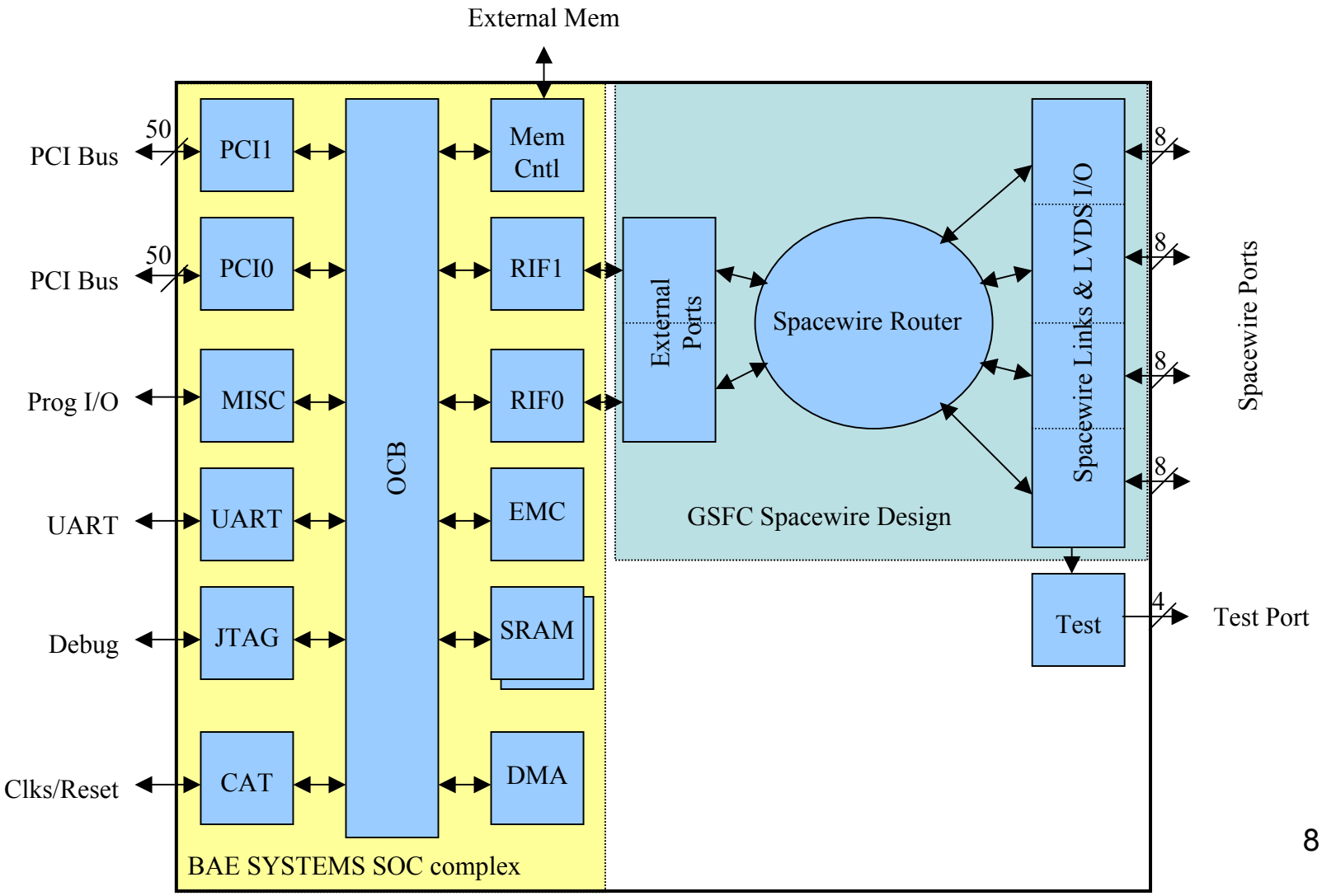
NASA Enterprise Impact:

Space Science, Earth Science: GOES-R (2012), SIM, NPOESS, Lunar Discovery, Mars Communications (Mars '09)

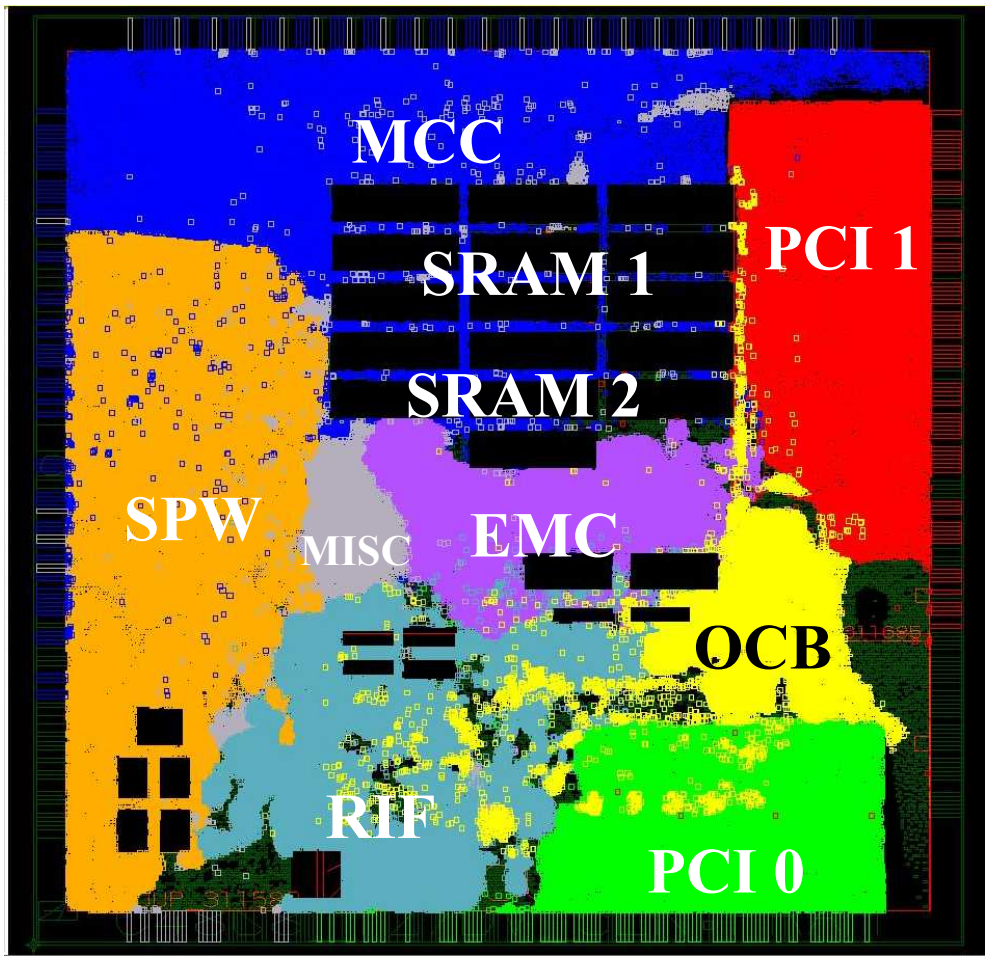
Exploration System: Lunar Mission, Robotic/Human Mission, and CEV. Provide data transfer rate increase at least 10 times over current state-of-the-art technology - result is increased transfer rate for future spacecraft command and control interfaces and bus interface.

Participants: GRC, BAE SYSTEMS, GSFC

Spacewire ASIC Block Diagram



Spacewire ASIC Key Features



- **4 Spacewire Ports**
  - ECSS-50-12A Compliant
  - Integrated LVDS I/O
- **2 User External I/F Ports (PCI)**
  - Up to 33 MHz operation
  - 32 bit Address / Data Bus
- **Embedded Micro-Controller**
  - Support Spacewire Transport Layer
- **Memory Interface**
  - EEPROM for initialization
  - SDRAM or SRAM bulk storage
- **Test Interfaces**
  - 16550 UART
  - JTAG
  - Spacewire Data Access
- **Miscellaneous**
  - Interrupts
  - Programmable I/O
- **Packaging**
  - 32mm CGA
- **Low Power**
  - 3.3V I/O & 2.5V Core

Future Work

- Higher speed Physical Layer
- Protocol development
  - Reliable transport
  - File transfer