Spacewire related activities in JAXA & Japan: Summary

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M. Ozaki, T. Takahashi (ISAS/JAXA)
M. Nomachi (Osaka Univ.)
NeXT mission WG

**Backbone: Data Handling Group for Scientific Satellites**

Data Handling Group
covers all key scientists & engineers
for laboratories, balloons,
and multi-scale scientific satellites

- T. Hashimoto (ISAS/JAXA)
- H. Hayakawa (ISAS/JAXA)
- H. Hihara (NTSpace)
- S. Ishii (MHI)
- Y. Kasaba (ISAS/JAXA)
- H. Kataza (ISAS/JAXA)
- M. Kokubun (U. Tokyo)
- Y. Kuroda (MHI)
- K. Matsuzaki (ISAS/JAXA)
- E. Miyata (Osaka U.)
- T. Nakazawa (ISAS/JAXA)
- Nishiyama (ISAS/JAXA)
- M. Nomachi (Osaka U.)
- M. Ozaki (ISAS/JAXA)

- Y. Saito (ISAS/JAXA)
- S. Sakai (ISAS/JAXA)
- K. Sakamura (U. Tokyo)
- T. Takahashi (ISAS/JAXA)
- T. Takashima (ISAS/JAXA)
- Y. Terada (ISAS/JAXA)
- Y. Tsuda (ISAS/JAXA)
- H. Yamakawa (ISAS/JAXA)
- T. Yamada (ISAS/JAXA)

with Industries
(NTS, MHI, …)
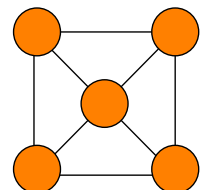
# Plans for "New Frame Work"

Establishment of "Modular Structure"

Standard architecture for   Laboratories (GSE)
Balloons / Sounding rockets
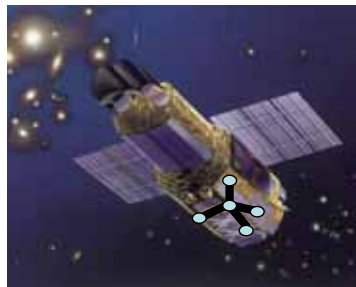Piggy-bag satellites
Large-scale satellites
Formation flights

…based on "Standard Interface" between multiple onboard computers
"Spacewire" + "TRON" (popular real-time OS)

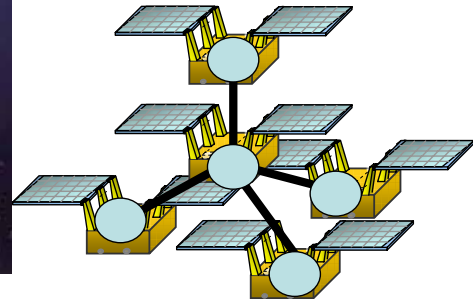**Step by Step approach toward the next missions**

Define
Function
Link/Connection
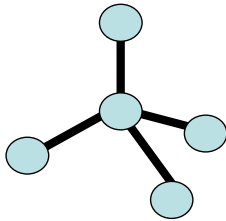
From Big Satellite

To distributed satellites

Development Status: Summary

2003   Chip: **SpW Protocol FPGA** (Osaka U. & MHI)
Application: **Balloon Experiment** (JAXA, Osaka U., Yamagata U.)

2004   **Multi I/F Extension: for T-Engine Platform** (NTS and others)
SpaceCube: Real "PC" (JAXA, Osaka U., Shimafuji Co.)
Application: Readout system for Compton Telescope

2005   **Start of Space Application**
[Technology]
- Establishment of common "Chip" & "Middleware"

[BepiColombo/MMO]
- Design fix of Electronics, including SpW I/F
- Development of "EGSE for Sensor", including SpW I/F
(common development with NeXT)

Osaka University

2003

Already introduced in Last meeting

Protocol Chip purely developed from the "written" specification

Nomachi (Osaka U.) & Ishii (MHI)
[Nomachi et al. IEEE 2004]

Passed
connectivity test @ Dundee U.
(the day before yesterday, Nov.9)
And checked with 4Links (Nov. 10)

System Designing
for Next Generation

2004

Already introduced in Last meeting

Space Cube for "Real" System: "Now available"

It can be supplied to anywhere.
[Contact: takahasi@astro.isas.jaxa.jp]

Space Cube   Enhanced version of "T-Cube" (T-Engine Project)

- Real Computer
  - Linux
  - TRON (Real Time Kernel)
- CPU: 200-300 MHz   (MIPS arch.)
- Memory: 64MB SDRAM
- I/F: PCI / USB / Ethernet / Serial etc.
  + 3-port SpW link

CPU	I/O	SpW

It will be used as EGSE.
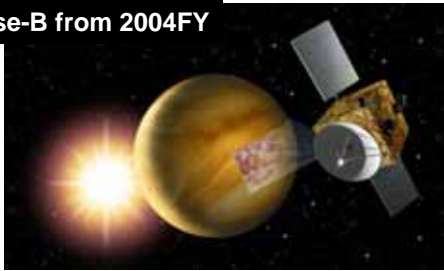
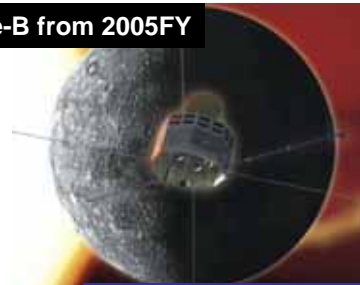| SpW	Sensor board
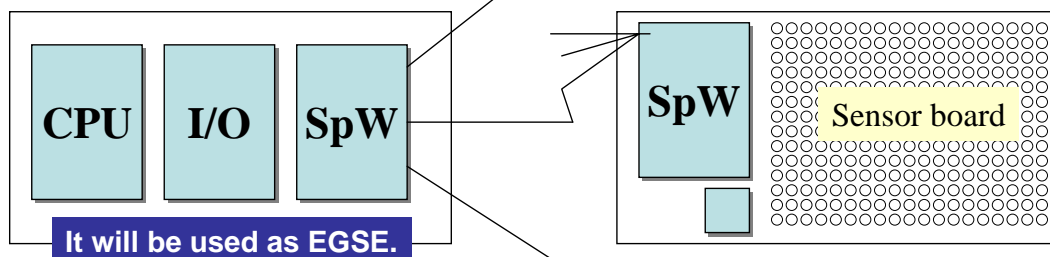
Scientific Missions in JAXA

• Venus Climate Orbiter (2009)

Phase-B from 2004FY
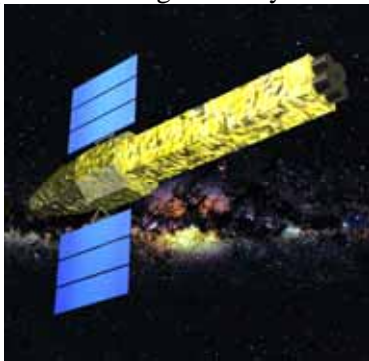
• BepiColombo / MMO (2012)

Phase-B from 2005FY

First SpW-applied mission

• NeXT (X-ray)

(approved as "High Priority Mission")

• Solar Sail (Engineering)

(approved as "High Priority Mission")
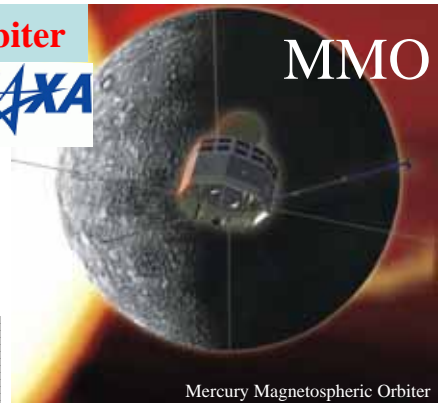

BepiColombo: ESA-JAXA joint mission
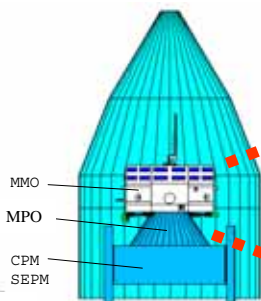
Mercury Magnetospheric Orbiter

MMO

Mercury Magnetospheric Orbiter

C. Noshi/RASC, Kyoto Univ.
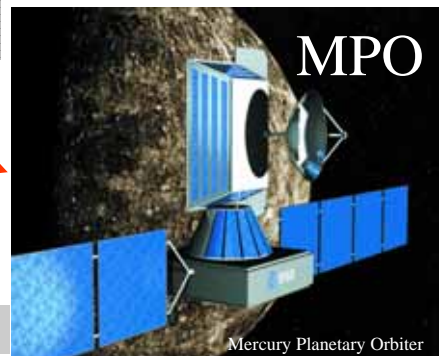
Soyuz Fregat 2B:
MPO+MMO

MMO
MPO
CPM
SEPM

Single Launch

At Cruising phase,
TLM/CMD to the MMO
is through MPO.
Separation is after MOI.

MPO

Mercury Planetary Orbiter

Mercury Planetary Orbiter

·eesa

Launch: mid 2012
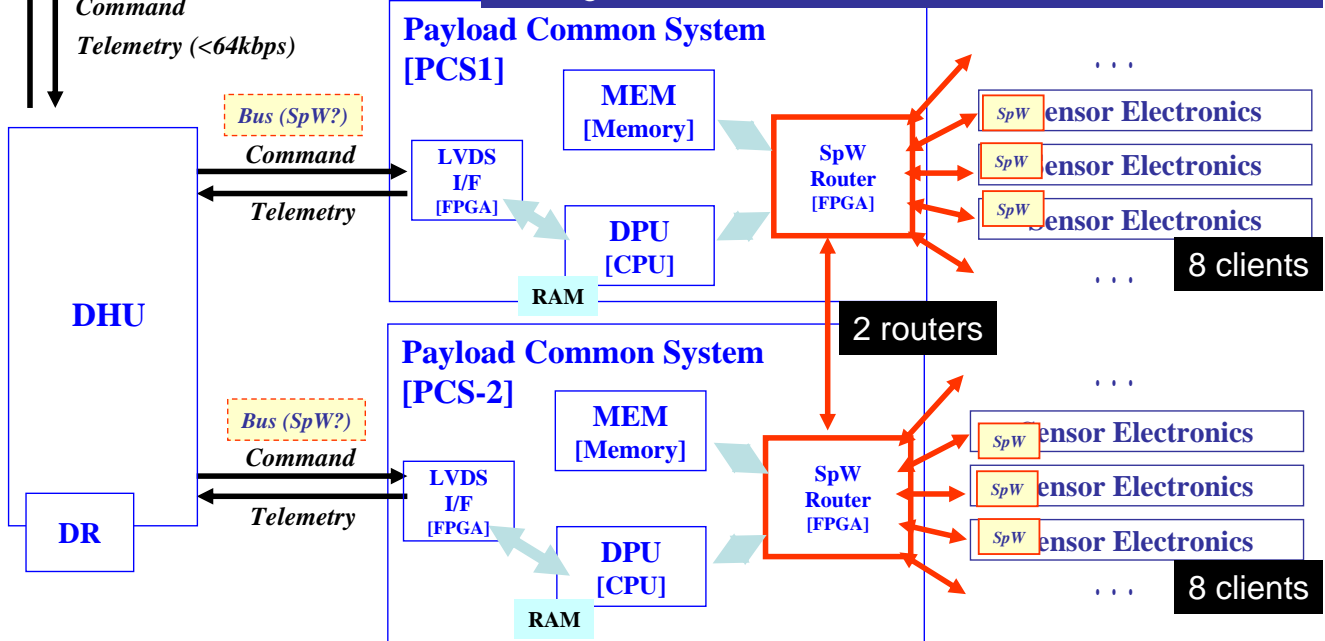
SpW in MMO: for Payload system "PCS with SpW router" x 2

- Small mass, Low power
- Common & Easy I/F to all PI teams in Japan / Europe.
- Design FIX: June 2006   - EGSE dev.: from 2005

(or MPO[ESA])

Command
Telemetry (<64kbps)

DHU

DR

Bus (SpW?)
Command
Telemetry

Payload Common System [PCS1]

MEM [Memory]

LVDS I/F [FPGA]

DPU [CPU]

RAM

SpW Router [FPGA]

SpW ensor Electronics
SpW ensor Electronics
SpW ensor Electronics

8 clients

2 routers

Bus (SpW?)
Command
Telemetry

Payload Common System [PCS-2]

MEM [Memory]

LVDS I/F [FPGA]

DPU [CPU]

RAM

SpW Router [FPGA]

SpW ensor Electronics
SpW ensor Electronics
SpW ensor Electronics

8 clients

General Request for I/F functions (TBR)

Detailes are summarized in Ozaki-san's presentation.

[PCS   each Sensor]
- Non-real   to each: CMD
- Semi-real to each: "Interruption" or 'High-priority CMD"   [option]
- Real   to all: Spin pulse (~0.25Hz) / Phase clock (2kHz)   [~0.1msec accuracy]
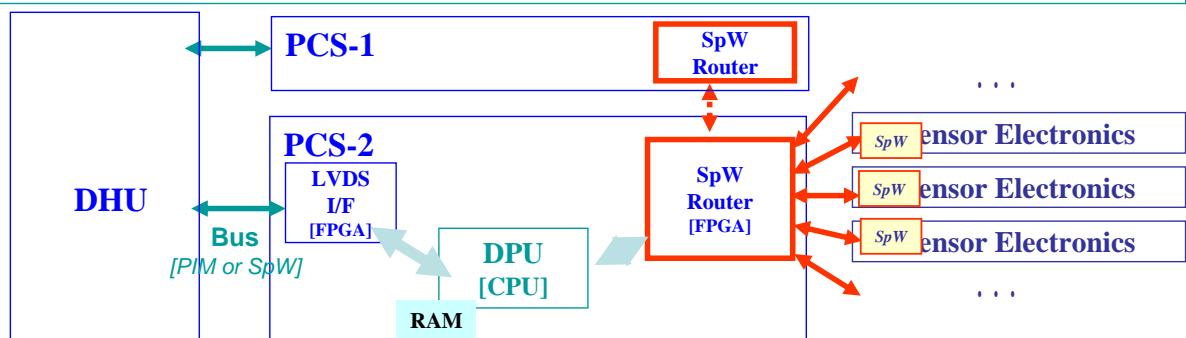   *(by "time code"??)*   + Spacecraft Time [32bit, ~10msec resolution]

[each Sensor   PCS]
- Non-real   to PCS: "Continuous & Fixed" data stream (< 2Mbps)
        - Clock: minimized, for low power consumption
        - Flow control: by PCS   (read: "pull" from PCS by RMAP ??)
- Semi-Real to PCS: Ack. / HK / Status info.   [option]

[Redundancy for Contingency]
        Routing table change in "emergency of Bus I/F or DPU"
        ex) S/C-system   [PCS1]   PCS2   Sensor group

DHU

PCS-1

PCS-2

LVDS I/F [FPGA]

Bus
[PIM or SpW]

DPU [CPU]

RAM

SpW Router

SpW Router [FPGA]

SpW ensor Electronics
SpW ensor Electronics
SpW ensor Electronics

Request from PI teams to I/F (TBR)

Details are summarized
in Ozaki-san's presentation.

Procurement & Compatibility of "ASIC/VHDL" for Client in Japan & Europe

For MMO & MPO, potentially, Japanese instruments   with JAXA ASIC/VHDL
(with ESA ASIC/VHDL)

European instruments   with ESA ASIC/VHDL
(with JAXA ASIC/VHDL)

Others ….   *by "Standard" or "Specific Chip/VHDL" or "Middleware"*

[Physical]
- Harness   Less-weight version (for low data rate / internal connections)
      [option: conversion to "2-lines", like CAN]

[Network]
- "Real-time" capability – "Time code" or "Priority"
   to All: Spacecraft time   : Bit length (24-32bit)   *[kept by Chip?]*
                  Pulse   : Sun / Clock
   to a Client: Interruption   = 'non-broadcasting' but 'immediately & higher priority'
- Packet: Automatic division of "long packet" to "short" one
                  (for inserting "HK/Status/Ack. Packet" within long data flow)
- Large buffer for "PULL":   inclusion into Chip   (for reduction of I/F circuit area)

Discussion   **BepiColombo:**   **with ESA**   **on Mar. 21? @ ESTEC?**
                          NeXT: **with NASA**   **on Feb. 22 @ GSFC**