Summary presentation of SpW related activities by ESA

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Overall Objectives, Data Systems

- Maximising the mission return … more data per €
- Improving on-board intelligence … more information per €

Translated into :

- ✓ *Defining a stable reference architecture for on-board payload data processing systems (processors, memory, I/O modules)*
- ✓ *Providing robust high speed on-board communication links between modules to transfer commands or data blocks and to support inter-process communication (point to point links)*
- ✓ *Reducing harness mass (on-board networks, routers, time codes, ..)*
- ✓ *Reducing implementation costs (reuse ⇒ Standardization, pre-developed and validated building blocks)*
- ✓ *Providing tools to secure the feasibility for data systems, from architectural design up to implementation validation (Test benches, demonstrators, EGSEs, ToPnet, S/W drivers)*
- ✓ *Maintaining compatibility with other buses and defining on-board services (hierarchical networking concept, CCSDS SOIF, SOIS)*

Data Systems Architectures

- Two complementary architectural paradigms:
  - Highly Integrated Control and Data Systems, for small spacecraft Avionics
  - Distributed data systems, for medium to large satellites embedding demanding payloads in terms of on-board data processing.

- The two approaches share common building blocks and technologies (Processors, ASICs, Bus and network interfaces, microelectronics devices)
- Fault tolerance, Harness minimization, hierarchical networks, standardized interfaces and services (at HW and SW) are systematic objectives underlying all R&D activities in the field of data systems.

Data Systems Architectures

Distributed data systems

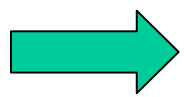
- *Driven by medium size to complex missions*
- *Based on a consistent functional breakdown*
- *Easy to adapt to precise mission requirements*

Distributed Data systems are inherently

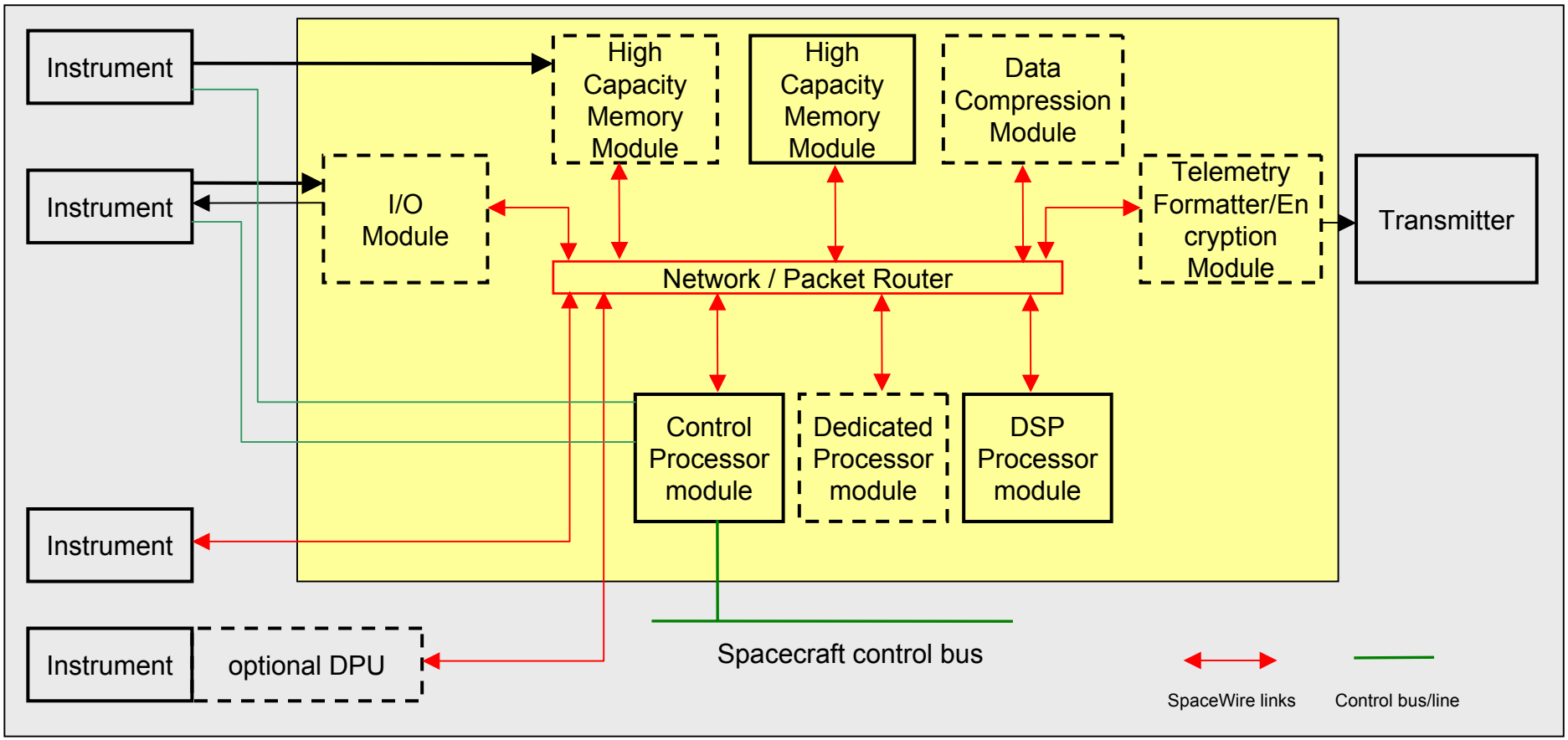
Modular Scalable Evolutionary

can be made Re-configurable

And can be modelled by a reference architecture



Distributed Data Handing and Processing architecture

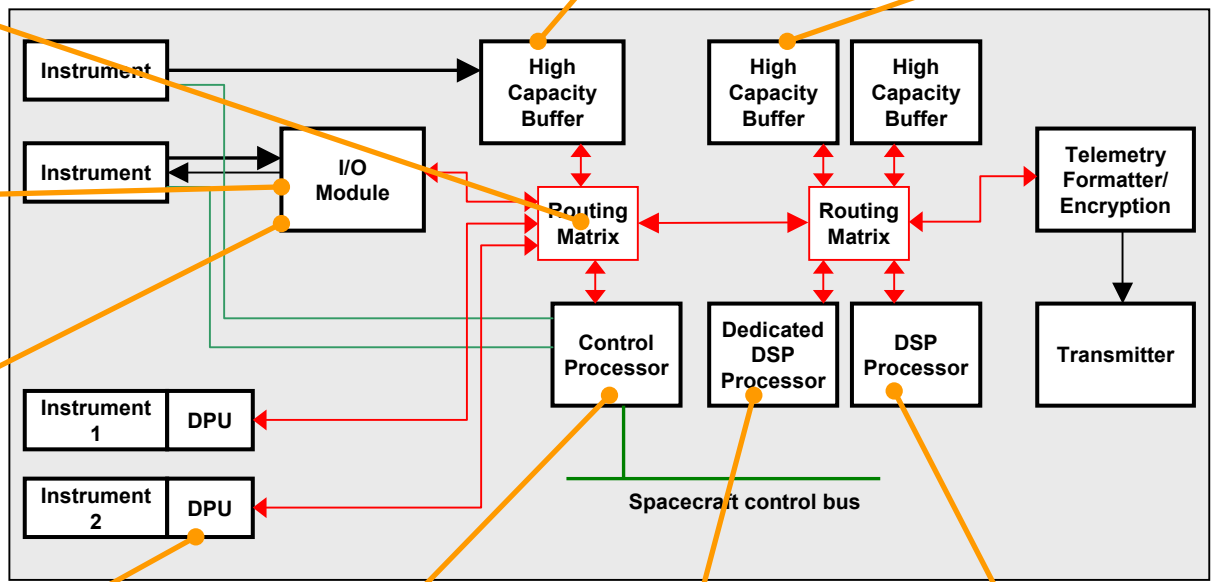


European Status of Technology Modules development (2003)

SpaceWire Router (under Development)

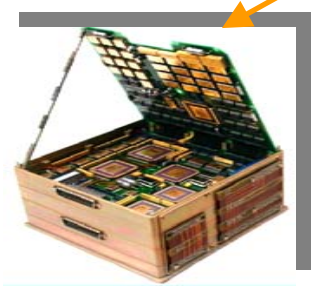
SAR Signal Acquisition Chain (under Development)

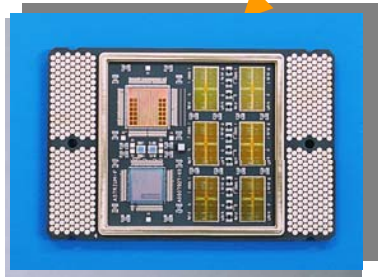
CCD Video Signal Acquisition Chain (under Development)

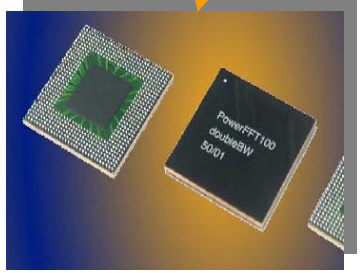


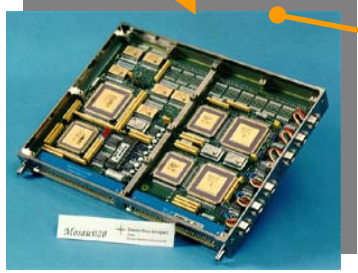
Technology Elements used On:

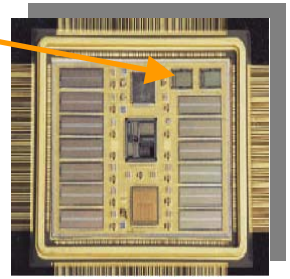
- METOP
- ROSETTA
- MARS-Express
- HERSCHEL-PLANCK
- CRYOSAT
- GOCE, COROT
- ISS EDR
- JWST
- GAIA, Bepi Colombo





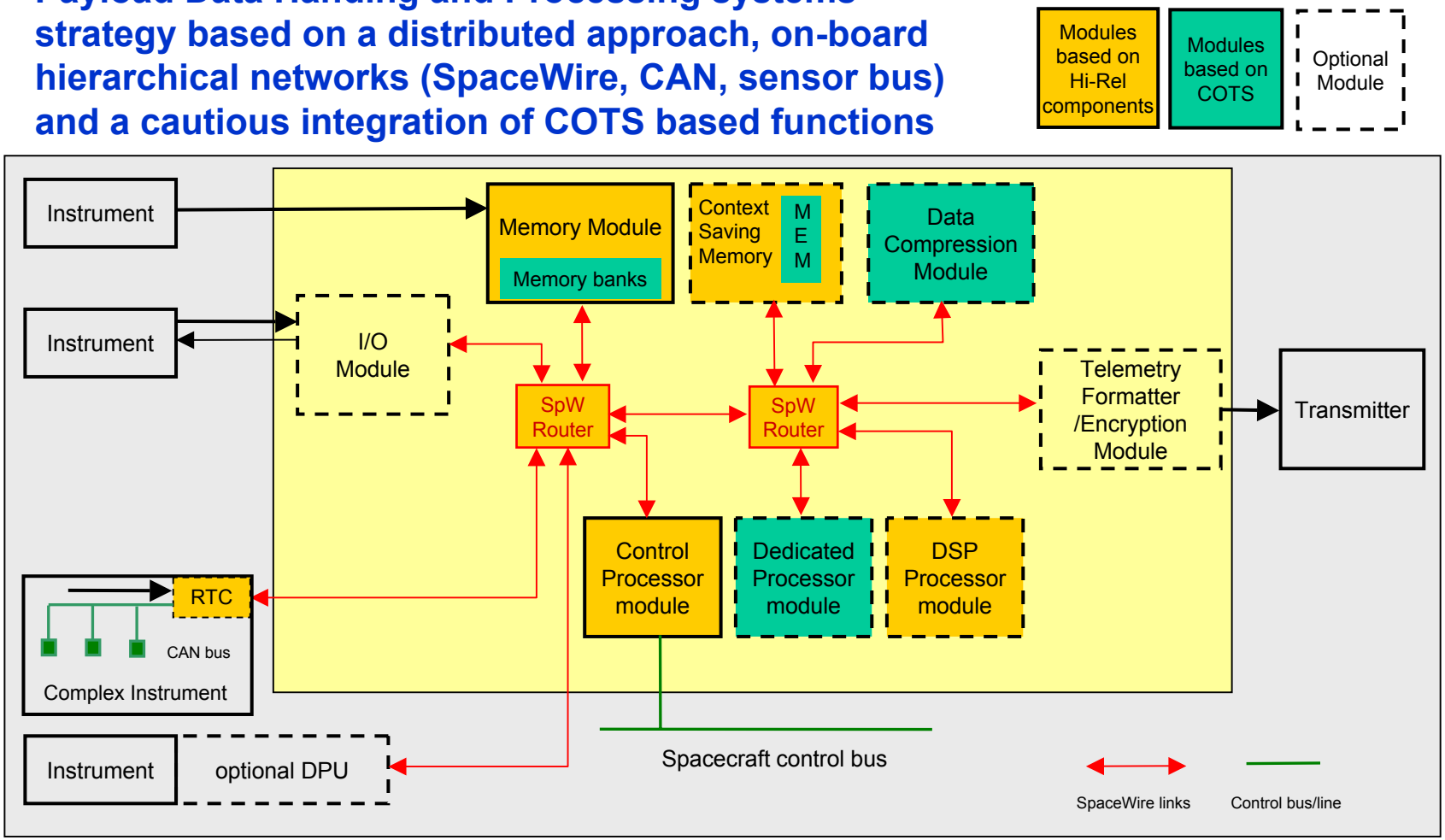






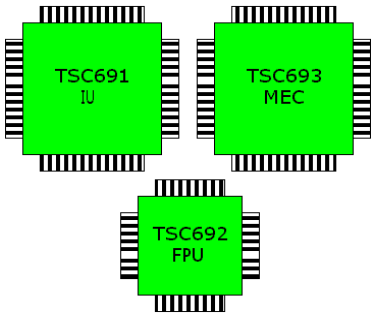
Distributed Payload Data Processing systems

Payload Data Handing and Processing systems strategy based on a distributed approach, on-board hierarchical networks (SpaceWire, CAN, sensor bus) and a cautious integration of COTS based functions



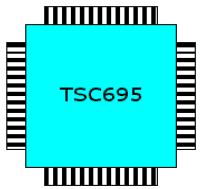
Radiation Tolerant RISC Processors Road Map

ERC32 3-chip set



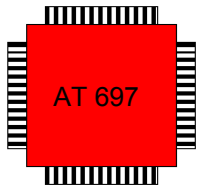
- SPARC V7, 32 bit
- Three chips
- 256, 160, and 256 pins
- 10 MIPS at 14 MHz
- Designed mid 90's by TEMIC
- CMOS RT 0.8 micron
- Partial European design
- RISC
- 50 Krad, ~15 MeV LET
- Used in man space systems: DMS-R, SPLC, ERA, ATV, and also in PROBA
- Phase-out: Last buy June 2002

ERC32 Single Chip



- SPARC V7, 32 bit
- Single chips of 256 pins
- 14 MIPS at 20 MHz
- Designed end 90's by TEMIC
- SCMOS RT Plus 0.5 micron
- Merging of the ERC32 3-chip set
- usage of SEU hardened F/F
- 300 Krad
- 10^{-8} error/dev/day
- Removing of unused functions
- Addition of new functions and bug fixes

LEON2FT



- SPARC V8, 32 bit
- Single Chip, 256 pins
- 100 MIPS at 100 MHz
- Use of Instruction and Data caches
- SDU (Support Debug Unit)
- AMBA bus and PCI
- SEU free by design (TMR)
- LEON core designed by ESA
- Demonstrators on 0.35µ and 0.18µ commercial technologies
- Prototypes built by ATMEL end 2004, Flight Part 2006

Next Generation General Purpose Processor (e.g. LEON3)

- If LEON 3 , same as LEON2F plus:
- Single Chip, CGA package
- SDU (Support Debug Unit; via Ethernet port)
- 0.18µ/0.13µ with standard lib.
- Enhanced FPU (80 MFLOPS)
- Memory Management Unit
- Multiprocessor support
- Prototype: 2006

Specialised processors →

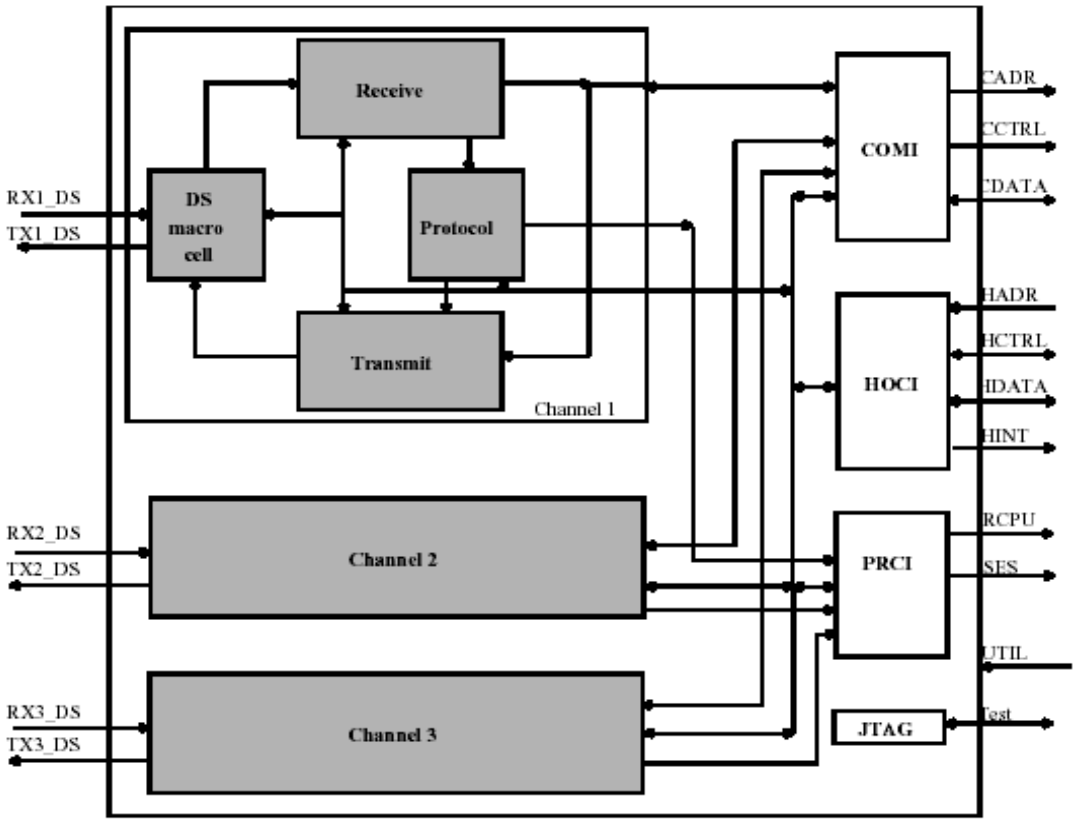
DSP: TSC21020F

20 Mips – 60 MFlops

PowerFFT

1K Complex FFT in 50µs

Available products : SMCS332

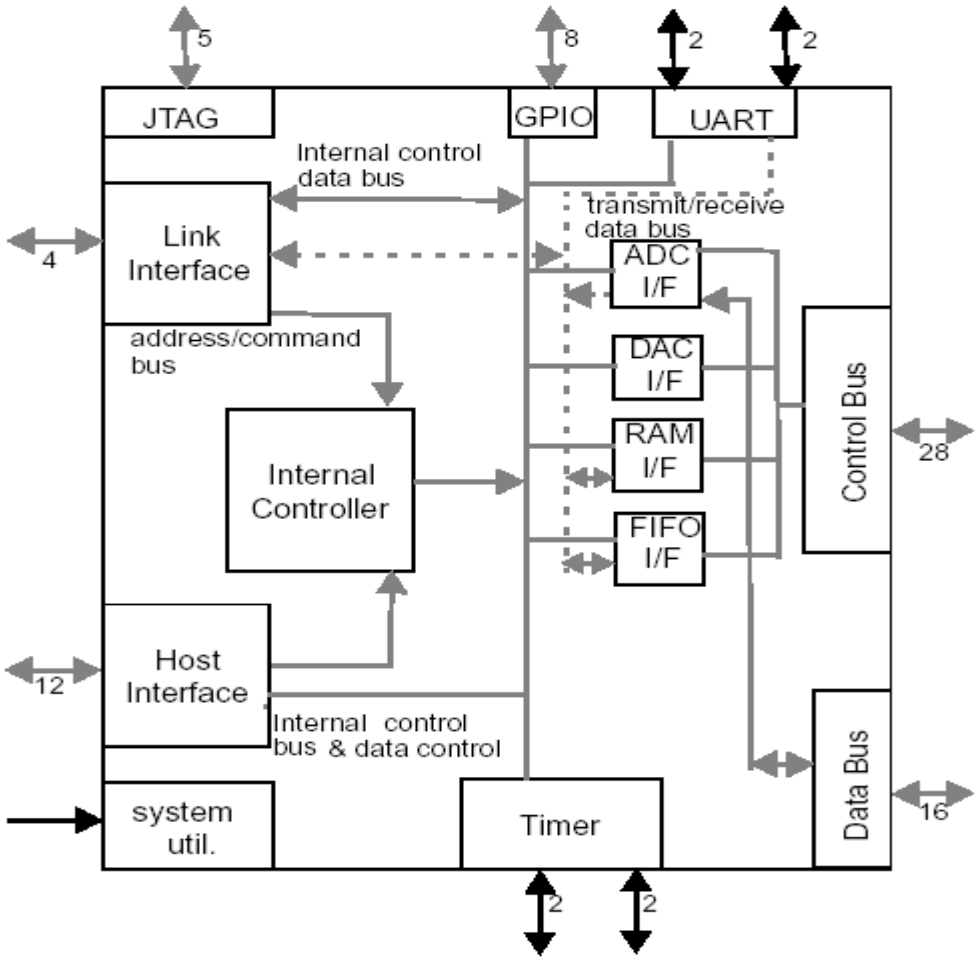


- IEEE1355 compliant
- Manufactured by Atmel
- Ref: TSS901E

Under development: SMCS332 SpW

- **ASIC**
  - Implementation in Atmel MG2RT gate array
  - Max gate count 480 kgates (max technology)
  - 0.5 µm CMOS process
- **Radiation tolerance**
  - Up to 100 kRad
  - SEU free cells to 100 MeV
  - Used for all memory cells
  - Latch-up immunity to 70 Mev
- **Performance**
  - SpaceWire interface baud-rate 200 Mbits/s
- **Power**
  - max 190mA at 5.5V at maximum data rate
  - 5 V and 3.3 V supply voltage
- **Package**
  - 196 pin ceramic Quad Flat Pack 25 mil pin spacing
- **Schedule**
  - Availability of prototypes: Q2 2005
  - Availability of flight parts: Q4 2005

Available products : SMCS116

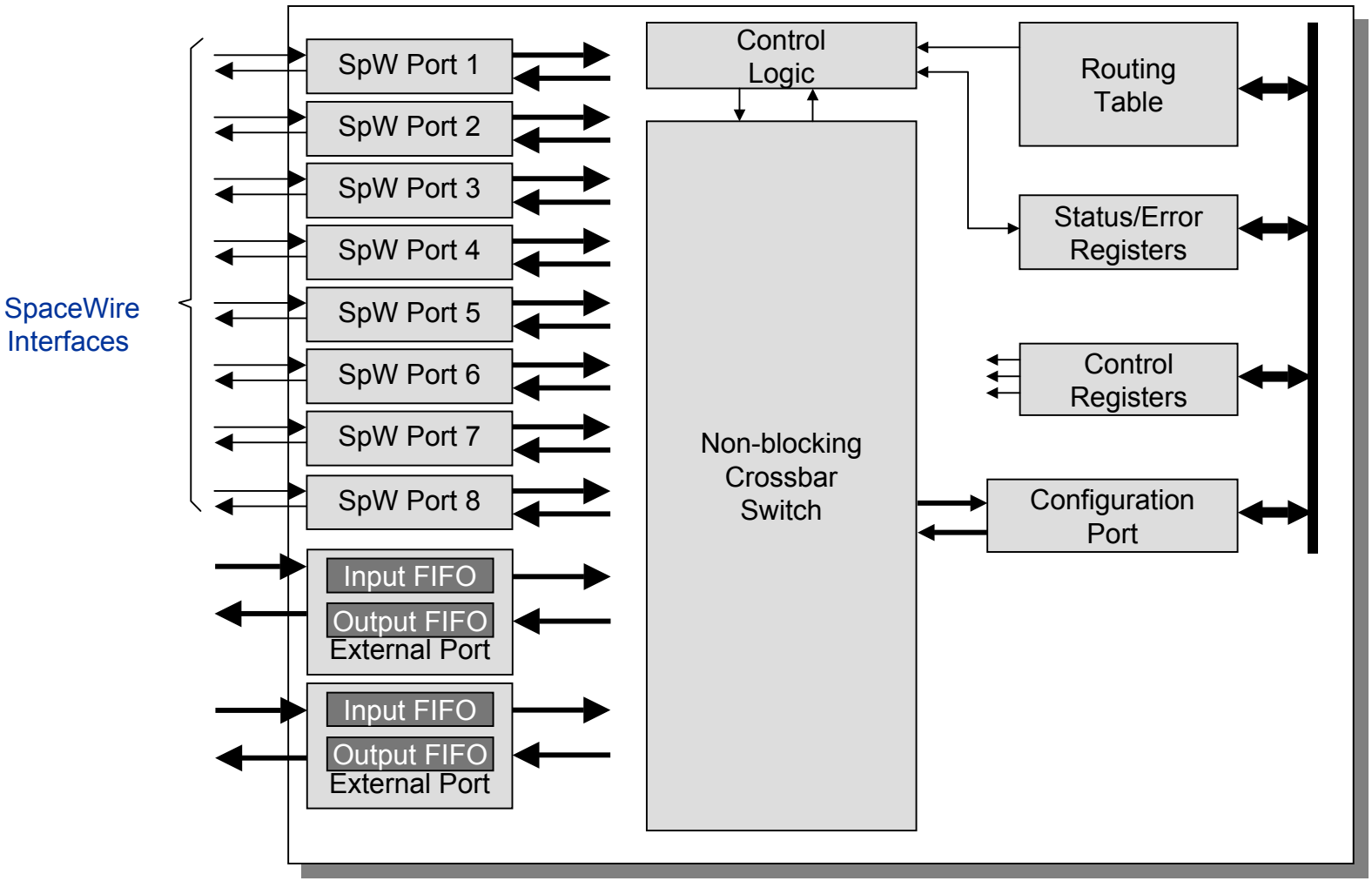


- IEEE1355 compliant
- Manufactured by Atmel
- Ref: T7906E

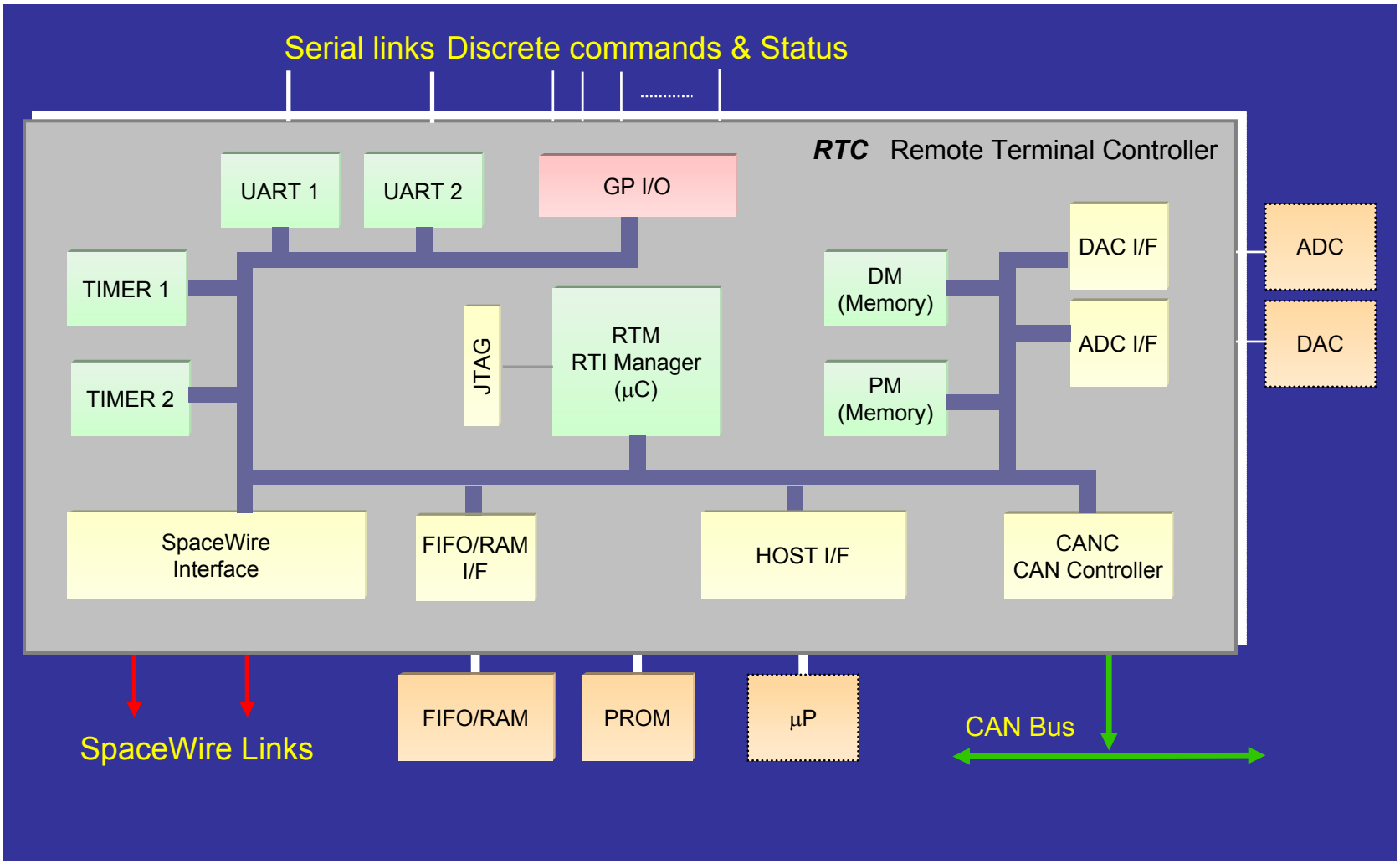
Under Development: SMCS116 SpW

- **ASIC**
  - Implementation in Atmel MG2RTP gate array
  - Max gate count 270 kgates (max technology)
  - 0.5 µm CMOS process
- **Radiation tolerance**
  - Up to 300 krad
  - SEU free cells to 100 MeV
  - Used for all memory cells
  - Latch-up immunity to 70 Mev
- **Performance**
  - SpaceWire interface baud-rate 200 Mbits/s
- Power
  - max 80mA at 5.5V at maximum data rate
  - 5 V and 3.3 V supply voltage
- **Package**
  - 100 pin ceramic Quad Flat Pack
- **Schedule**
  - Availability of prototypes: Q3 2005
  - Availability of flight parts: Q4 2005

Under Development: SpW Router Asic



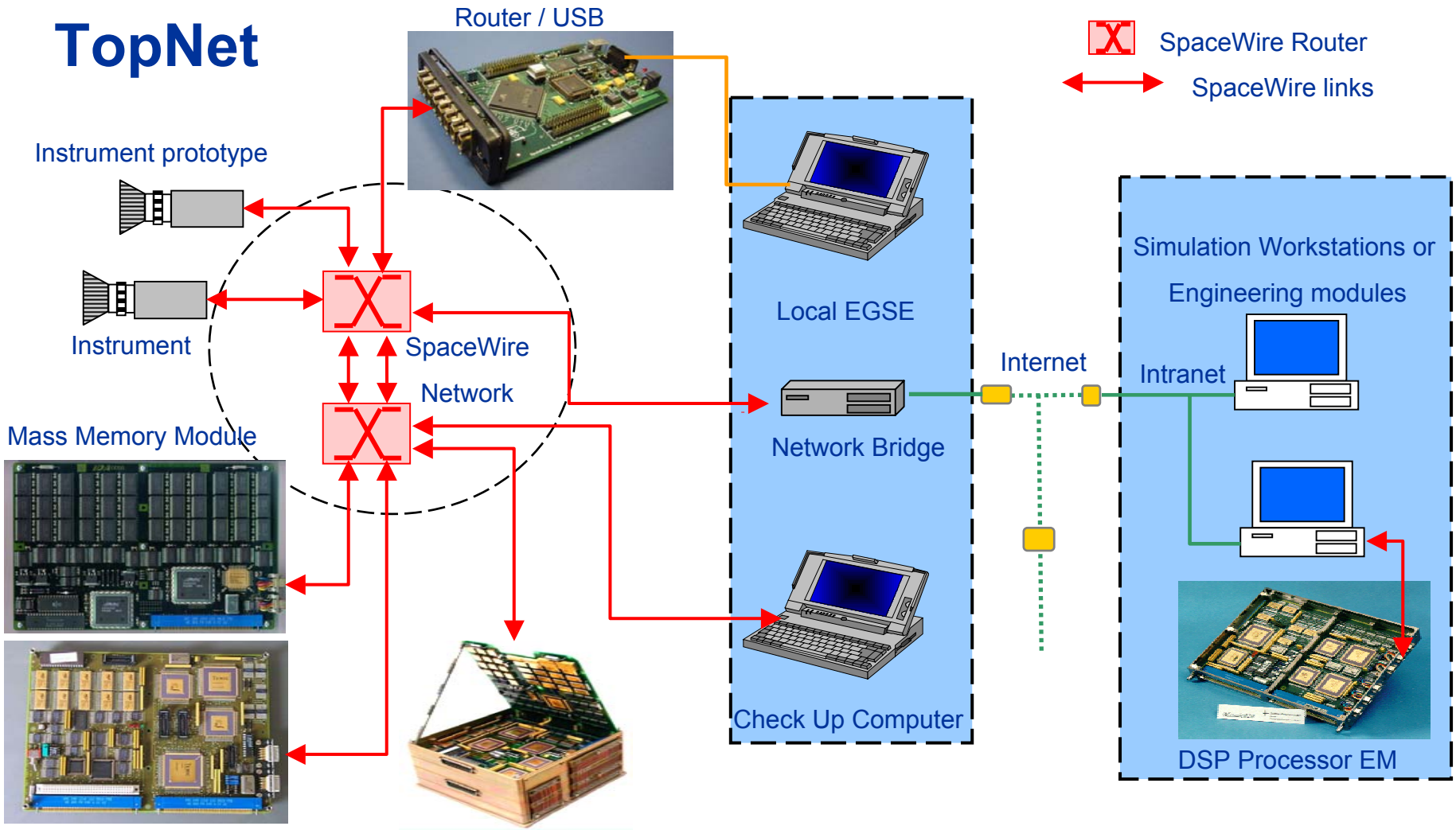
Under Development :SpaceWire Remote Terminal Controller



SpaceWire EGSE and support tools

- SpaceWire PCI Card
- SpaceWire USB Router box
- SpaceWire PCMCIA Card
- SpaceWire Link Monitor
- SpaceWire Protocol Analyser
- SpaceWire Conformance Tester
- Ethernet-to-SpaceWire bridge
- …

TopNet



New Concept for Geographically Distributed Test & Verification for Future Satellite Design

SpaceFibre

- SpaceFibre aims to be the very high speed extension (optical and TSP versions) of the SpaceWire standard

- Shall cover requirements of very high end applications
  - Higher data rates
  - Longer link length

- Core objectives of SpaceFibre activities:
  - Technology assessment of high speed optical data links
  - System architecture review and baseline design
  - Demonstrator detailed design and manufacturing
  - Environmental testing
  - Integration into SpaceWire network

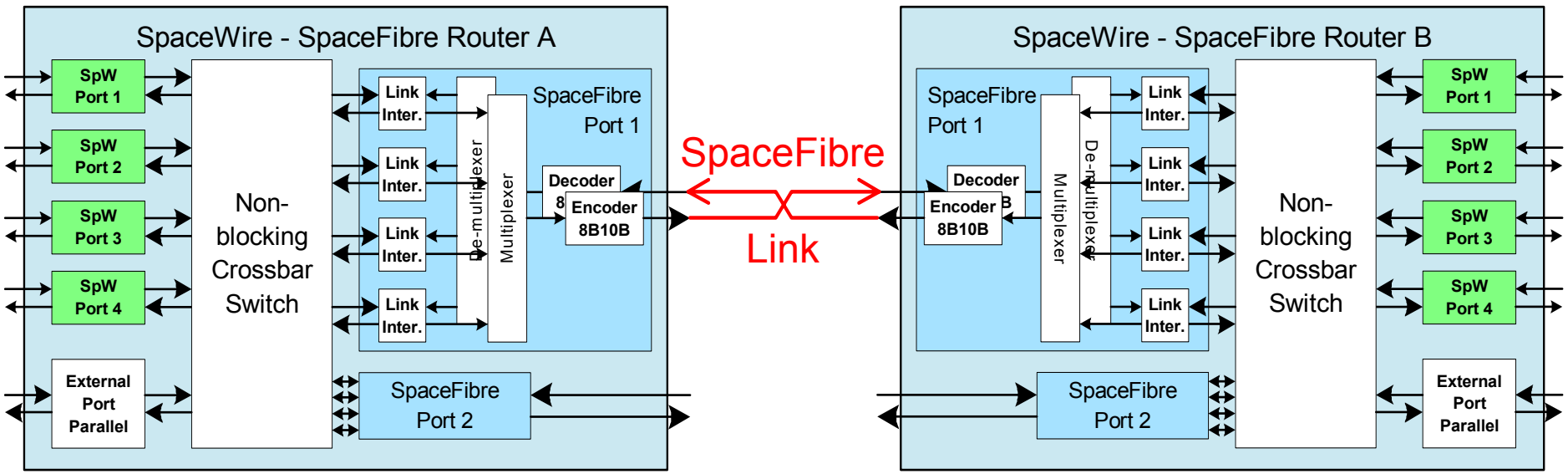
- Standardisation via the SpaceWire Working Group ?

SpaceFibre: Limitations of SpaceWire

- SpaceWire link data rate is currently 200Mb/s
  - High Resolution SAR, Hyper Spectral Imagers, High Speed High Resolution Cameras produce data at a rate of some Gb/s
  - Requires bundling of several SpaceWire links for these instruments
  - Higher system complexity and mass penalty
- Corresponding SpaceWire link maximum cable length is 10m
  - Limitation of data rate and cable length due to jitter and skew between on Data and Strobe signal
  - Sufficient for on satellite applications
  - Other applications like Launchers, Space Station and EGSEs for ground testing require longer cable length
- SpaceWire does not provide galvanic isolation
  - Often EMC requirement for connections between electronic boxes
  - Enables easier system integration on spacecraft level
  - Characteristic required for Ground Support Equipment

Mixed SpaceWire – SpaceFibre Network

- Transfer speed in network is determined by slowest link on the path
- SpaceFibre is slowed down by SpaceWire and capacity is not used
- One Solution:
  - Operation of several virtual SpaceWire Links over one SpaceFibre
  - Multiple link interfaces work synchronous in parallel
  - Fixed scheme for multiplexing – de-multiplexing characters in streams
  - Multiplexing avoids constraint on block size and use of big buffers



SpaceWire : Short Term Activities

- Production/validation of :
  - SMCS332-SPW Asic devices
  - SMCS116-SPW ASIC devices
  - SPW Router ASIC
- Specification and design of SpW-RTC, FPGA prototypes
- Freezing SpW-SnP-RMAP
- Develop a SpW-SnP-RMAP VHLD Macrocell
- Specify SpW-SnP-ADMIN procedures (Initialization, configuration)
- Support implementations for BepiColombo and GAIA and other projects
- Complete trade-offs and definition of SpaceFibre
- Complete the development of TopNet tools
- Define a TopNet Pilot demonstration scenario

SpaceWire : Medium Term Activities

- Production/validation of :
  - SpW RTC ASIC
  - Other devices with SpW Links (e.g. COLE ASIC, HIVAC, …)
- Harmonize SpaceWire supported services with CCSD SOIS
- Run TopNet Pilot demonstration
- Validate and demonstrate SpaceFibre concepts
- Extend the usage of SpW networks from Payload Data Processing systems to Avionics