The new SpaceWire compliant SMCS332 / SMCSlite ASIC

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Outline

- **Introduction**

- **Motivation**

- **New SMCS332SpW   New Features / Functions**

- **New SMCS116SpW   New Features / Functions**

- **Compliance to the new SpaceWire protocol**

- **SMCS332SpW / SMCS116SpW ASIC**

- **Industrial Team**

- **Schedule**

Introduction

SMCS   (Scalable Multi-channel Communication Sub-system)

- **communication controller ASIC**
- **for space applications (radiation tolerant)**

Tasks:

- **hardware supported execution of major parts of the inter-processor protocol**
- **provide a fast interface to serial protocol**

Introduction – The current SMCS

SMCS332/TSS901E

● **bases on IEEE-1355 protocol**

● **3 IEEE-1355 links with up to 200 Mbit/s data transmit rate**

● **each parallel interface can be configured to 8, 16 or 32 bits**

● **checksum generation/check at packet level**

SMCS116/T7906E (SMCSlite)

● **bases on IEEE-1355 protocol**

● **1 IEEE-1355 link with up to 200 Mbit/s data transmit rate**

● **RAM / FIFO / DAC / ADC Interface**

● **Timer**

● **UART**

● **GPIO**

● **each parallel interface can be configured to 8 or 16 bits**

● **checksum generation/check at packet level**

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Introduction – The current SMCS

Satellite on-board data network
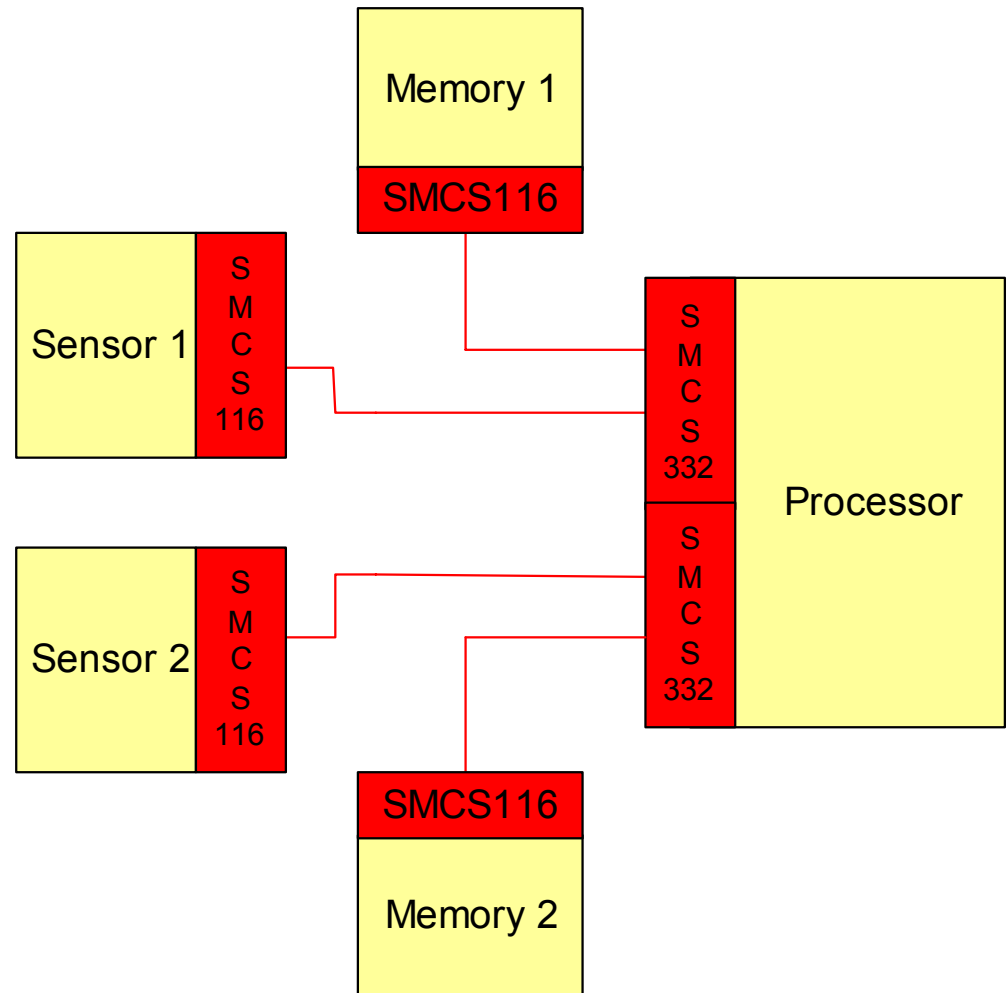
- point-to-Point Network
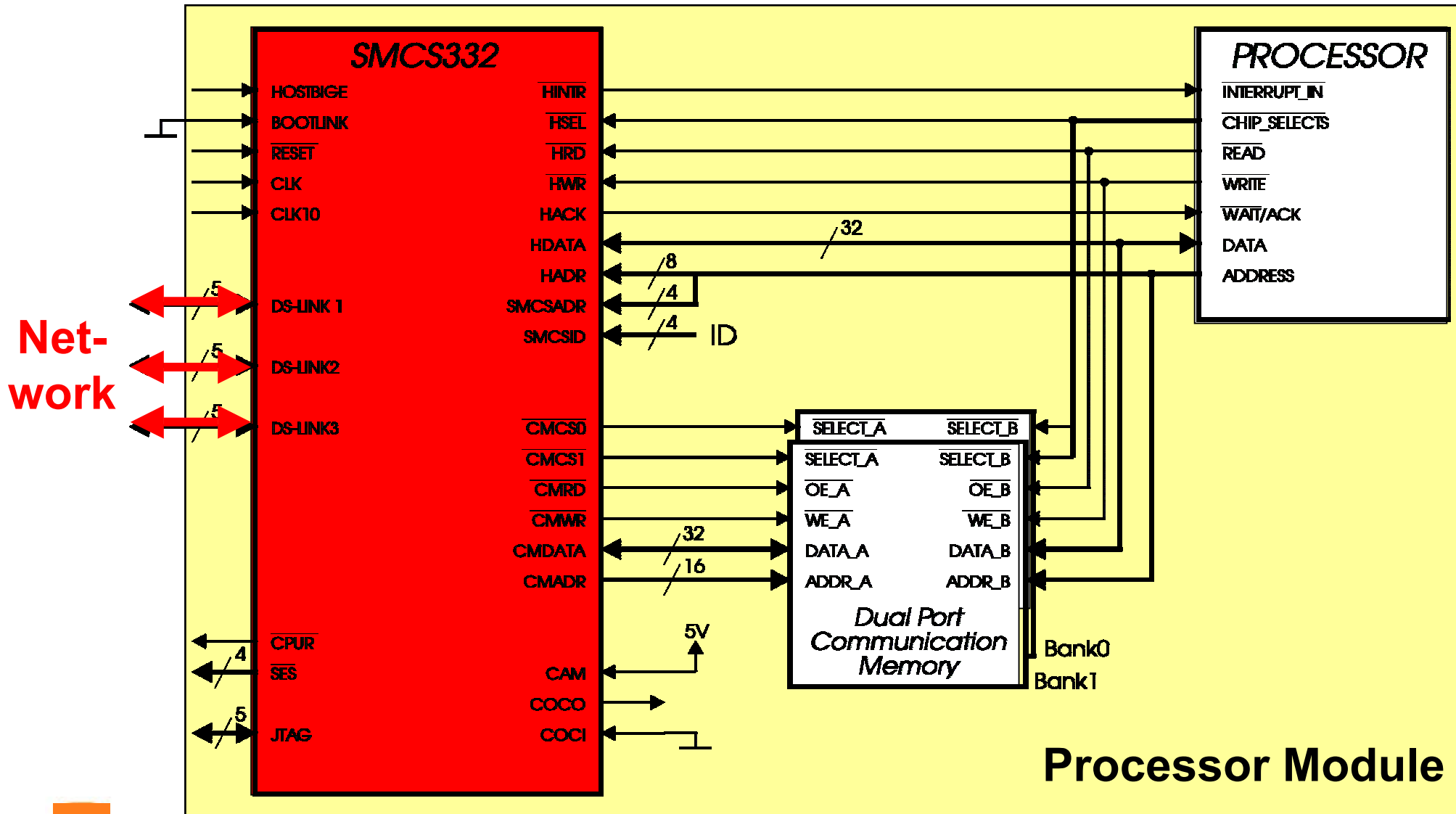- IEEE1355 / SpaceWire
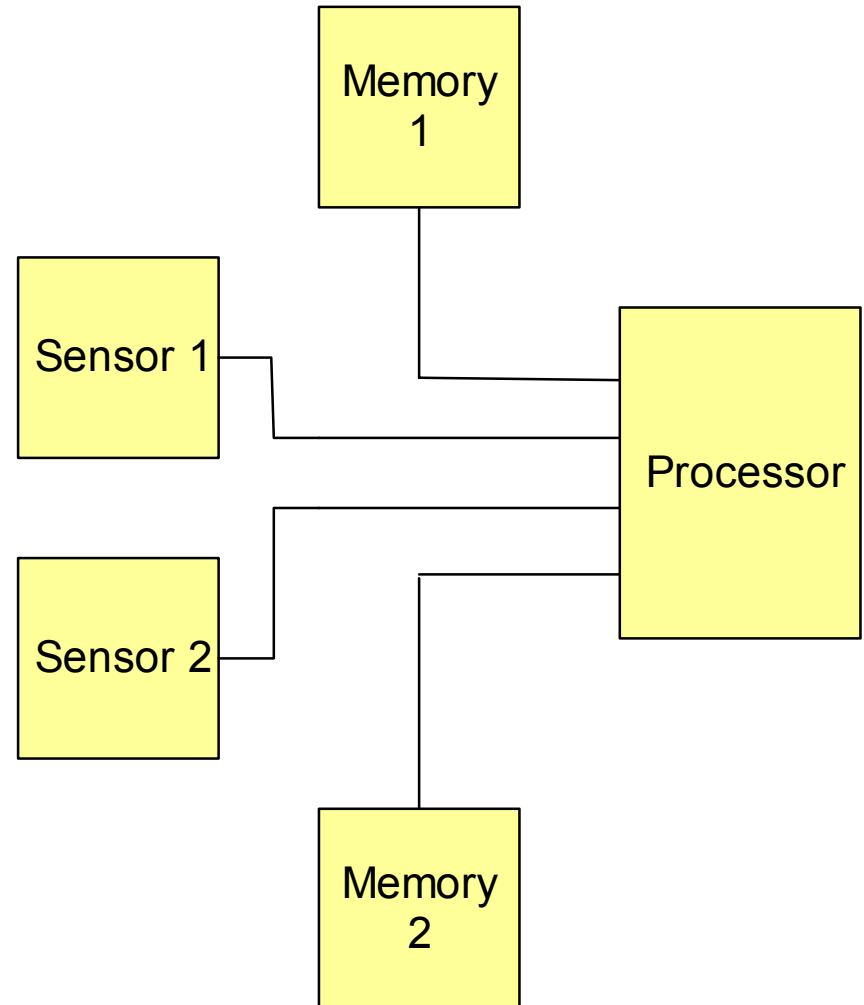
Introduction – The current SMCS

Application of SMCS ASICS

**IEEE 1355
or SpaceWire network**
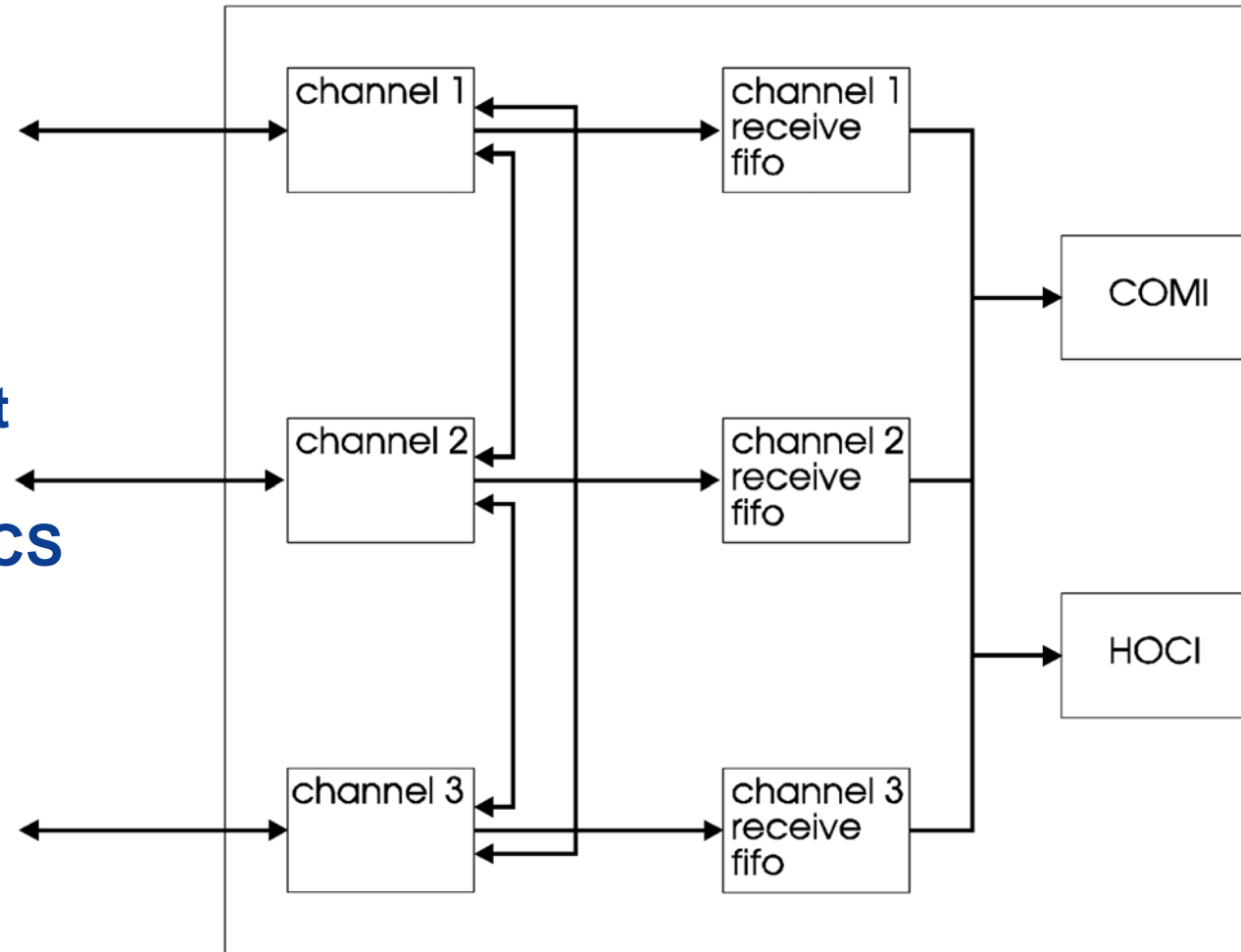
SMCS332 in typical module environment

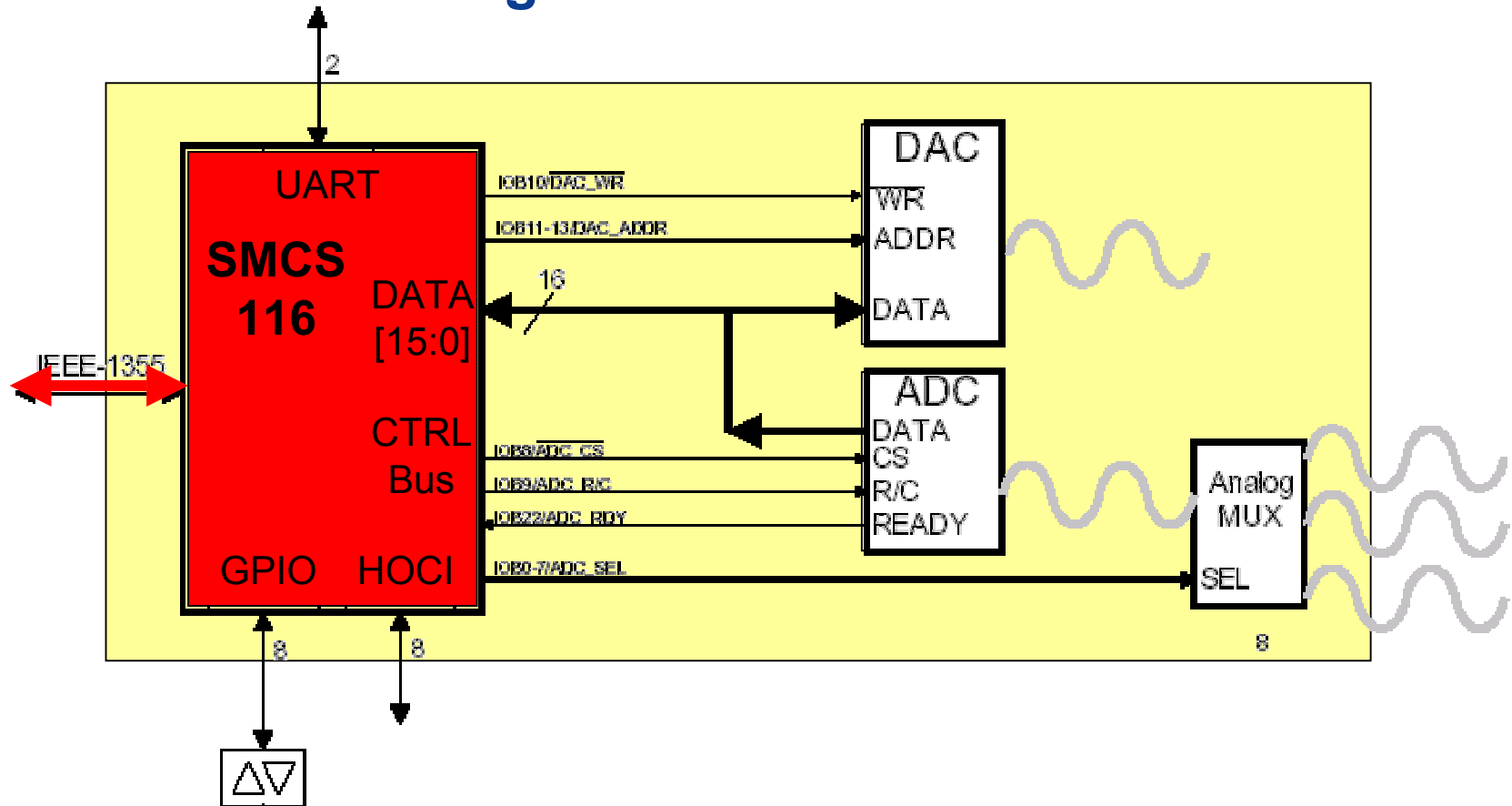© **EADS Astrium GmbH**

Wormhole Routing SMCS332

Wormhole Routing (Router functionality)

- SMCS receives packet
- header determines output port
- packet flows through SMCS
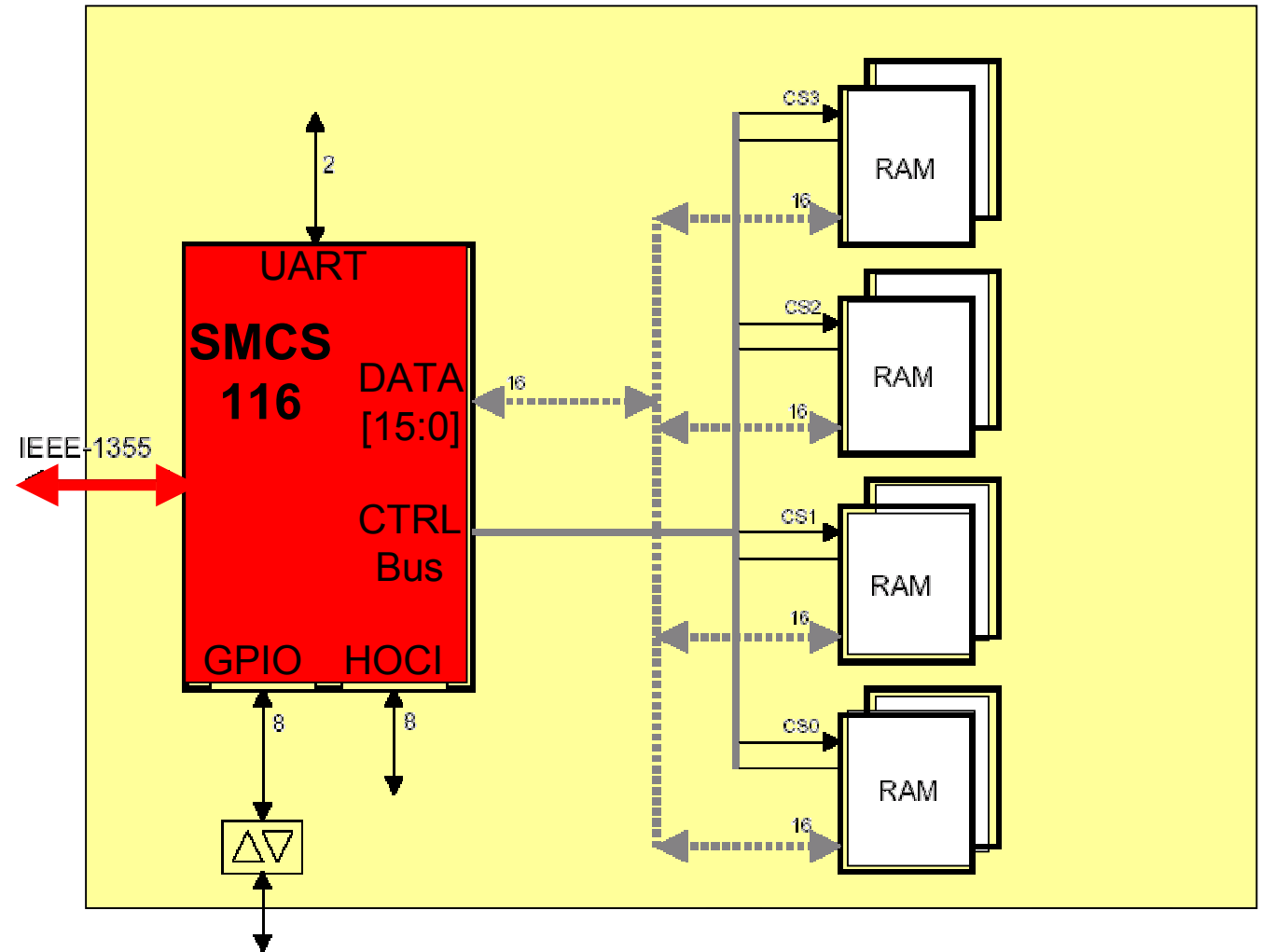- EOP marker terminates connection

SMCSlite Applications

SMCSlite as communication and system controller on an interface node consisting of an ADC and DAC.

SMCSlite Applications 2

SMCSlite connected to four banks of memory.

SMCSlite Applications 3

Communication device for microprocessors
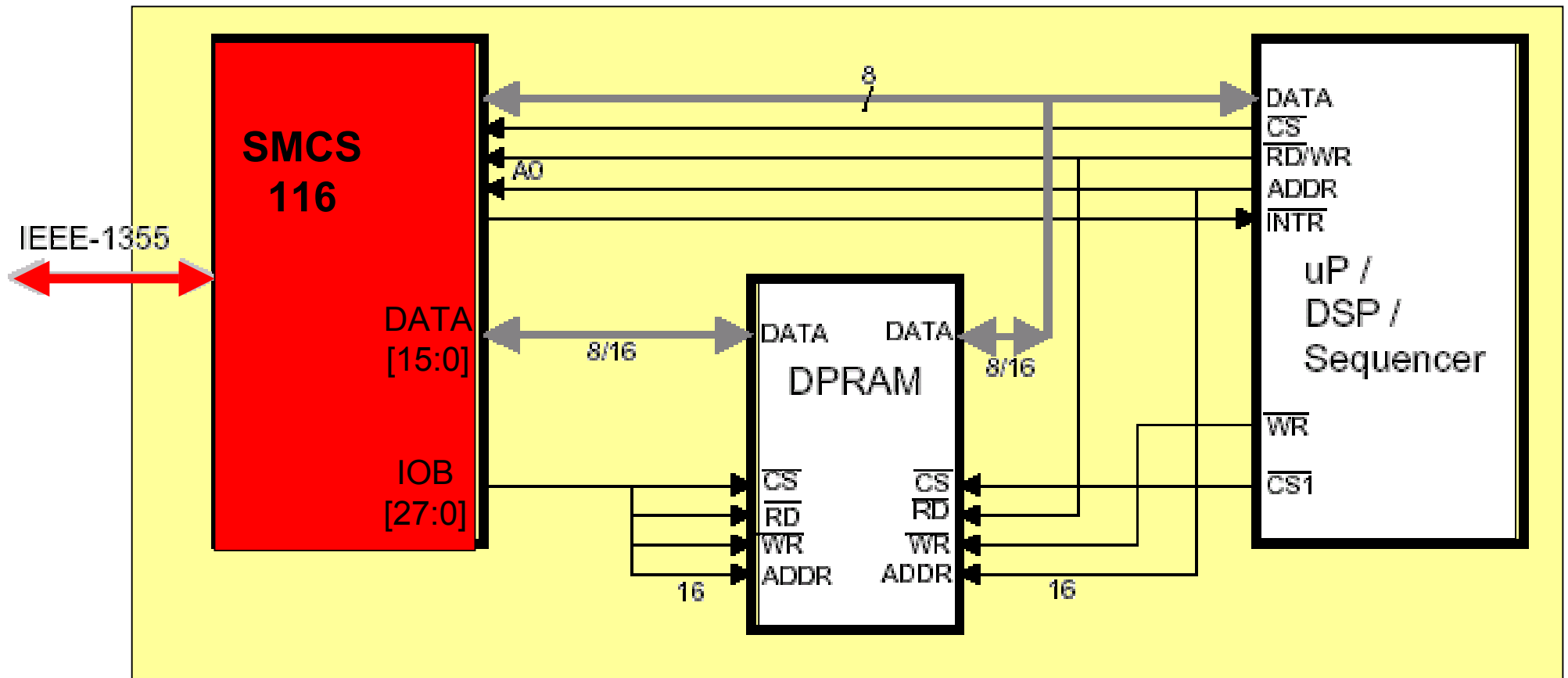
Introduction   SMCS332

- **3 bi-directional link channels**
  each with DS macro cell,
  receive, transmit section,
  protocol processing unit

- **COMI: Com Memory Interface**
  performs autonomous accesses
  to the communication memory

- **HOCI: Host Control Interface**
  gives r/w access to config reg
  and to DS channels for the CPU

- **PRCI: Protocol Command
       Interface**
  collects commands from
  protocol units

- **JTAG: Test Interface**
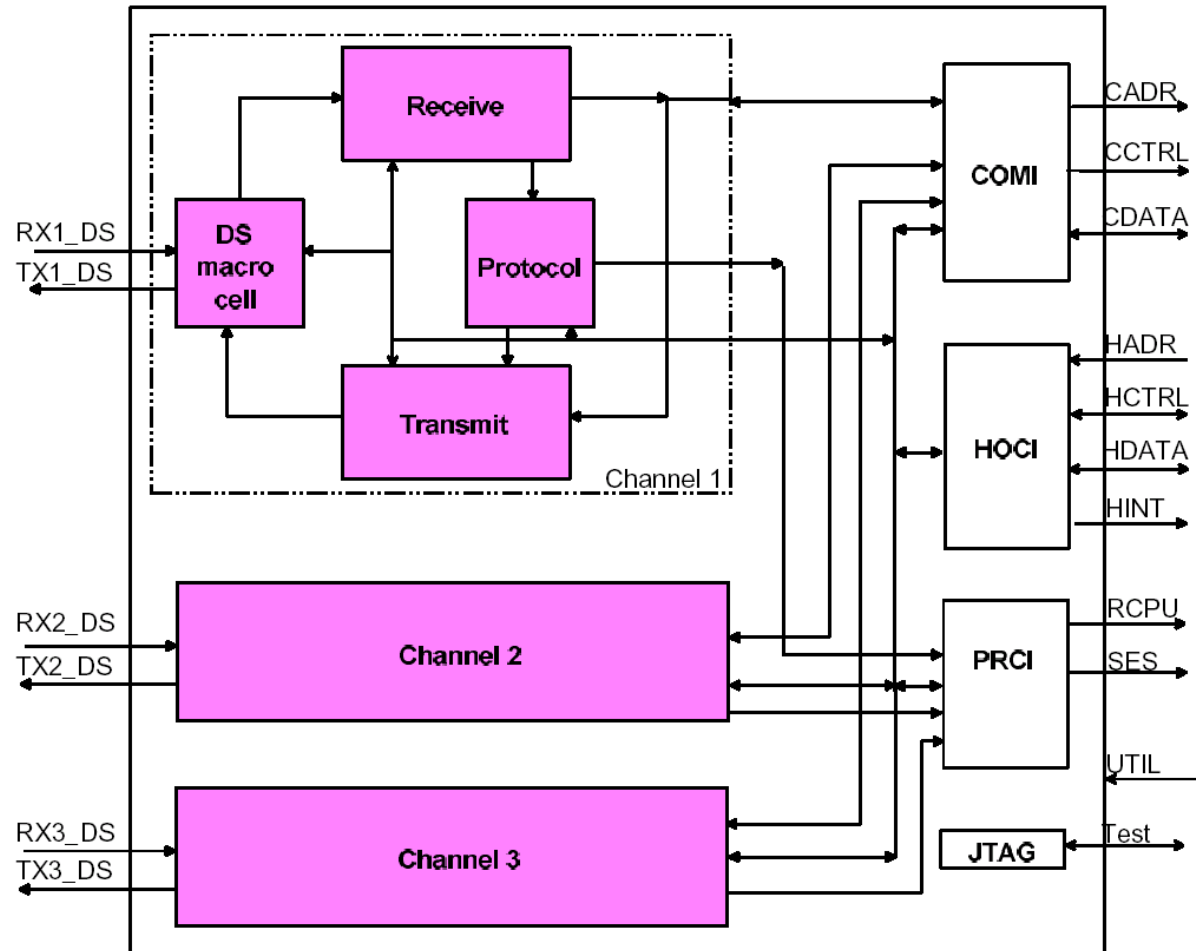
Introduction SMCS116

Link Interface: Interface to serial IEEE-1355 link

Host Interface: Chip can be programmed & controlled by a local host

ADC/DAC I/F: allows the read (write) from an AD (DA) converter

RAM IF: 4 different banks of memory are addressable

FIFO I/F: provides control signals (full, write, empty, read)

GIPO: General Purpose Interface

UART: 2 independent UARTs

JTAG: Test Interface

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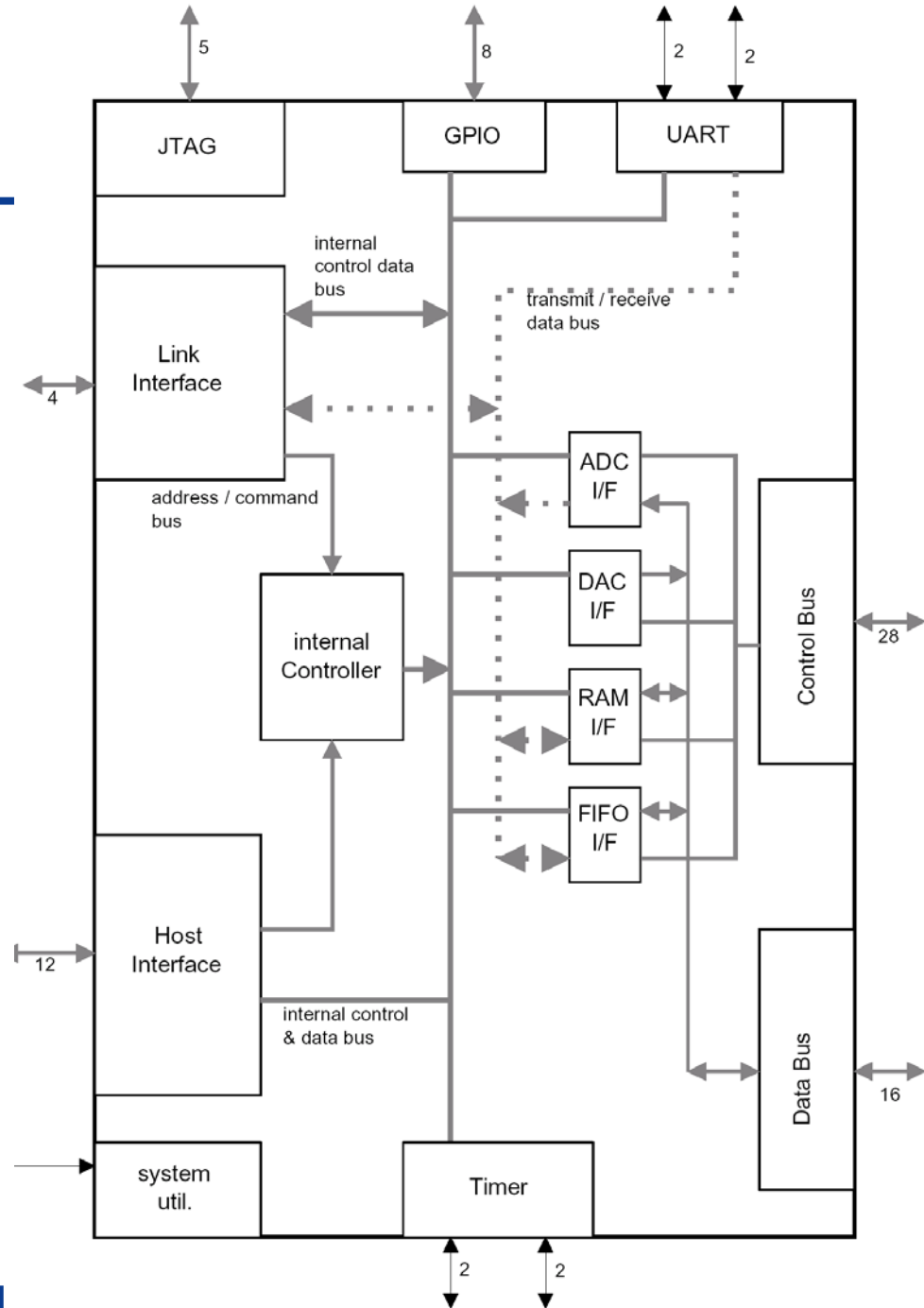
Motivation

Motivation for new SMCS SpW ASICs

● **SMCS ASICs are often used communication controllers**
● **SpaceWire standard is becoming increasingly important**

Requirements for the new SMCS SpW

● **SpaceWire compliant (ECSS-E-50-12A, 24-Jan-2003)**
● **Pin compatible to existing SMCS332 / SMCSlite**
  cannot be achieved completely

● **correct known anomalies of the existing SMCS ASICs**
● **Goal: Backward compatibility concerning software**

Pin-compatibility

Due to a new PLL in the MG2RT technology the pin-out of the new SMCS chips has to be slightly changed.

- **Pin change of the SMCS332SpW:**

	current		new
	current		new
- Pin#1	VCC	->	PLLOUT
- Pin#3	GND	->	VCC
- Pin#169	NC	->	VCC_3VOLT
- Pin#175	LEN1	->	not used (GND)
- Pin#182	LEN2	->	not used (GND)
- Pin#192	LEN3	->	TIME_CODE_SYNC
- Pin #196	PLLOUT	->	GND

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SMCS332SpW / SMCS116SpW - New Features

New Features due to the SpaceWire Interface:

● **The new SpaceWire interface is resistant against simultaneous switching on the D, S inputs**

● **It is 'hot' plug able (no master-slave situation has to be arranged)**

● **The SpaceWire Interface transmits / receives the new time code characters**

  - Therefore 2 additional registers are used

● **The new SpaceWire Interface has no EOP2 token**

  - EOP is End Of Packet marker (former EOP1)
  - EEP is End of Error Packet marker (former EOP2)

SMCS332SpW - New Functions

Anomaly Correction:

● **All known anomalies (#B.1 – #B.5) will be corrected.**

New Functions :

● **Time code**

   - The SMCS332SpW can send Time Code characters

   - The SMCS332SpW can be used as Time Code master

● **New header field control bit**

   - more flexibility for packet generation

SMCS332SpW - New Functions

● **Arbitrary packet length**

SMCS332:

- the difference between end address and start address gives the packet length

- each packet is automatically completed with an EOP

SMCS332SpW:

- an additional bit prevents from the automatic EOP

- this allows arbitrary packet lengths

Attention: Finally the packet should be completed with an EOP!

SMCS332SpW - New Functions

Removal of packet size restrictions

● **Receive data over HOCI FIFO**

- SMCS332: maximum 4 bytes packets (if host interface is operated in 16 or 32 width mode)

- SMCS332SpW: no restriction for the packet size

● **Transmit data over COMI**

SMCS332:

- COMI in 8 bit modes: only packets of size n*4+4 (or n*4+3) bytes should be sent

- COMI in 16 bit modes: only packets of size n*4+4 bytes should be sent.

SMCS332SpW: no restrictions for the packet size

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SMCSlite-SpW - New Functions

Anomaly Correction:

● **The known anomaly (#A.1) will be corrected.**

New Functions :

● **Protocol**

  - the protocol engine will be modified that it tolerates and executes commands of any length

  - rest of a packet (read beyond 1 byte; write beyond 2 bytes) will be ignored

● **Time code**

  - The SMCS116SpW can send Time Code characters

  - The SMCS116SpW can be used as Time Code master

SMCSlite-SpW - New Functions

- **FIFO**

  - support of 16 bit data bus in active and passive mode

- **UART**

  - implementation of an additional interrupt which is set if the transmit FIFO is empty

- **ADC**

  - the timing/ sequence during the use of an external analogue multiplexer will be modified

Compliance to the new SpaceWire protocol

SMCS332SpW

● The SMCS332SpW directs all received data directly to the SW. Therefore, the SW has to handle the protocol and the SMCS332SpW is fully compliant to the new protocol.

SMCS116SpW

● The new SMCS332SpW will be able to handle data transfers without protocol and will be compliant to the new SpaceWire protocol in the way that a special protocol identifier is used for the chip.

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SMCS332SpW / SMCS116SpW - ASIC

SMCS332SpW

- Radiation tolerant gate array technology from Atmel
- MG2RT
- 196 pins
- 5 V and 3.3 V version (performance of 3.3V version: 100MBit/s)

SMCS116SpW

- Radiation tolerant gate array technology from Atmel
- MG2RTP
- 100 pins
- 5 and 3.3 V version (performance of 3.3V version TBC)

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Industrial Team

The Upgrade of the SMCS ASICs is an ESA project.

The SMCS332SpW / SMCS116SpW will be developed and tested by EADS Astrium GmbH.

The ASICs will be manufactured by Atmel who also provide the customer support for the chip.

Additional support for applications (boards, drivers, test equipment) will be provided by University of Dundee through STAR-Dundee.

Schedule

Schedule:

Project KO: **May 2004**

Prototype manufactured:
- **SMCS332SpW**   **done; tests running**
- **SMCS116SpW**   **Q2 2005**

ASICs available: **Q3 2005 (TBC)**

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