SpaceWire Active Backplane (SpWAB) Specification

Presented at: 14th SpaceWire Working Group
Date: 23rd February 2010
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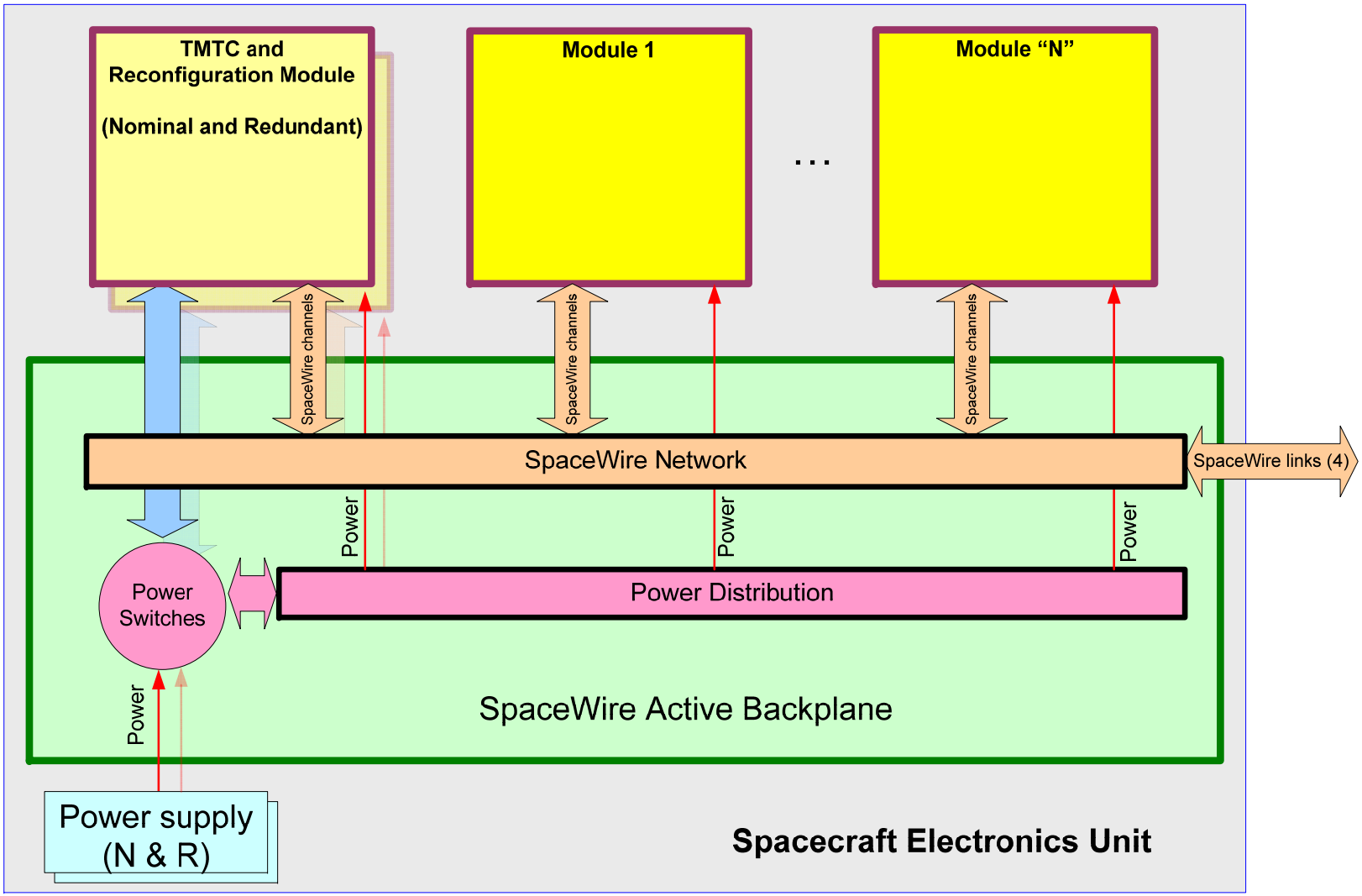
Why an active backplane?

- Decouples SpaceWire network and power distribution architecture from the Module design
- Scalable to suit module count and bandwidth requirements
- Modules do not need to be powered in certain combinations to provide the connectivity required
- Permits a common backplane interface
- Improved FDIR hierarchy

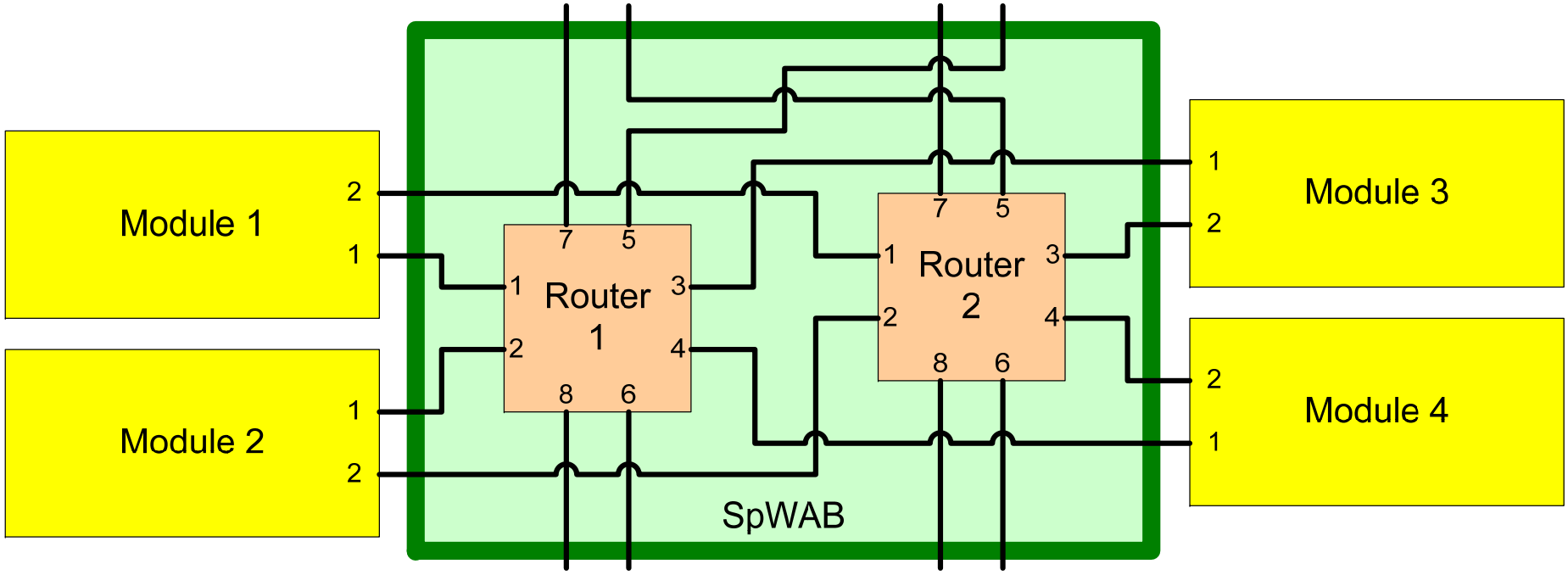
SpWAB context



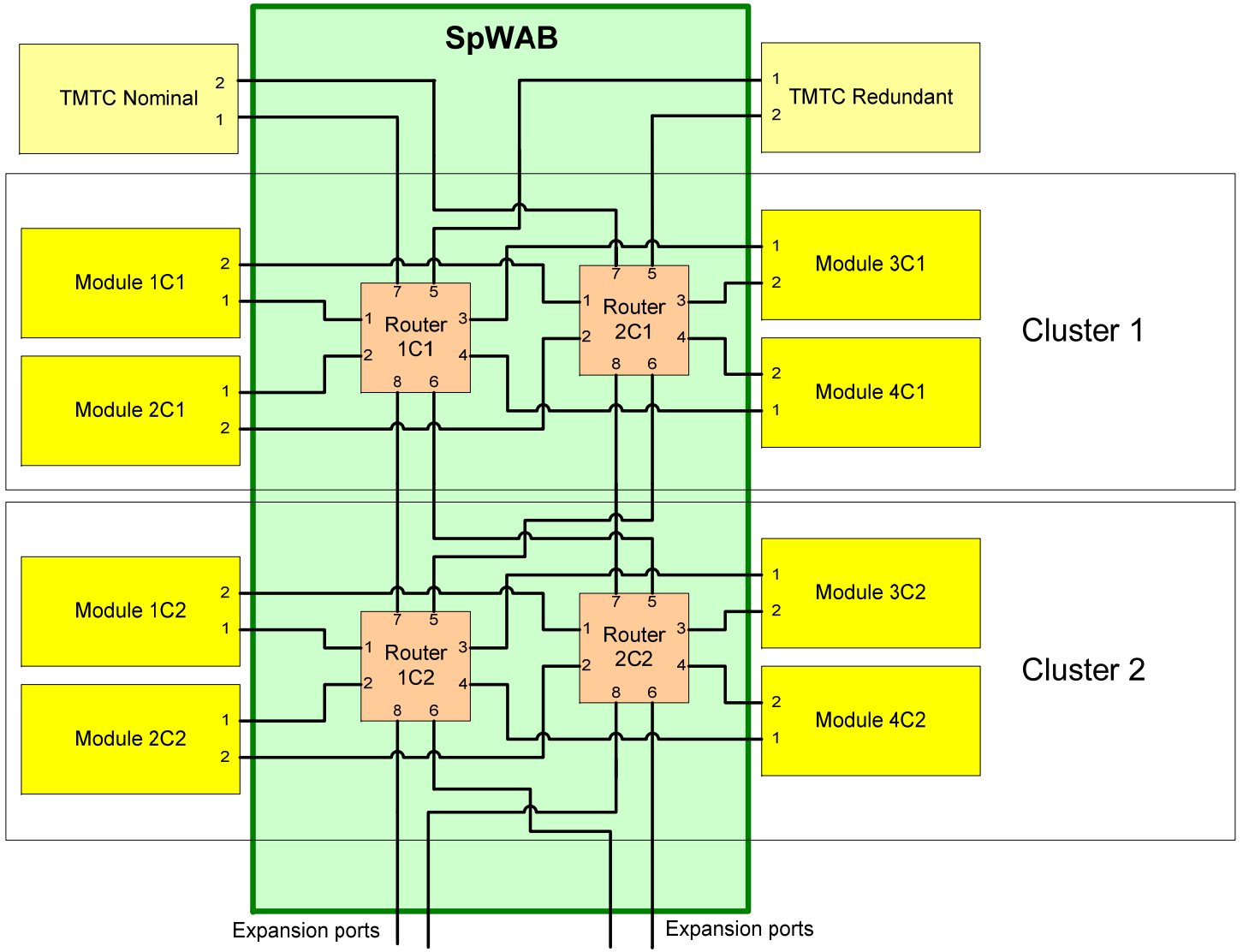
Network topology constraints

- SpaceWire network is to connect Modules
- Network is built from 8 port routers
- Need to avoid single point failures and failure propagation, this means that each Module must interface to at least 2 routers
- Should not rely on a Module to provide routing capability between ports (otherwise that Module must be powered)
- Links from a Router must also connect to other Routers to provide scalability
- Need “Spare” ports for EGSE connection and network expansion

Network building block (Cluster)



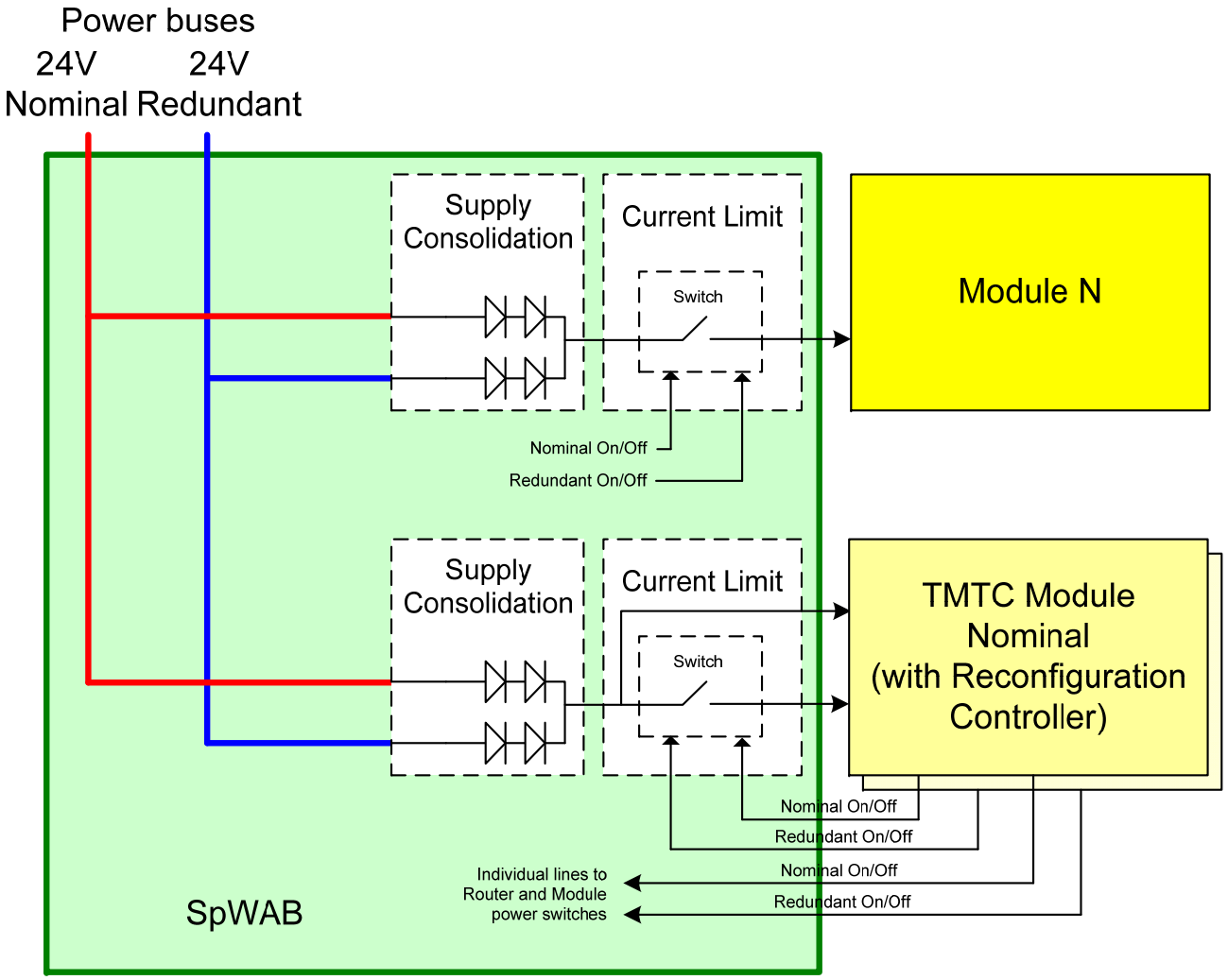
Cluster to Cluster connections



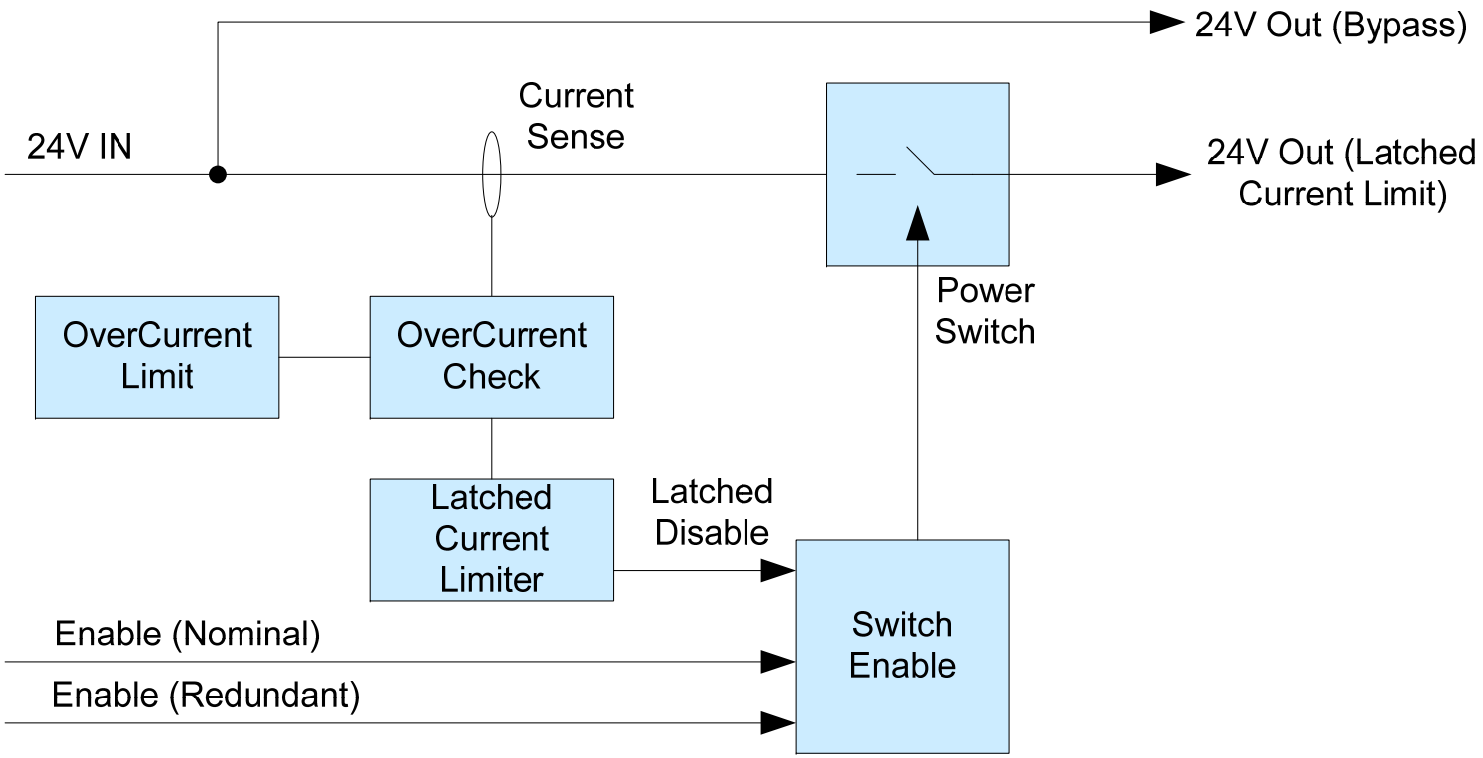
Power distribution

- In a SpaceWire network architecture with an "n from m" redundancy approach we need to have some power control over each Module; this permits failed or unneeded Modules to be powered off
- The power architecture has to be similar to the Network architecture and take into account the potential need to switch off Routers
- The electronics on each Module will have different power and voltage needs so a generic architecture needs to take this into account
- The current thoughts are that a regulated voltage (24V) will be supplied to each Module and that Point Of Load (POL) converters will be employed on each Module to provide the voltage rails they need
- It is anticipated that a Module would need less than 20 watts
- The POL approach is a typical of commercial hardware due to the range of logic supply rails needed and the availability of high efficiency compact power modules
- The Module power switches are under centralised control
- If no master processor appears to be in control then reconfiguration hardware will decide which Modules are powered (with TC over-ride)

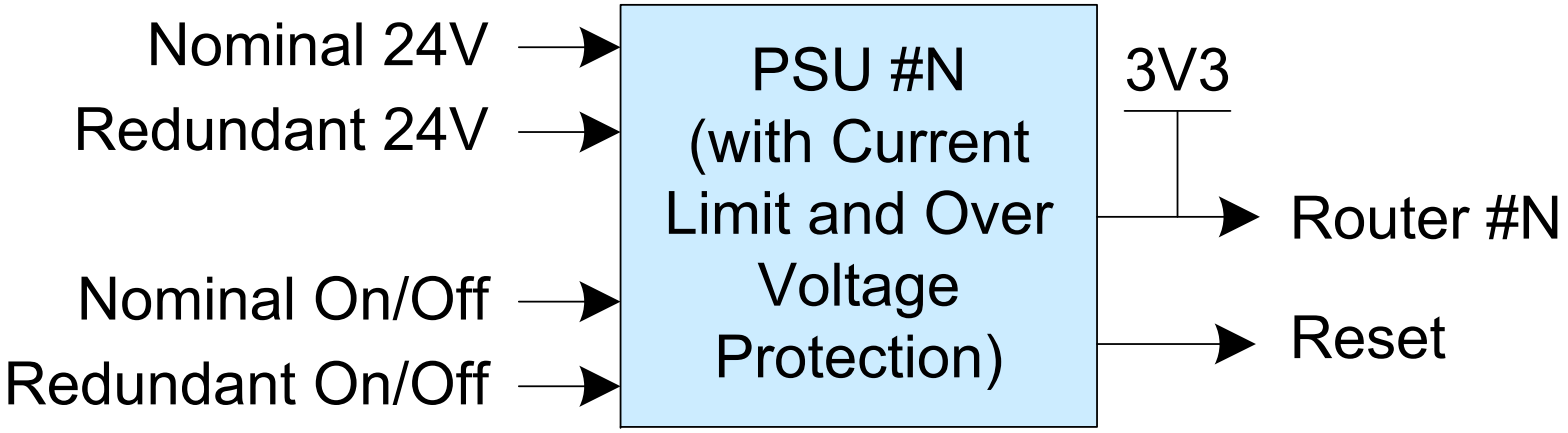
Module power architecture



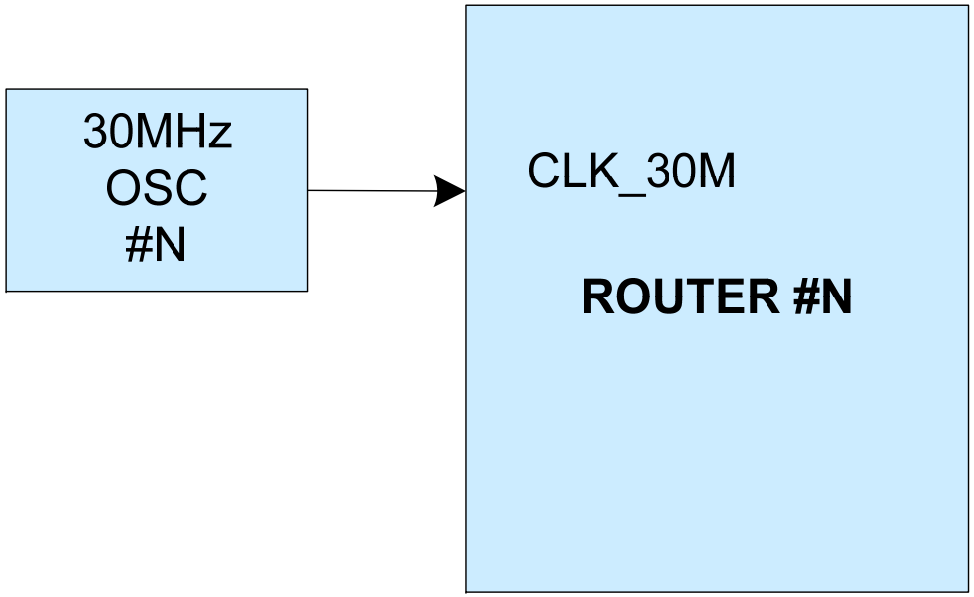
Module power (LCL)



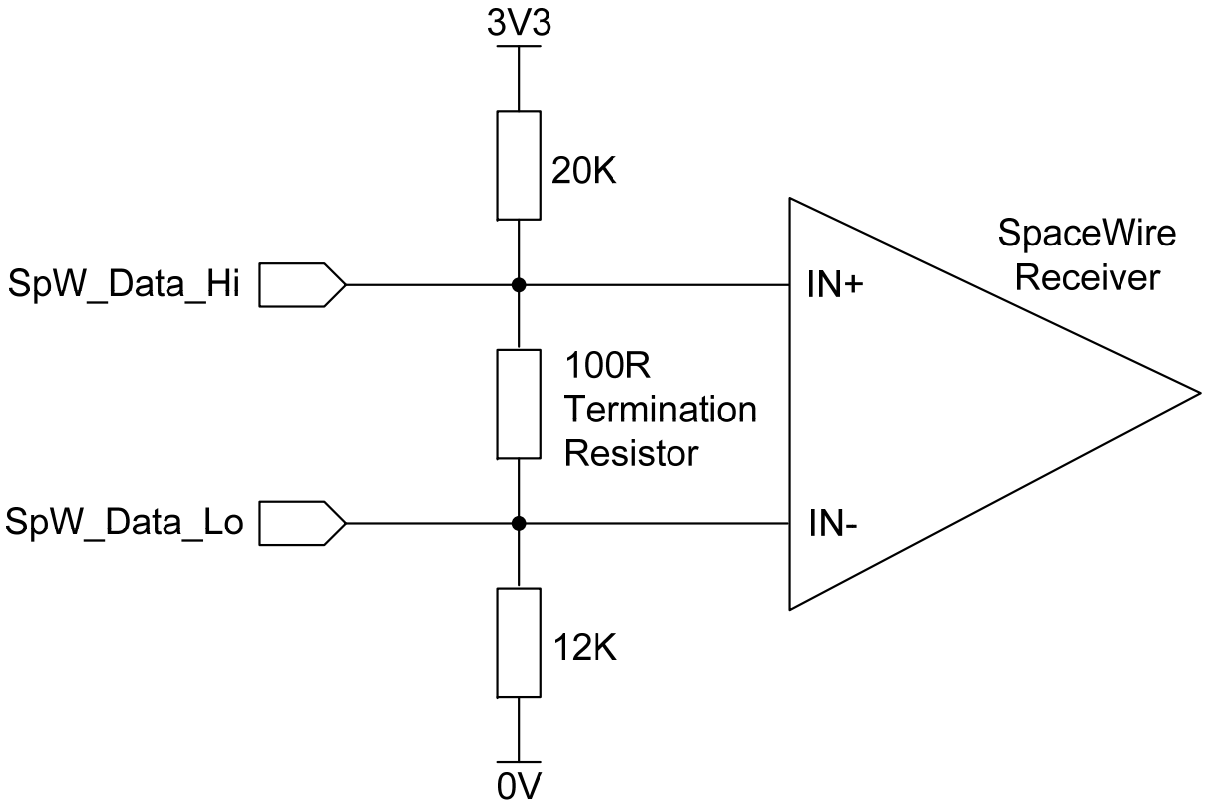
Router power



Router clock



Router input safe bias



Reconfiguration Controller

- Hardware only controller
- Coupled to TMTC function to permit ground access without the need to power up and configure a SpaceWire network
- Switches power to the Routers in at least 1 master Cluster
- Provides discrete lines to switch on Modules and Routers
- Contains watchdogs that monitor the heartbeat (health message) from the master processor
- Contains a table based sequencer that follows a timed isolation and recovery sequence when watchdog signal failures detected

Advantages of this architecture

- Single point failure proof
- Same number of routers in path after a single router failure
- No failure propagation that stops Modules in other clusters communicating on any port
- Good inter-cluster bandwidth (200Mbps)
- Spare ports for expansion or EGSE
- Opportunity to use Group Adaptive routing to automatically bypass bad links and routers

Backplane connectors

- Ideally we need a controlled impedance connector to avoid SpaceWire signal degradation
- No suitable space approved connector identified
- In 2008 SEA consulted Hypertac and proposed development of a connector using Twinax contacts
- The Hypertac connector is at the conceptual stage and needs development funding

Proposed Hypertac connector

- **Sabritec 100 ohm Twinax contacts are a potential candidate for Space applications**
- **Connector based on 119 contact HPH series body (~95mm long)**
- **Body can contain 8 Twinax contacts and 36 standard power/signal contacts**

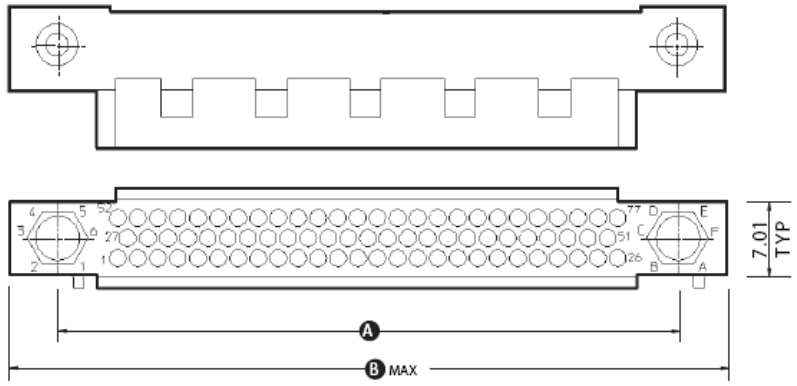
HPH connector body

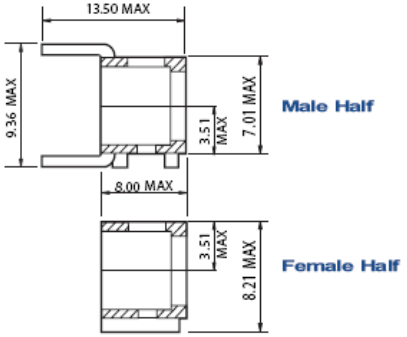
HPH Series

HYPERTAC

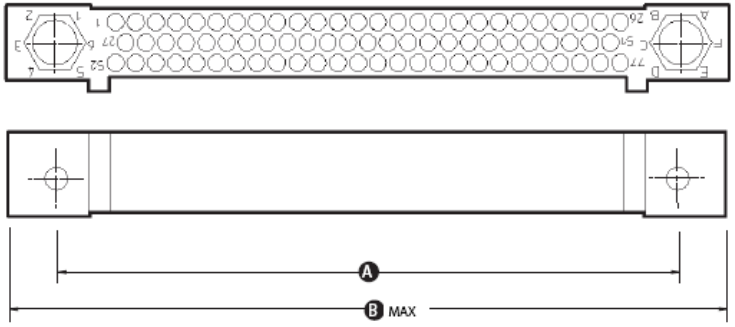
HPH insulators

3 ROW Male Half





3 ROW Female Half

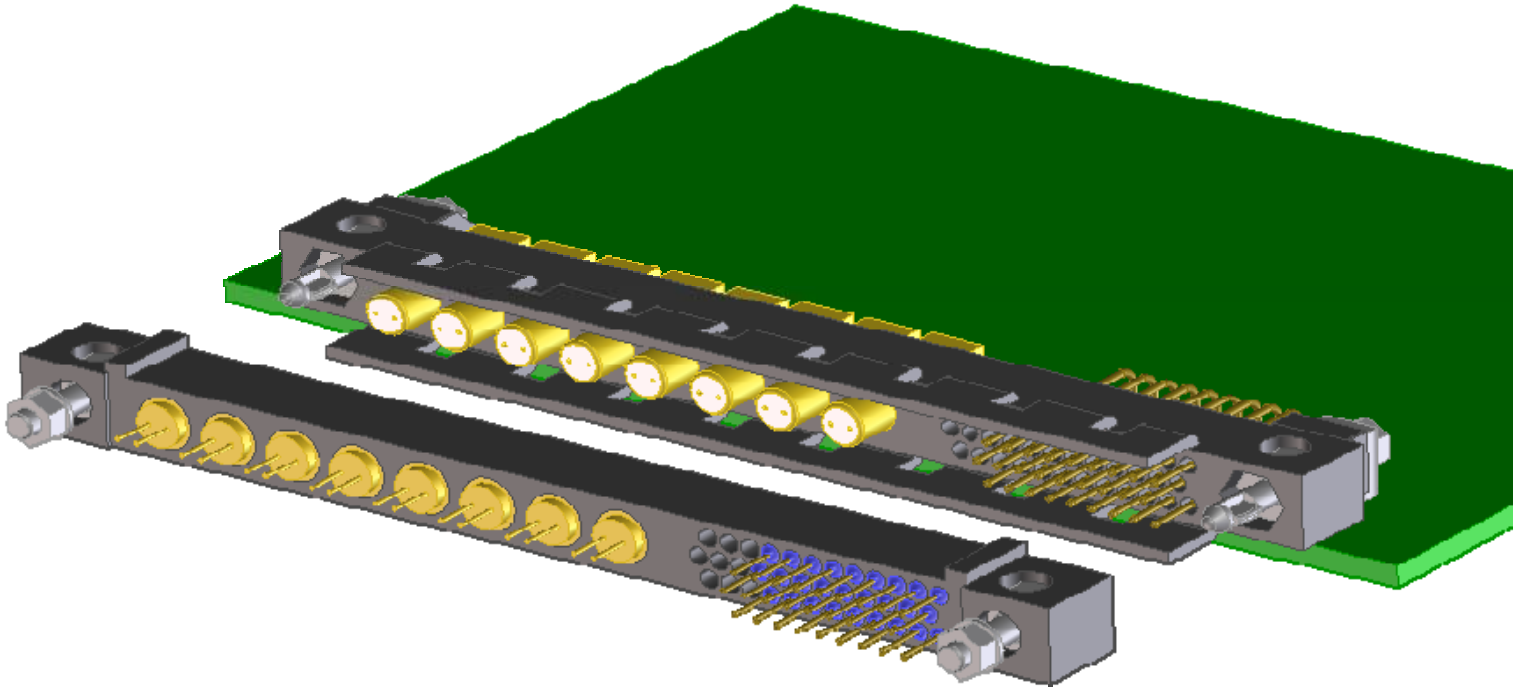


No. OF POSITIONS	20†	50*	77*	119*	152*
Dimension A	22.86 *0.901"*	41.91 *1.65"*	59.06 *2.325"*	85.73 *3.375"*	106.68 *4.200"*
Dimension B	32.18 *1.267"*	51.23 *2.017"*	68.38 *2.692"*	95.05 *3.742"*	116.50 *4.586"*

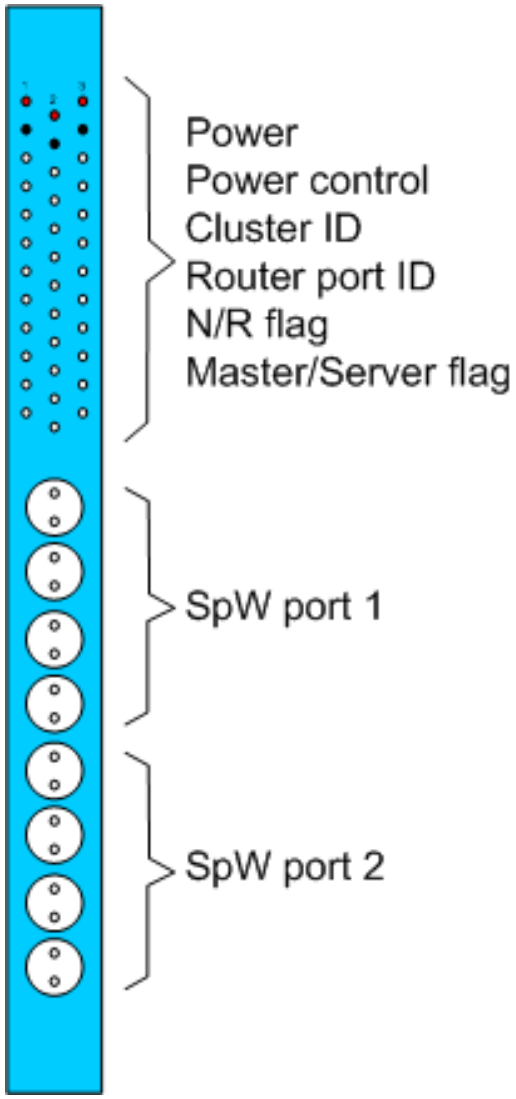
* Off the shelf

† Subject to availability

Connector concept



Contact allocation



TwinAx Pin	Signal
TA1 Pin 1	SPW 1 DATA IN +
TA 1 Pin 2	SPW 1 DATA IN -
TA 2 Pin 1	SPW 1 STRB IN +
TA 2 Pin 2	SPW 1 STRB IN -
TA 3 Pin 1	SPW 1 DATA OUT +
TA 3 Pin 2	SPW 1 DATA OUT -
TA 4 Pin 1	SPW 1 STRB OUT +
TA 4 Pin 2	SPW 1 STRB OUT -
TA 5 Pin 1	SPW 2 DATA IN +
TA 5 Pin 2	SPW 2 DATA IN -
TA 6 Pin 1	SPW 2 STRB IN +
TA 6 Pin 2	SPW 2 STRB IN -
TA 7 Pin 1	SPW 2 DATA OUT +
TA 7 Pin 2	SPW 2 DATA OUT -
TA 8 Pin 1	SPW 2 STRB OUT +
TA 8 Pin 2	SPW 2 STRB OUT -

Contact allocation (2)

Pin	Signal
Pin 1	Protected +24V
Pin 2	Protected +24V
Pin 3	Protected +24V
Pin 4	0V
Pin 5	0V
Pin 6	0V
Pin 7	Module 1 On
Pin 8	Module 1 Off
Pin 9	Module 2 On
Pin 10	Module 2 Off
Pin 11	Module 3 On
Pin 12	Module 3 Off
Pin 13	Module 4 On
Pin 14	Module 4 Off
Pin 15	Module 5 On
Pin 16	Module 5 Off
Pin 17	Module 6 On
Pin 18	Module 6 Off
Pin 19	Module 7 On
Pin 20	Module 7 Off
Pin 21	Module 8 On
Pin 22	Module 8 Off
Pin 23	Router 1 On
Pin 24	Router 1 Off
Pin 25	Router 2 On
Pin 26	Router 2 Off
Pin 27	Router 3 On
Pin 28	Router 3 Off
Pin 29	Router 4 On
Pin 30	Router 4 Off
Pin 31	TMTC On
Pin 32	TMTC Off
Pin 33	0V
Pin 34	Direct 24V
Pin 35	0V
Pin 36	Direct 24V

Pin	Signal
Pin 1	Protected +24V
Pin 2	Protected +24V
Pin 3	Protected +24V
Pin 4	0V
Pin 5	0V
Pin 6	0V
Pin 7	Cluster ID bit 0
Pin 8	Cluster ID bit 1
Pin 9	Cluster ID bit 2
Pin 10	Cluster ID bit 3
Pin 11	Router port ID bit 0
Pin 12	Router port ID bit 1
Pin 13	Router port ID bit 2
Pin 14	Nominal = NC, Redundant = 0V
Pin 15	Master/Server
Pin 16	Spare
Pin 17	Spare
Pin 18	Spare
Pin 19	Spare
Pin 20	Spare
Pin 21	Spare
Pin 22	Spare
Pin 23	Spare
Pin 24	Spare
Pin 25	Spare
Pin 26	Spare
Pin 27	Spare
Pin 28	Spare
Pin 29	Spare
Pin 30	Spare
Pin 31	Spare
Pin 32	Spare
Pin 33	Reserved
Pin 34	Reserved
Pin 35	Reserved
Pin 36	Reserved

Modular Architecture for Robust Computing (MARC) Project Status

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The MARC project

- This SpaceWire backplane presentation is based on work performed on the MARC (Modular Architecture for Robust Computation) project
- The objective of the MARC project is to design and develop a demonstration system with a HW distributed architecture based on a SpaceWire network as the communication medium
- The MARC project is currently in the software integration phase

MARC rack


SYSTEM RESET
PSU 1
MAINS
CURRENT
PSU 2
MAINS
CURRENT
ROUTER 1
ROUTER 2
ROUTER 3
ROUTER 4
SpW-EGSE
SpW-GCM
SpW-
S-E-A

MARC backplane