# HSSL development on DSM ST 65nm technology



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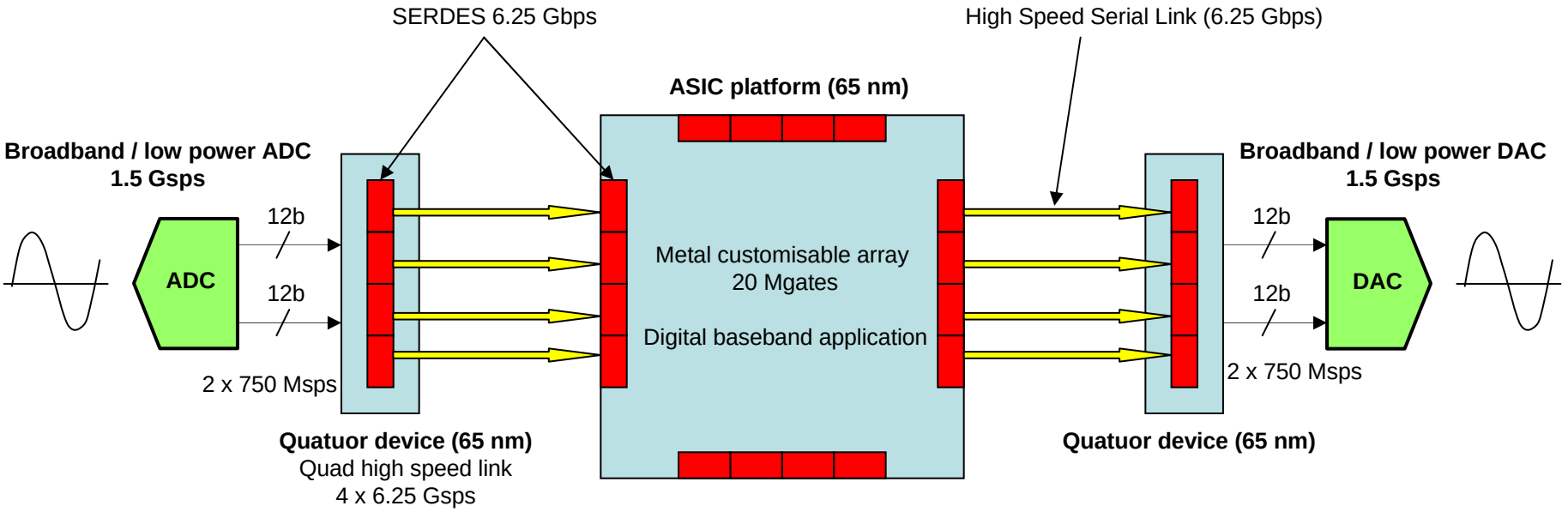
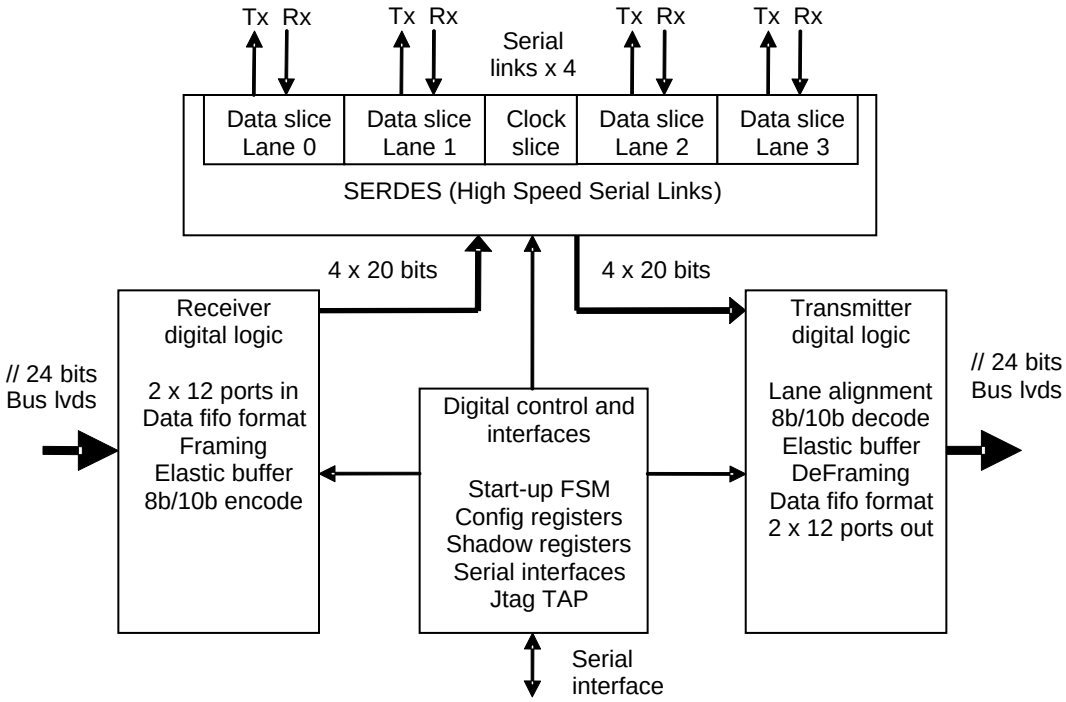
# *interfacing between ASIC platform and broadband ADC / DAC*



# Quatuor top level representation




- **1 data slice = 1 serializer (Rx) + 1 deserializer (Tx)**
- **1 data slice can either be configured in half or full duplex mode**
- **Quatuor = 4 serializers + 4 deserializers (8 CML buffers)**
- **Quatuor = 2 x 12 bits input ports (24 LVDS buffers)**
- **Quatuor = 2 x 12 bits output ports (24 LVDS buffers)**
- **One common clock slice (Data Ready) for the four data slices**
- **Each data slice can be activated / deactivated independently**
- **Aggregated data ranging from 6.25 Gbps (1 active lane) to 25 Gbps (4 active lanes)**

# *Quatuor basic specifications*

- **Tx mode (serializer / half duplex)**
  - **The 4 serializers (CML) can be independently switched on / off**
  - **Each 12 bits parallel input port (LVDS) can accommodate 8, 9, 10, 11 or 12bits**

- **Rx mode (deserializer / half duplex)**
  - **The 4 deserializers (CML) can be independently switched on / off**
  - **Each 12 bits parallel output port (LVDS) can accommodate 8, 9, 10, 11 or 12bits**

- **TxRx mode (SerDes / full duplex)**
  - **From the 4 lanes available ONLY 2 full duplex lanes (2 data slices) can be activated at the same time**
  - **In theory the device could also be configured with 4 full duplex lanes (25Gbps in Tx + 25Gbps in Rx) but due power limitations the full duplex mode is restricted to 2 full duplex active lanes at the same time**

# *Quatuor basic specifications*

- **2 external clocks required**
  - **REFCLK low jitter (Data Ready), reference choices at:**
    - **125 Mhz**
    - **156.25 Mhz**
    - **250 Mhz**
    - **312.5 Mhz**
  - **SMPCLK (Sampling Clock) for parallel interfaces with external devices**
    - **Min 150 Mhz (min data payload rate is 1.8 Gbps)**
    - **Max 1.5 Ghz**

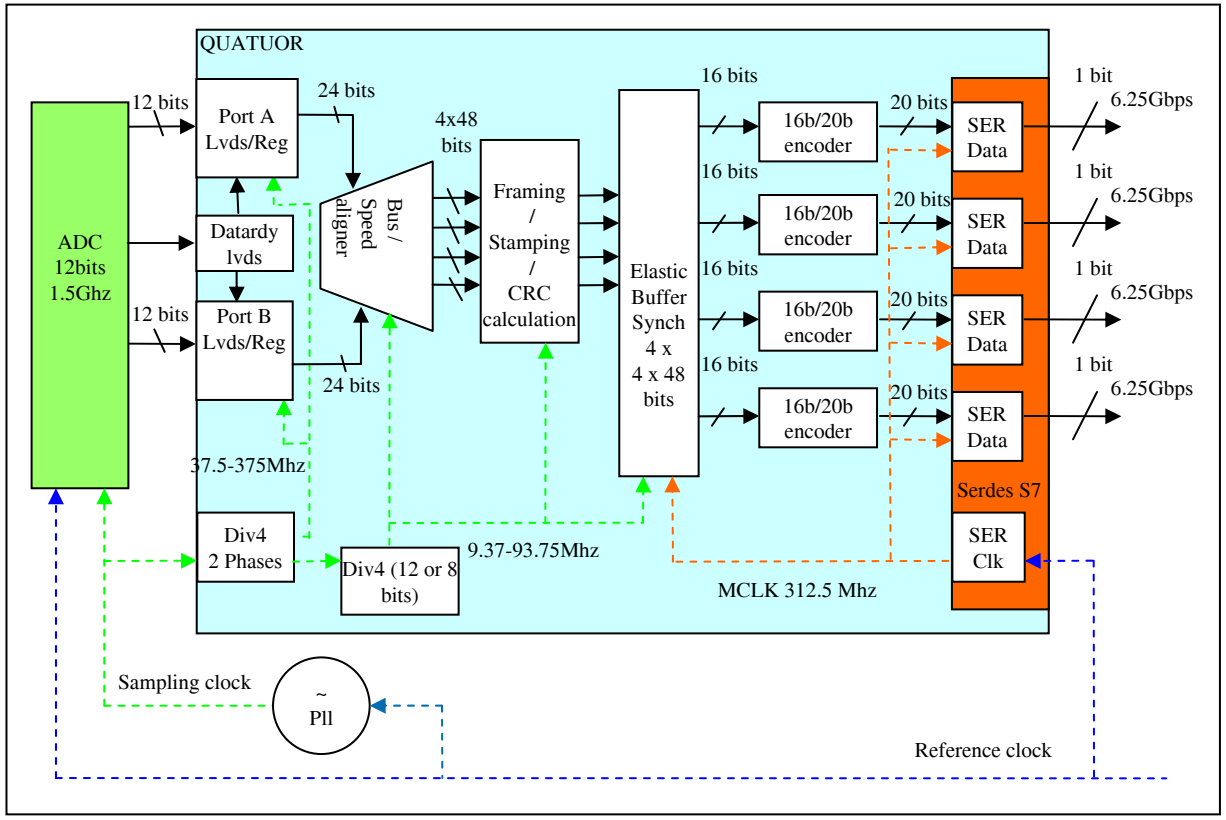
- **Multiple data rates elaborated from a unique internal 6.25 Ghz reference**
  - **Max data rate 4 active lanes in same direction:**
    - **25 Gbps Full data rate (Payload at 20Gb/s)**
  - **Min 1 data lanes activated out of 4:**
    - **3.125 Gbps Half data rate (Payload at 2.5Gbps)**

# *Quatuor data rates summary table*

| Fs max | Data Width | Fs Ratio | System clk | Active // LVDS ports | Payload before coding | Payload after coding | Aggregation Ratio | lane data rate (SerDes) |
|---|---|---|---|---|---|---|---|---|
| Mhz | Bits no | 48 bits | Mhz | Ports no | Gb/s | (8b10b)Gb/s | Port:Lane | Gb/s |
| 1500 | 12 | 16 | 93.75 | 2 | 18 | 22.5 | 1:1 | 25 |
| 1500 | 8 | 24 | 62.50 | 2 | 12 | 15 | 1:1 | 25 |
| 1200 | 8 | 24 | 50.00 | 2 | 9.6 | 12 | 2:1 | 12.5 |
| 750 | 12 | 16 | 46.88 | 2 | 9 | 11.25 | 2:1 | 12.5 |
| 312.5 | 10 | 16 | 19.53 | 2 | 6.25 | N/A | 2:1 | 6.25 |
| 375 | 12 | 16 | 23.44 | 2 | 4.5 | 5.625 | 4:1 | 6.25 |
| 300 | 8 | 24 | 12.50 | 2 | 2.4 | 3 | 2:1 | 6.25 |

**Space Fibre mode**
**Quatuor internal encoder bypassed**

# *Quatuor configured in Tx mode (half duplex)*
# *4 active Tx lanes / aggregated data rate 25 Gbps*




**aggregated data rate 25 Gbps (Tx)**

**4 Tx lanes ON**

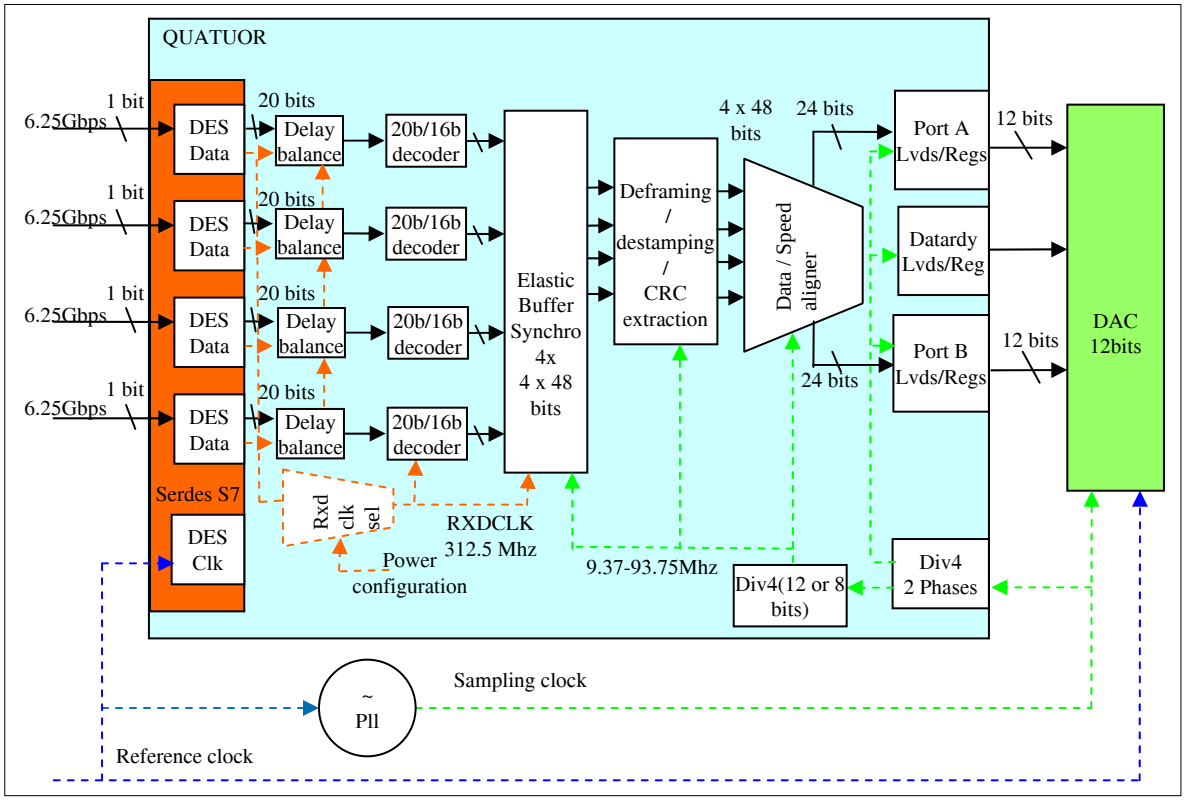
**4 Rx lanes OFF**

# *Quatuor configured in Rx mode (half duplex)*
# *4 active Rx lanes / aggregated data rate 25 Gbps*

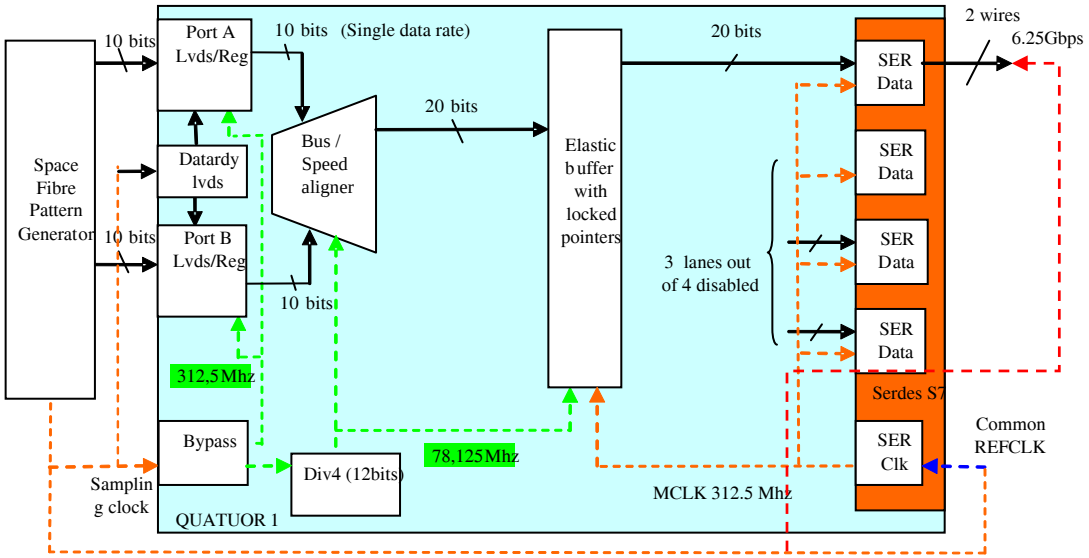
**aggregated data rate 25 Gbps (Rx)**

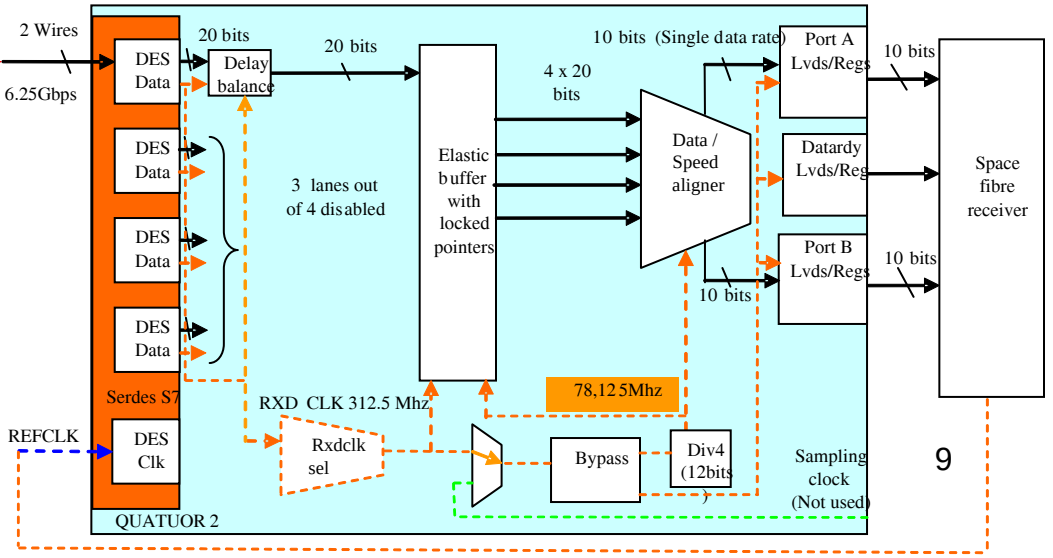
**4 Rx lanes ON**

**4 Tx lanes OFF**



# Quatuor configured in Space Fibre mode (Full duplex)
# 1 active lane only / data rate 6.25 Gbps



# Deep Submicron Roadmap