HSSL development on DSM ST 65nm technology
interfacing between ASIC platform and broadband ADC / DAC

- **ADC**
  - Broadband / low power ADC 1.5 Gsps
  - 2 x 750 Msps
  - 12b
  - Quad high speed link 4 x 6.25 Gsps

- **DAC**
  - Broadband / low power DAC 1.5 Gsps
  - 2 x 750 Msps
  - 12b

- **ASIC platform (65 nm)**
  - Metal customisable array 20 Mgates
  - Digital baseband application
  - SERDES 6.25 Gbps
  - High Speed Serial Link (6.25 Gbps)

- **Quatuor device (65 nm)**
  - Quad high speed link 4 x 6.25 Gsps
Quatuor top level representation

- 1 data slice = 1 serializer (Rx) + 1 deserializer (Tx)
- 1 data slice can either be configured in half or full duplex mode
- Quatuor = 4 serializers + 4 deserializers (8 CML buffers)
- Quatuor = 2 x 12 bits input ports (24 LVDS buffers)
- Quatuor = 2 x 12 bits output ports (24 LVDS buffers)
- One common clock slice (Data Ready) for the four data slices
- Each data slice can be activated / deactivated independently
- Aggregated data ranging from 6.25 Gbps (1 active lane) to 25 Gbps (4 active lanes)
Quatuor basic specifications

- **Tx mode (serializer / half duplex)**
  - The 4 serializers (CML) can be independently switched on / off
  - Each 12 bits parallel input port (LVDS) can accommodate 8, 9, 10, 11 or 12 bits

- **Rx mode (deserializer / half duplex)**
  - The 4 deserializers (CML) can be independently switched on / off
  - Each 12 bits parallel output port (LVDS) can accommodate 8, 9, 10, 11 or 12 bits

- **TxRx mode (SerDes / full duplex)**
  - From the 4 lanes available ONLY 2 full duplex lanes (2 data slices) can be activated at the same time
  - In theory the device could also be configured with 4 full duplex lanes (25Gbps in Tx + 25Gbps in Rx) but due power limitations the full duplex mode is restricted to 2 full duplex active lanes at the same time
Quatuor basic specifications

• 2 external clocks required
  – REFCLK low jitter (Data Ready), reference choices at:
    – 125 Mhz
    – 156.25 Mhz
    – 250 Mhz
    – 312.5 Mhz
  – SMPCLK (Sampling Clock) for parallel interfaces with external devices
    – Min 150 Mhz (min data payload rate is 1.8 Gbps)
    – Max 1.5 Ghz

• Multiple data rates elaborated from a unique internal 6.25 Ghz reference
  – Max data rate 4 active lanes in same direction:
    – 25 Gbps Full data rate (Payload at 20Gb/s)
  – Min 1 data lanes activated out of 4:
    – 3.125 Gbps Half data rate (Payload at 2.5Gbps)
**Quatuor data rates summary table**

<table>
<thead>
<tr>
<th>Fs max (Mhz)</th>
<th>Data Width</th>
<th>Fs Ratio</th>
<th>System clk (Mhz)</th>
<th>Active // LVDS ports</th>
<th>Payload before coding</th>
<th>Payload after coding</th>
<th>Aggregation Ratio</th>
<th>lane data rate (SerDes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1500</td>
<td>12</td>
<td>16</td>
<td>93.75</td>
<td>2</td>
<td>18</td>
<td>22.5</td>
<td>1:1</td>
<td>25</td>
</tr>
<tr>
<td>1500</td>
<td>8</td>
<td>24</td>
<td>62.50</td>
<td>2</td>
<td>12</td>
<td>15</td>
<td>1:1</td>
<td>25</td>
</tr>
<tr>
<td>1200</td>
<td>8</td>
<td>24</td>
<td>50.00</td>
<td>2</td>
<td>9.6</td>
<td>12</td>
<td>2:1</td>
<td>12.5</td>
</tr>
<tr>
<td>750</td>
<td>12</td>
<td>16</td>
<td>46.88</td>
<td>2</td>
<td>9</td>
<td>11.25</td>
<td>2:1</td>
<td>12.5</td>
</tr>
<tr>
<td>312.5</td>
<td>10</td>
<td>16</td>
<td>19.53</td>
<td>2</td>
<td>6.25</td>
<td>N/A</td>
<td>2:1</td>
<td>6.25</td>
</tr>
<tr>
<td>375</td>
<td>12</td>
<td>16</td>
<td>23.44</td>
<td>2</td>
<td>4.5</td>
<td>5.625</td>
<td>4:1</td>
<td>6.25</td>
</tr>
<tr>
<td>300</td>
<td>8</td>
<td>24</td>
<td>12.50</td>
<td>2</td>
<td>2.4</td>
<td>3</td>
<td>2:1</td>
<td>6.25</td>
</tr>
</tbody>
</table>

**Space Fibre mode**
**Quatuor internal encoder bypassed**
Quatuor configured in Tx mode (half duplex)
4 active Tx lanes / aggregated data rate 25 Gbps

aggregated data rate 25 Gbps (Tx)
4 Tx lanes ON
4 Rx lanes OFF
Quatuor configured in Rx mode (half duplex)
4 active Rx lanes / aggregated data rate 25 Gbps

aggregated data rate 25 Gbps (Rx)
4 Rx lanes ON
4 Tx lanes OFF
Quatuor configured in Space Fibre mode (Full duplex)
1 active lane only / data rate 6.25 Gbps
Deep Submicron Roadmap

- **Radiation Tests of ST 130/90/65 nm**
- **65nm evaluation / HSSL proto (phase 1)**
- **harden lib / test vehicle (phase 2)**
- **Qualification (phase 3)**
- **ADC (phase 1)**
- **ADC (phase 2)**
- **Qualification (phase 3)**
- **DAC (phase 1)**
- **DAC (phase 2)**
- **Qualification (phase 3)**
- **Advanced Packaging Development (flip chip)**

**Legend**
- Running / Approved Activities
- Activities approved by IPC but support from delegates still to be confirmed
- Activities not founded yet

**Dates:**
- 2006
- 2007
- 2008
- 2009
- 2010
- 2011
- 2012
- 2013
- 2014

**Timeline:**
- 24/02/2010

**Additional Notes:**
- Advanced Packaging Development (flip chip)

**Ready For Future OBP Payloads**