Plug and play over SpaceWire in RASTA systems

Overview

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Overview

- **Introduction to RASTA**
- **Current Plug and Play implementation**
- **Application of SpaceWire PnP**
- **Issues and differences to current implementation**

Background

Many software and hardware components developed in R&D activities do not reach required maturity level for use in space projects, due to lack of a representative environment for validation & demonstration.

The RASTA (Reference Avionics System Testbed Activity) aims to fill this gap by providing a standard hardware and software infrastructure to integrate R&D activity results.

The RASTA objectives are to:

- **allow new technology to be validated in flight representative environment,**
- **support mission and spacecraft design,**
- **support on-board software verification and validation through the project life-cycle by means of a coherent emulations platform,**
- **maximize reuse of the existing avionics technologies and to be scalable.**

Info was obtained from Aeroflex Gaisler (www.gaisler.com)

Hardware concept

RASTA development platform is today based on the Compact PCI (cPCI) bus. Communication between boards is performed via the PCI bus in the backplane.

For other protocols, such as SpaceWire and Mil-Std-1553B, connectors are provided on the front-panel of each board.

The trend is to use less the PCI and more the SpaceWire interfaces on the front-panels. Future RASTA systems will probably use an active or a passive SpaceWire backplane.

RASTA comprises processor and interface boards, and in the future also SpaceWire router boards. Standard parts are used for processors such as UT699, but also FPGA boards are used to allow new functions to be incorporated.

Software concept

The on-board software and tools developed or adapted for RASTA are part of a complete set of layers and libraries allowing the integration of embedded real-time applications independently from the actual operating system used for the RASTA environment, with minimum modification.

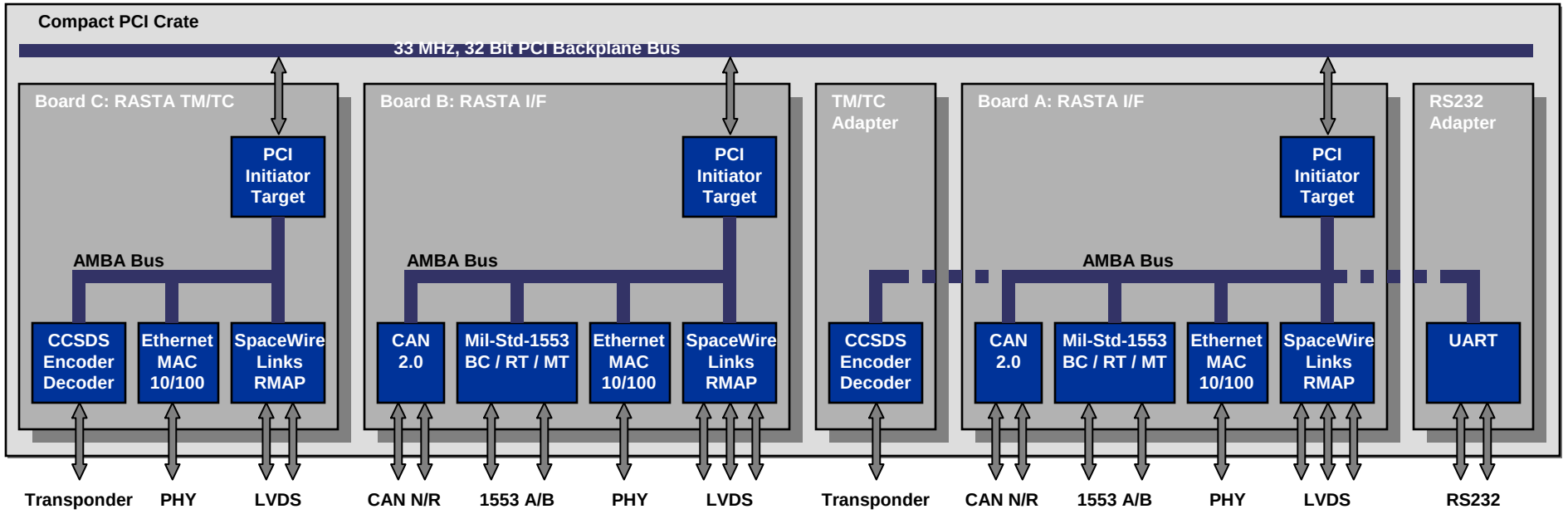
Baseline operating system is open source RTEMS 4.10, but also VxWorks 6.5 is supported. To communicate with interface boards, device drivers are provided that execute on any LEON3 processor, e.g. UT699.

RTEMS has been extended with a Plug&Play capability to detect installed boards, including any IP cores residing inside the FPGA/ASIC devices on these boards.

General CPCI crate configuration

A compact PCI crate with Xilinx based development boards can be used to emulate different designs featuring LEON3 and LEON4 processors.

The architecture features communication via the backplane PCI bus, or via the SpaceWire links on the front-panels.



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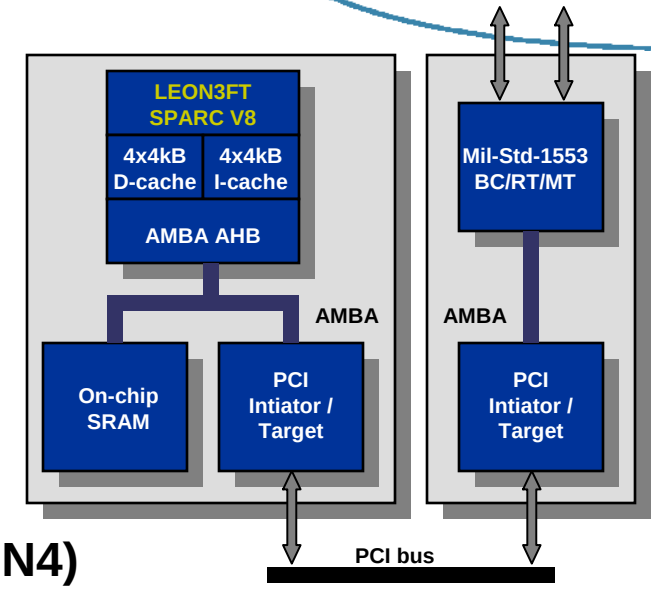
RTEMS PCI and SpaceWire support

PCI support
- Configuration space access
- Auto configuration library (PCI Plug&Play)
- Shared interrupt management
- Address translation

PCI host drivers
- GRPCI core (e.g. UT699)
- PCIF core (Actel RTAX2000S/AX2000)
- Synopsys PCI core (e.g. AT697)

SpaceWire RMAP drivers
- GRSPW / GRSPW2 (UT699, LEON3FT-RTAX, LEON4)
- RMAP initiator software stack
- Auto configuration library(not Plug&Play)

PCI / SpaceWire board drivers
- GR-RASTA-I/F, GR-RASTA-TM/TC, GR-RASTA-ADC/DAC
- GR701A Companion Chip, GR703 CCSDS TM/TC Chip



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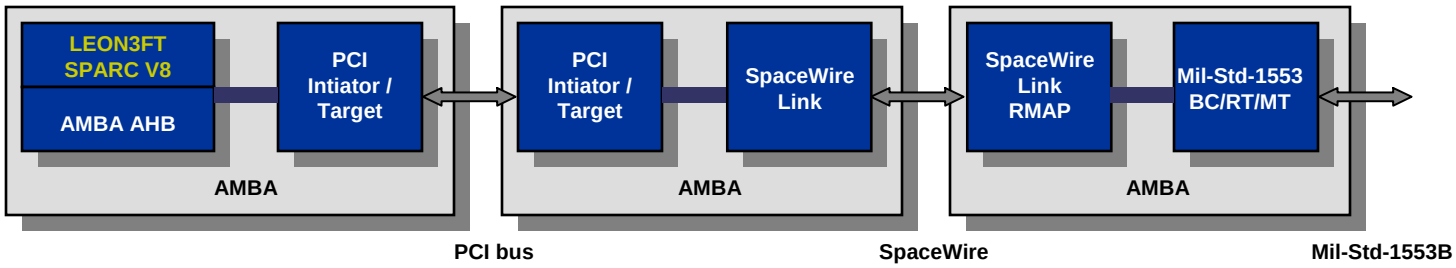
RTEMS current Plug & Play capability

RASTA RTEMS supports multi-level plug&play discovery: AMBA bus, PCI bus, SpaceWire link

- Initial scanning of on-chip AMBA bus is performed
- RTEMS drivers are registered for detected IP cores
- If a PCI interface is found, PCI bus is scanned and configured
- If a known peripheral PCI board is found, with AMBA plug&play indication, the AMBA bus of the peripheral device is scanned
- RTEMS drivers are registered for detected IP cores on PCI board
- If a SpW interface is found, optional RMAP initiator stack is loaded
- If the SpW link is active, optional scanning for remote RMAP targets is performed on the SpaceWire network. Addresses known in advance.
- If a known peripheral SpW board is found, with AMBA plug&play indication, the AMBA bus of the peripheral device is scanned
- RTEMS drivers are registered for detected IP cores on SpW board



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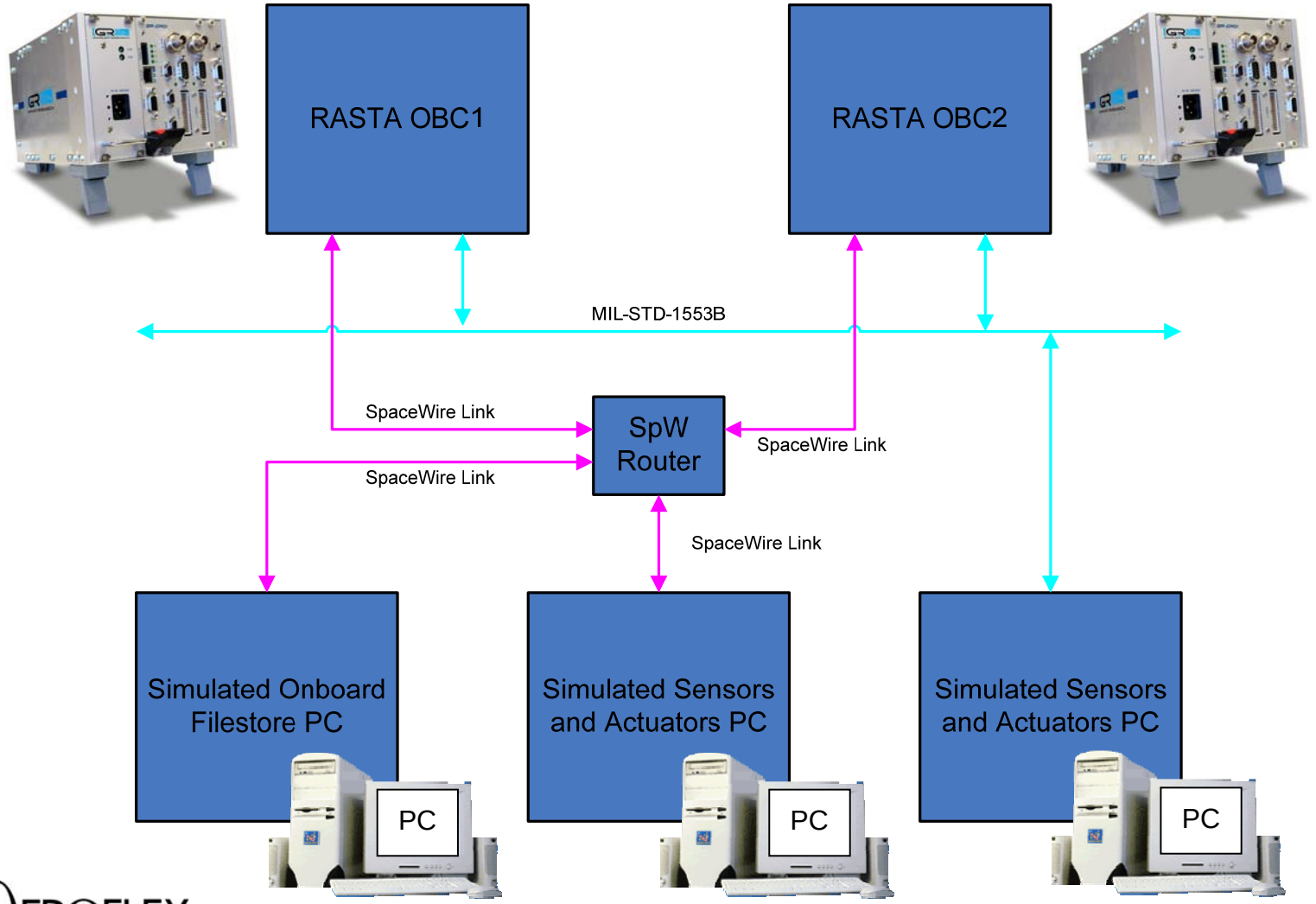
Example of deployed RASTA system



Info was obtained from CCSDS SOIS Spring 2009 Meeting (ccsds.org)

RTEMS future Plug & Play capability

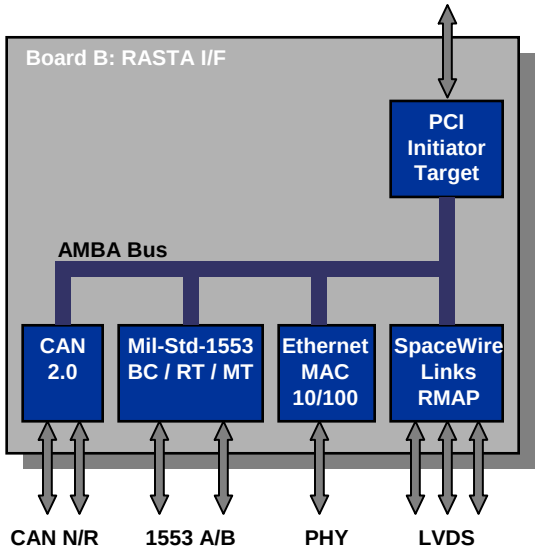
RASTA RTEMS supports multi-level plug&play discovery: AMBA bus, PCI bus, SpaceWire link

- **Initial scanning of on-chip AMBA bus is performed**
- **RTEMS drivers are registered for detected IP cores**
- **If a PCI interface is found, PCI bus is scanned and configured**
- **If a known peripheral PCI board is found, with AMBA plug&play indication, the AMBA bus of the peripheral device is scanned**
- **RTEMS drivers are registered for detected IP cores on PCI board**
- **If a SpW interface is found, optional SpWPnP initiator stack (similar to RMAP) is loaded**
- **Start a breadth first traversal of the network. No addresses known in advance.**
- **If a known peripheral SpW board is found identified by the SpW Vendor and Device ID the AMBA bus of the peripheral device is scanned.**
- **RTEMS drivers are registered for detected IP cores on SpW board**

Issues and differences to PCI plug and play

Multiple SpW nodes in a system:

- In contrast to PCI systems it is common to have several ports in a single system (node).
- This causes several paths being available to the same node.
- Software must be able to determine that a found node is the same that its own or has already been found before.
- Use network ID.
- Network ID should be node specific while DLA should be port specific.



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Issues and differences to PCI plug and play

Addresses not known:

- **Current RASTA SpW initator stack has a predetermined list of SpW addresses to scan.**
- **In PnP version nodes and routers should be discoverable without knowing the address.**
- **Use path addressing and configuration port at address 0?**
- **Use default address 254?**

Issues and differences to PCI plug and play

Stuck links:

- RASTA systems enable IP cores such as UARTS and Ethernet MACs to be accessible over SpaceWire and PCI.
- PCI has an upper limit on the completion time of an access.
- The same does not apply for SpaceWire causing the possibility for one device to hang all devices on a remote system.
- Watchdog timer available for routers but redundant links are still needed to continue operation before the hanging device is ready again.
- Software transparency needed when using the redundant links.
- Group adaptive routing
- SpW-RT?

Issues and differences to PCI plug and play

Interrupt routing:

- PCI bus has dedicated interrupt routing which allows device drivers to use the interrupt driven mode also when accessing the device over PCI.
- Shared interrupts used over PCI.
- Currently polling mode is used over SpaceWire.
- No support for irq routing over SpaceWire with or without PnP extension.

Hot plugging?

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