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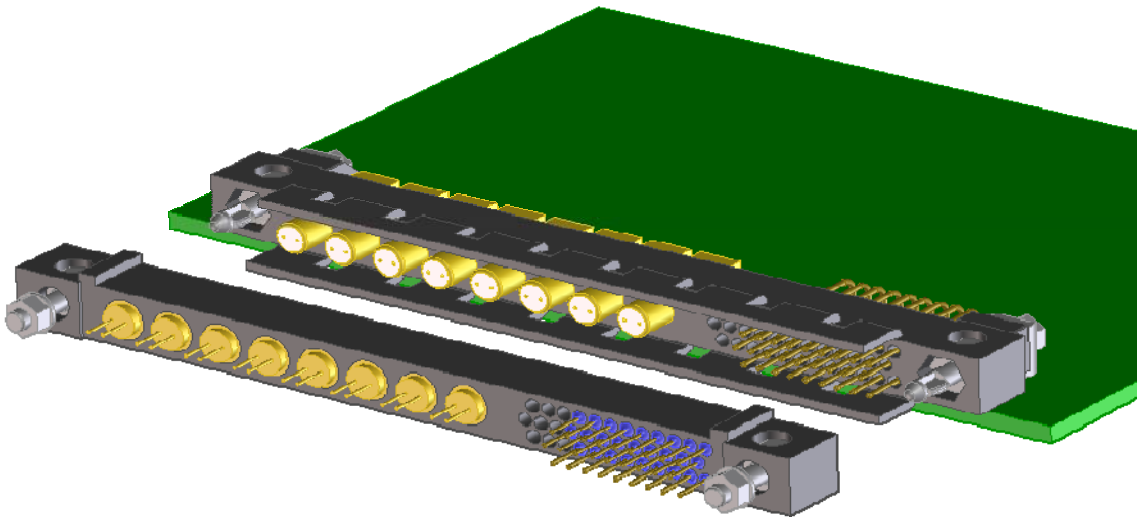
TABLE OF CONTENTS



21

Figures

Tables

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1 INTRODUCTION

The purpose of this document is to specify a SpaceWire Active Backplane SpWAB. The specification covers the power distribution architecture, network architecture and the electrical interfaces to the backplane.

The architecture has been derived from the ESA funded mini-project Modular Architecture for Robust Computing (MARC) that has been performed by SEA, SciSys and Astrium UK.

1.1 APPLICABLE DOCUMENTS

[AD1] SpaceWire standard…

[AD2] SpaceWire protocols….

1.2 REFERENCE DOCUMENTS

[RD1] Atmel 8 Port SpaceWire Router user manual …

1.3 ABBREVIATIONS AND ACRONYMS

The following list of abbreviations and acronyms are pertinent to this document.

AD	Applicable Document
CCM	Core Computing Module
CCSDS	Consultative Committee for Space Data Systems
CHRC	Core Hardware Reconfiguration Controller
CUC	CCSCS Unsegmented Code (this is a time code format)
ECSS	European Co-operation for Space Standardisation
EGSE	Electrical Ground System Equipment
ESA	European Space Agency
FDIR	Fault Detection Isolation and Recovery
IO	Input Output
MARC	Modular Architecture for Robust Computing
Mbps	10^6 bits per second
MET	Mission Elapsed Time (SOIS terminology)
NA	Not Applicable
PCB	Printed Circuit Board
PSU	Power Supply Unit
RMAP	Remote Memory Access Protocol (ECSS-E-50-12)
SCET	SpaceCraft Elapsed Time
TCC	Time Code Count (the 6 bit time value in the SpaceWire Time-Code)
TCM	Time Code Manager

2 ACTIVE BACKPLANE OVERVIEW

2.1.1 Overview

The SpaceWire Active Backplane (SpWAB) is intended to be contained within an electronics unit within a Spacecraft. The electronics unit is anticipated to handle both platform and payload processing tasks within the Spacecraft.

The SpWAB permits a decentralised architecture based on a SpaceWire network as a communication medium. It is anticipated that this decentralised architecture will simplify resource sharing (e.g. communication network, memory, etc.) among payload and platform modules.

The context of the backplane (green area) described in this document is shown in Figure 2-1.

Power is supplied to the SpWAB and the Modules that are plugged into the backplane from Nominal and Redundant Power Supplies (PSUs).

The Backplane architecture can support any number of modules to the limit of the SpaceWire address space.

The backplane supports Nominal and Redundant TMTC Modules that contain Core Hardware Reconfiguration Controllers (CHRCs). It is the responsibility of the CHRC to handle the highest level of reconfiguration, in particular the CHRC provides autonomous power switching that is triggered by a system watchdog.

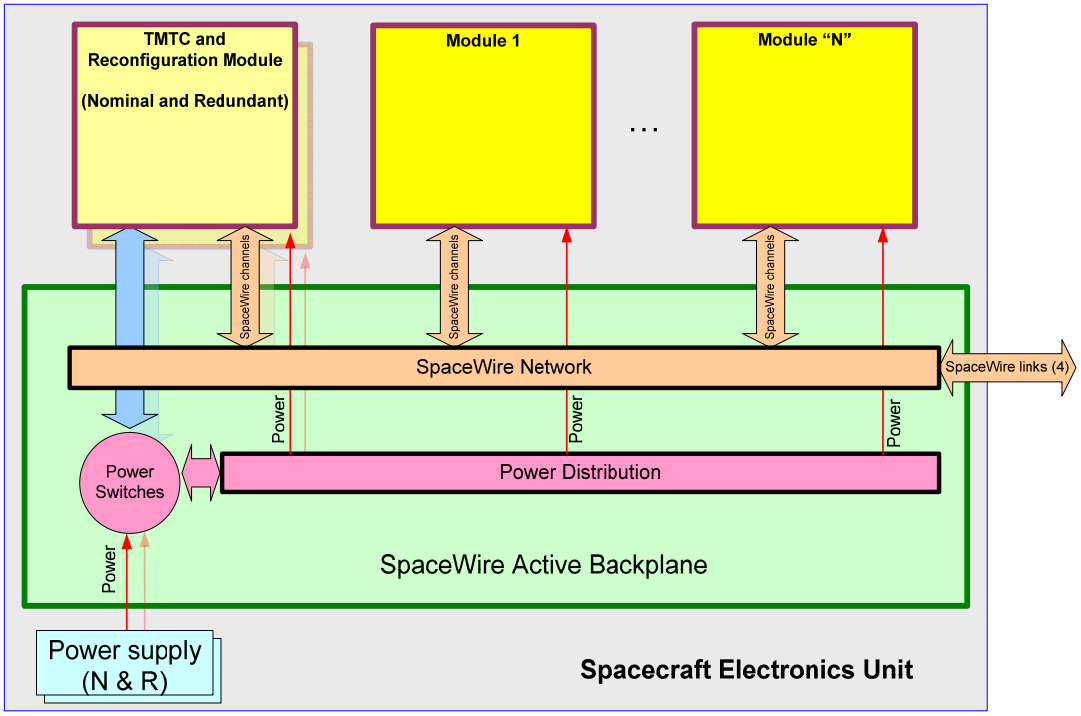

Figure 2-1 : SpWAB context within an example Spacecraft Electronics Unit

3 SPACEWIRE NETWORK SPECIFICATION

3.1 MODULE CONNECTIONS

Each module connected to the backplane is attached to the SpaceWire network via 2 SpaceWire ports. The ports on the Module shall be numbered 1 and 2.

The cluster architecture of the backplane (and design of the module) shall allow:

- full functionality of a module when one of the SpaceWire ports to the network fails.
- full functionality of a module when one of the SpaceWire routers in the network fails.

The Module shall be compatible with the RMAP protocol for monitoring and control. It shall be possible to read back all RMAP accessible control registers.

Where practical each control function shall be located at a different address so that the masking/ORing of bits is not required.

The Module shall be compatible with SpaceWire protocols [AD1] and [AD2].

The Module shall be able to provide packets that use path or logical addressing.

A module may have further interfaces, for example at the front panel, however these are not routed via the backplane.

3.2 CLUSTER NETWORK ARCHITECTURE

The modular network building block shown in Figure 3-1 is used for the backplane network. This building block is called a "Cluster". The Modules within the cluster adopt Module numbers based on the Router ports that they connect to, for example Module 1 connects to port 1 on Router 1 and port 1 Router 2.

Each module shall be referenced by a combination of the Module number and the Cluster number. Thus Module 1C2 is Module 1 within Cluster 2. Using this identification method means that the network paths to any module can be deduced simply.

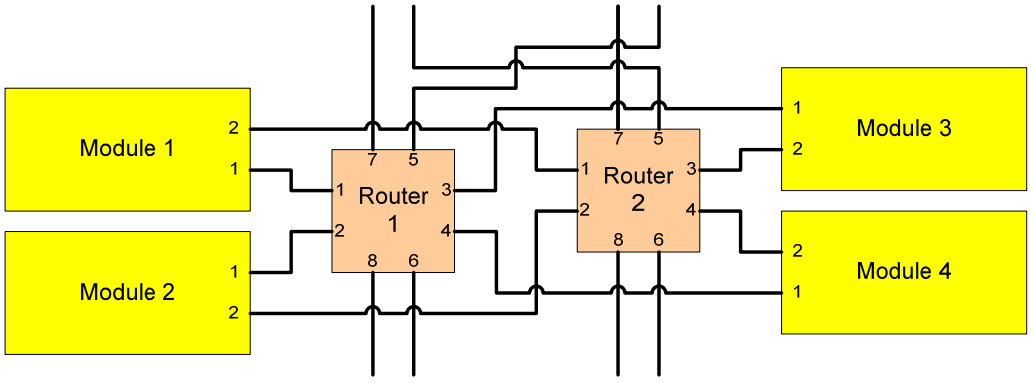

Figure 3-1 : Network Cluster comprising 2 Routers and 4 Modules

The minimum backplane incorporates 2 Clusters as shown in Figure 3-2.

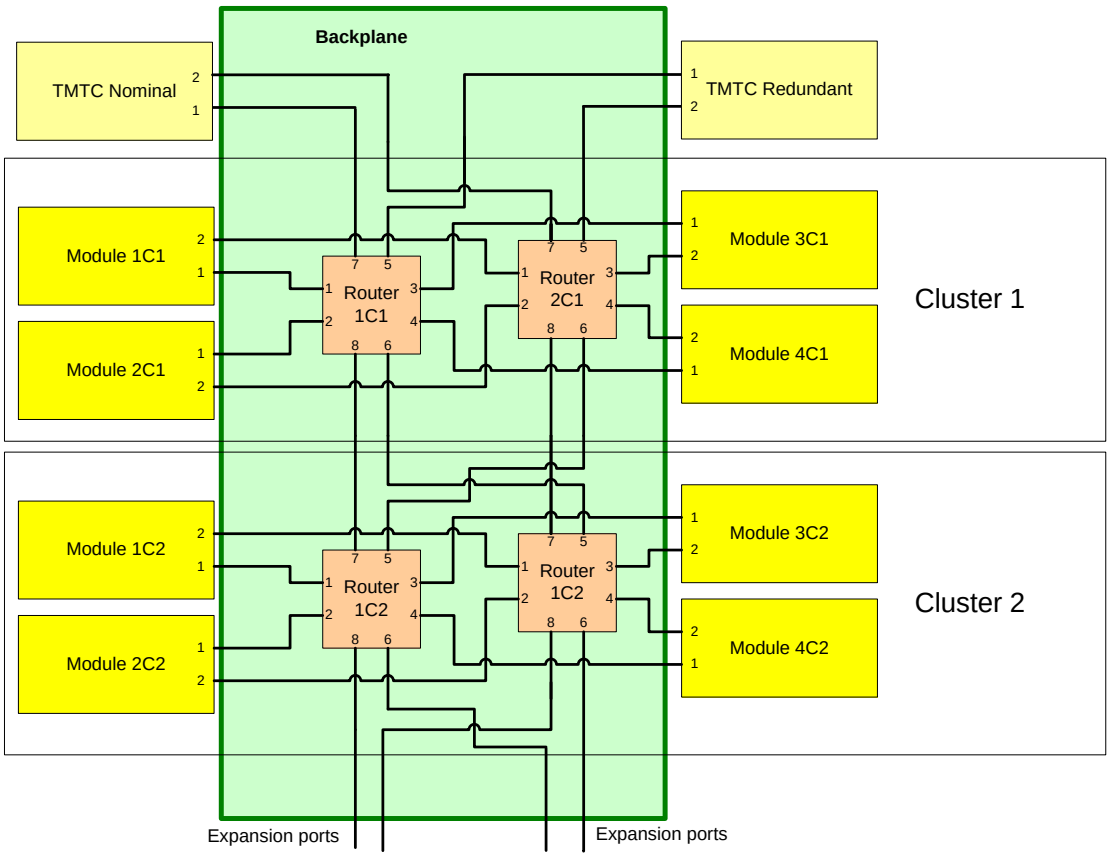

Figure 3-2 : MARC Backplane Connection Architecture

3.2.1 SpaceWire Ports

Standard FR4 material may be used at frequencies up to 2GHz and can therefore accommodate the edge speeds (~1ns) present in a 200Mbps SpaceWire link. The routing of SpaceWire signals at 200Mbps through PCBs, vias, connectors and cables is non-trivial since impedance discontinuities must be minimised. The backplane design must therefore ensure:

- Controlled impedance backplane connectors are employed that have an impedance of 100 ohms and have shielded pairs of pins for differential signals which operate at frequencies of at least 1GHz.
- The path lengths of the SpaceWire signals within each point to point link though the PCB, connector and backplane are matched for electrical length to avoid introducing skew that closes the eye diagram.
- The number of through vias is minimised.

3.3 SPACEWIRE NETWORK ROUTERS

The SpWAB connection architecture shown in Figure 3-2 utilises four 8-port routers to create an active backplane. These are ATMEL AT7910E 8 port SpaceWire Routers.

There are eight SpaceWire ports, two external parallel ports and an internal configuration port in the SpaceWire router. A low latency, worm-hole routing, non-blocking, crossbar switch enables packets arriving at any SpaceWire port, external port or generated in the configuration port to be directed out of any other SpaceWire or external port, or to be routed to the configuration port.

The external ports (input FIFO and output FIFO) are unused in the SpWAB. The time-code port is also unused.

Each SpaceWire router is configured using its configuration port which is accessible via RMAP command to any of its SpaceWire ports. It contains registers which control the operation of the SpaceWire ports, external ports and the crossbar switch. The configuration port holds status registers for the various SpW ports and the crossbar switch. These registers can be read using a configuration read command to determine the status of the router and to access error information. Status and error information can also be selected for output on several status pins. The routing table is accessed via the configuration port. The logical address port mappings and priority bits can be set in the routing table. The routing table is used to control group adaptive routing and priority arbitration in the crossbar switch.

The data rate of the SpaceWire link interfaces ranges from 2 to 200 Mbit/s. The requirement for the SpWAB is to operate at up to 200 Mbit/s.

3.3.1 Input Failsafe

The receiver inputs of the SpaceWire Router do not have internal failsafe biasing. For failsafe biasing external high value resistors shall be incorporated.

The IN+ line shall be pulled up to 3V3 with 20kΩ and the IN− line is pulled to GND with 12kΩ as recommended by the SpaceWire Router User Manual [RD1].

This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.

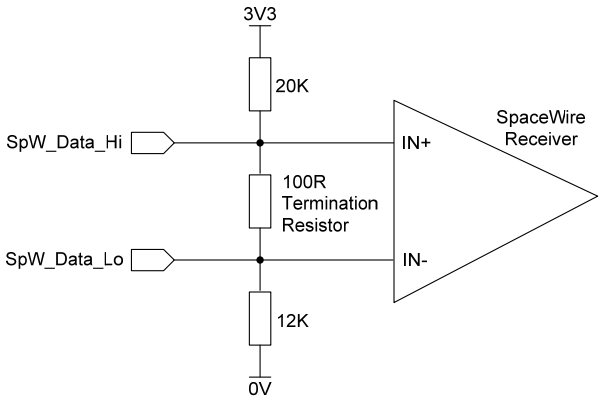

Figure 3-3 : Failsafe Biasing of Router Inputs

3.3.2 Router Clock

The routers on the backplane must be designed as stand alone functions, with aim of preventing single point failures within the design. As a consequence each router shall have its own dedicated 30MHz clock.

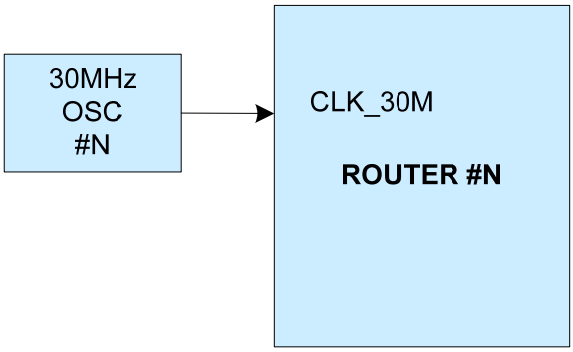

Figure 3-4 : Clock Distribution on Backplane

3.3.3 Router Power

The backplane routers require a 3V3 voltage rail. Each backplane router shall be provided with a separate 3V3 voltage rail with aim of preventing single point failures within the design.

The 3V3 voltage rail is shall be protected against over-voltage to prevent failure propagation through the router ports.

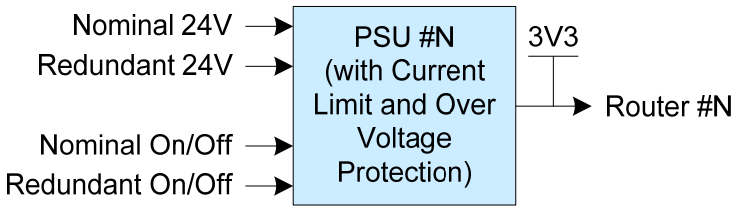

Figure 3-5 : Router PSU Topology

The PSU shall have Nominal and Redundant input power feeds and shall prevent fault propagation between the two power lines.

The PSU shall have Nominal and Redundant inputs for On/Off control. A failure of one input shall not prevent the operation of the other input.

3.3.4 Reset Generation

Each router shall have a reset line that is active for a period of at least 10ms after the router power rail has risen to within the router supply rail limits.

No Router reset lines shall be common with any other Router.

4 MODULE POWER DISTRIBUTION SPECIFICATION

Power to the Modules shall be provided by the backplane.

The backplane power system shall be designed to prevent failure propagation of an overcurrent between modules by using latching current limiters as shown in Figure 4-1.

The power distribution on the backplane shall be redundant with two power supplies each providing 24V. These are called 24V Nominal and 24V Redundant and shall be routed separately on the backplane to avoid fault propagation between the rails.

The supplies shall be diode consolidated at the power interface of each module (see Figure 4-2).

Each Power Supplies shall be capable of delivering 100W of power.

Power switches shall be incorporated into the backplane so that power to each Module can be controlled independently of other Routers and Modules on the network. The CHRC on either of the TMTC Modules shall control the power switches.

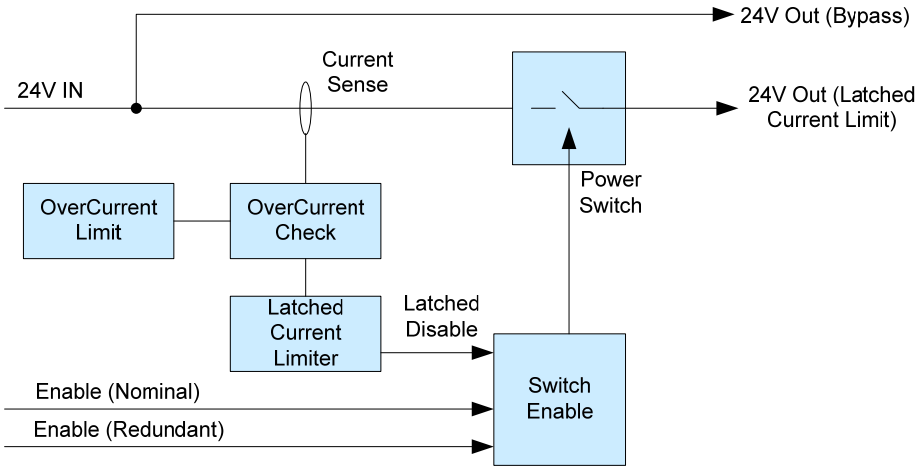

Figure 4-1 : Latching Current Limiter Block Diagram

The power distribution architecture is shown in Figure 4-2.

The TMTC module controls all power switches.

The TMTC module has a current limit bypass connection so that the module may incorporate a controller to switch on/off part of the TMTC circuitry. The TMTC shall ensure that failures cannot propagate to the backplane power supply via this bypass connection.

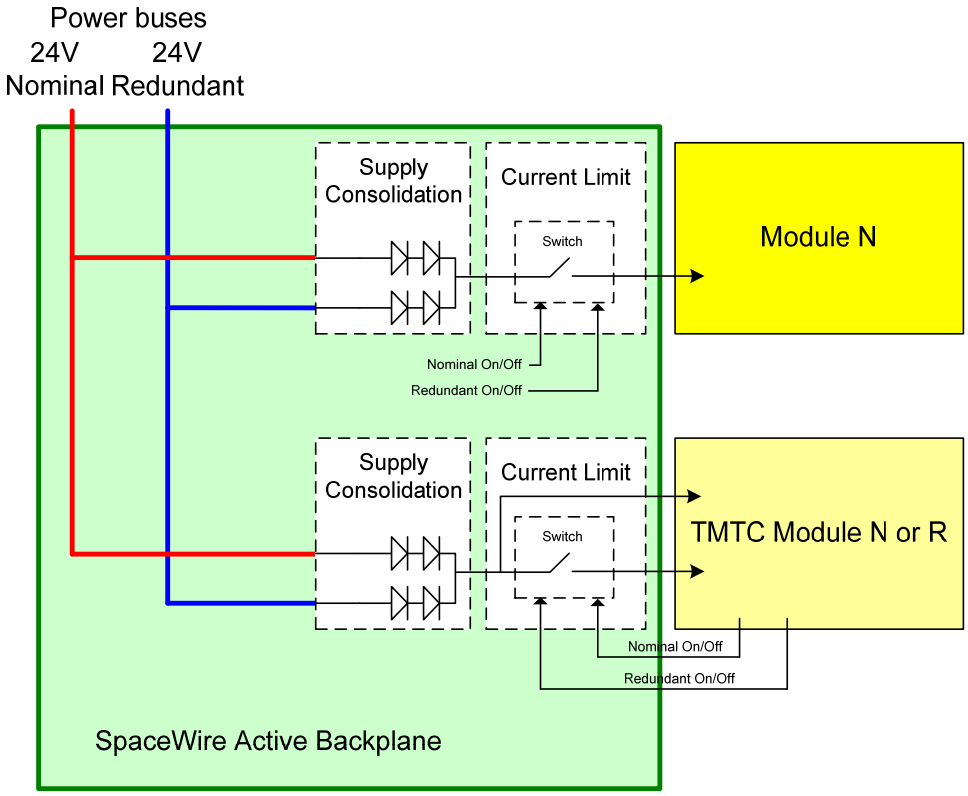

Figure 4-2 : Power Distribution and Control Architecture

5 CONNECTOR INTERFACE SPECIFICATION

The interface between the Module and the backplane is via a connector.

The connector provides the power and SpaceWire connections to the backplane.

5.1 BACKPLANE CONNECTOR

Hypertac HPH-XX connectors shall be used for backplane interface to the modules.

This connector incorporates 8 Twinax contacts that have been designed specifically for high-speed differential applications and are capable of supporting data rates up to 1 Gb/s.

The Twinax connections provide pairs of pins with dedicated ground shields allowing screened differential pairs to be routed through the connector. The Twinax contacts are 50 ohms controlled impedance per line giving 100 ohms differential impedance as required by SpaceWire.

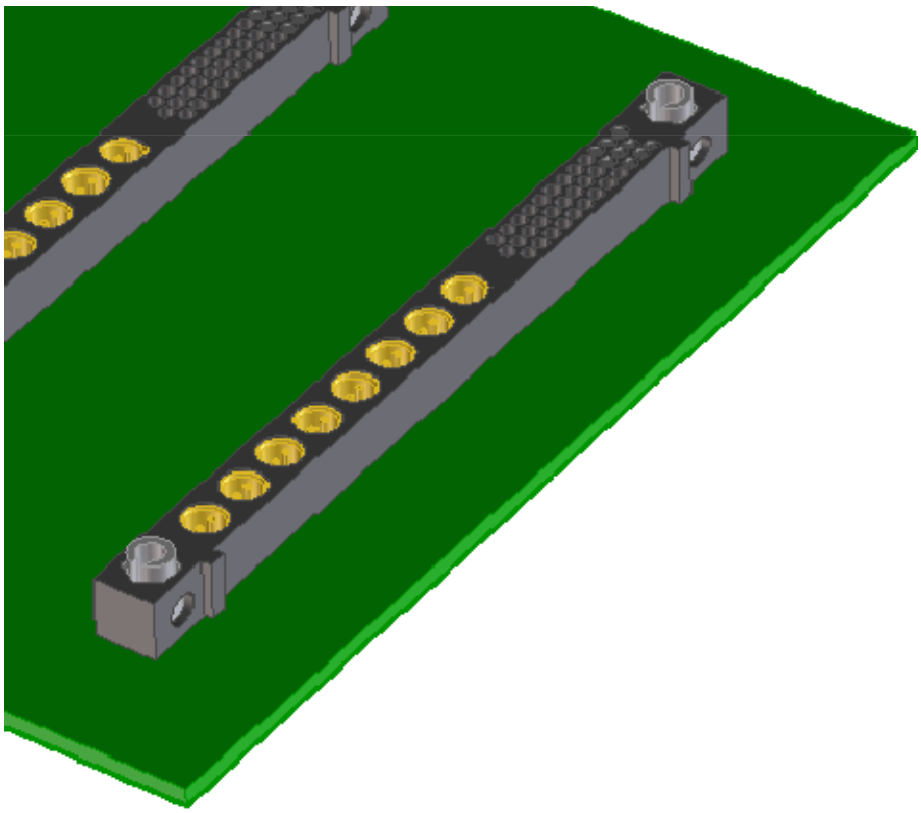

Figure 5-1 : Backplane Connector

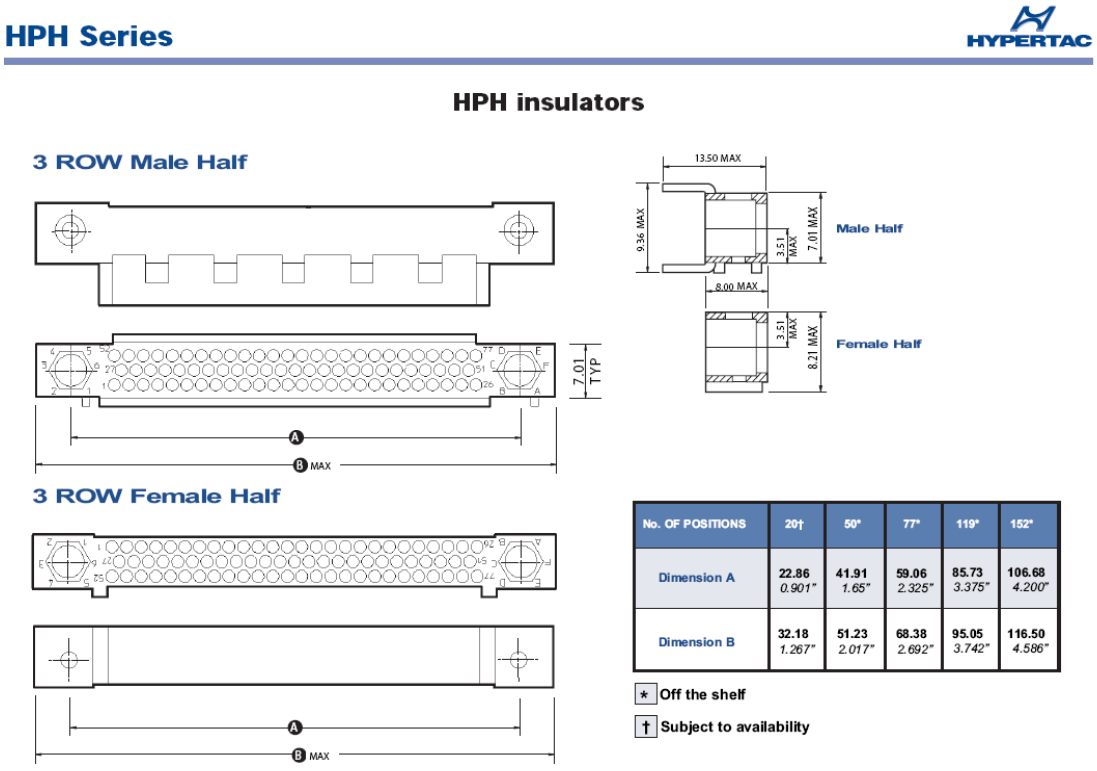

Table 5-1 : Backplane Connector Dimensions (as per 119 positions in table)

5.2 MODULE CONNECTOR

Hypertac HPH-XX connectors shall be used for module interface to the backplane.

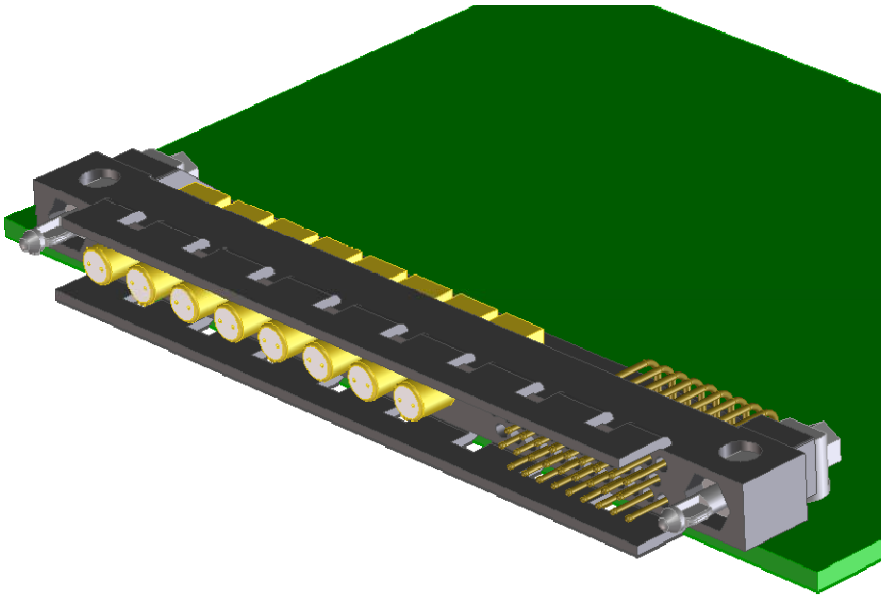

Figure 5-2 : Module Connector

5.3 MODULE CONNECTOR POLARISATION

The Hypertac HPH-XX connectors provide 2 polarisation pins. Each pin has 6 positions.
Polarisation pin 1 has 6 positions referenced as A to E
Polarisation pin 1 has 6 positions referenced as 1 to 6
The module polarisations shall be:

TMTC Nominal: A1
TMTC Redundant: A2
Module 1C1: B1
Module 2C1: B2
Module 3C1: B3
Module 4C1: B4
Module 1C2: C1
Module 2C2: C2
Module 3C2: C3
Module 4C2: C4

5.4 MODULE CONNECTOR PIN OUT

This connector incorporates 8 Twinax contacts that have been designed specifically for high-speed differential applications and are capable of supporting data rates up to 1 Gb/s.

In addition to high speed impedance controlled contacts the connector contains 36 signal and power pins.

All modules have the same pin-out for this connector. The pin out for the backplane signal interconnect is shown in Table 5-1.

Signal names are with relation to the router i.e. SPW_P1_Data_In is SpaceWire Data path to the Data Input Port 1 of the SpaceWire router. A module would therefore connect its Data output port to this signal.

TwinAx Pin	Signal
TA1 Pin 1	SPW 1 DATA IN +
TA 1 Pin 2	SPW 1 DATA IN -
TA 2 Pin 1	SPW 1 STRB IN +
TA 2 Pin 2	SPW 1 STRB IN -
TA 3 Pin 1	SPW 1 DATA OUT +
TA 3 Pin 2	SPW 1 DATA OUT -
TA 4 Pin 1	SPW 1 STRB OUT +
TA 4 Pin 2	SPW 1 STRB OUT -
TA 5 Pin 1	SPW 2 DATA IN +
TA 5 Pin 2	SPW 2 DATA IN -
TA 6 Pin 1	SPW 2 STRB IN +
TA 6 Pin 2	SPW 2 STRB IN -
TA 7 Pin 1	SPW 2 DATA OUT +
TA 7 Pin 2	SPW 2 DATA OUT -
TA 8 Pin 1	SPW 2 STRB OUT +
TA 8 Pin 2	SPW 2 STRB OUT -

Table 5-2 : Backplane SpaceWire Twinax pin-out

Pin	Signal
Pin 1	Protected +24V
Pin 2	Protected +24V
Pin 3	Protected +24V
Pin 4	0V
Pin 5	0V
Pin 6	0V
Pin 7	Module 1 On
Pin 8	Module 1 Off
Pin 9	Module 2 On
Pin 10	Module 2 Off
Pin 11	Module 3 On
Pin 12	Module 3 Off
Pin 13	Module 4 On
Pin 14	Module 4 Off
Pin 15	Module 5 On
Pin 16	Module 5 Off
Pin 17	Module 6 On
Pin 18	Module 6 Off
Pin 19	Module 7 On
Pin 20	Module 7 Off
Pin 21	Module 8 On
Pin 22	Module 8 Off
Pin 23	Router 1 On
Pin 24	Router 1 Off
Pin 25	Router 2 On
Pin 26	Router 2 Off
Pin 27	Router 3 On
Pin 28	Router 3 Off
Pin 29	Router 4 On
Pin 30	Router 4 Off
Pin 31	TMTC On

Pin 32	TMTC Off
Pin 33	0V
Pin 34	Direct 24V
Pin 35	0V
Pin 36	Direct 24V

Table 5-3 : TMTC Module Backplane signal pin-out

Pin	Signal
Pin 1	Protected +24V
Pin 2	Protected +24V
Pin 3	Protected +24V
Pin 4	0V
Pin 5	0V
Pin 6	0V
Pin 7	Cluster ID bit 0
Pin 8	Cluster ID bit 1
Pin 9	Cluster ID bit 2
Pin 10	Cluster ID bit 3
Pin 11	Router port ID bit 0
Pin 12	Router port ID bit 1
Pin 13	Router port ID bit 2
Pin 14	Nominal = NC, Redundant = 0V
Pin 15	Master/Server
Pin 16	Spare
Pin 17	Spare
Pin 18	Spare
Pin 19	Spare
Pin 20	Spare
Pin 21	Spare
Pin 22	Spare
Pin 23	Spare
Pin 24	Spare
Pin 25	Spare
Pin 26	Spare
Pin 27	Spare
Pin 28	Spare
Pin 29	Spare
Pin 30	Spare
Pin 31	Spare
Pin 32	Spare
Pin 33	Reserved

Pin 34	Reserved
Pin 35	Reserved
Pin 36	Reserved

Table 5-4 : Module Backplane signal pin-out

5.4.1 Backplane Interconnect to PSU

D-Sub Mixed Layout plug connectors shall be used to connect the backplane to the PSUs.

The connectors are 9W4 configuration which contains 5 off signal pins rated at 5A and 4 power pins rated at 40A.

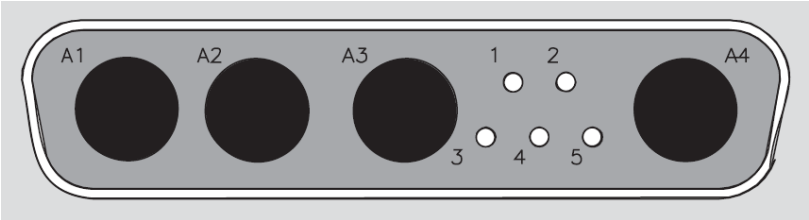

Figure 5-3 : 9W4 D-Sub Mixed Layout Connectors

Two 9W4 connectors shall be used – one per PSU.

The pin out for both 9W4 connectors shall be the same.

The pin out shall be as shown in Table 5-5 below.

Pin	Signal
Pin A1	PSU Output +24V
Pin A2	PSU Output +24V
Pin A3	PSU Output 0V
Pin 1	PSU Output +24V Sense
Pin 2	PSU Output +0V Sense
Pin 3	Spare
Pin 4	Spare
Pin 5	Sapre
Pin A2	PSU Output 0V

Table 5-5 : Pin-Out of Backplane to PSU/PSU Control Panel Connectors

5.4.2 External SpaceWire interfaces

The last cluster in the chain has 4 SpaceWire interfaces. These shall connect to individual connectors wired in accordance with the ECSS-E-50-12A Spacewire standard. Thus connector shall be a nine contact micro-miniature D-type as defined in ESCC 3401/071.

The pin out for the backplane interconnects is shown for reference in Table 5-6 below.

Pin	Signal	Pin	Signal
Pin 1	SPW DATA IN +	Pin 6	SPW DATA IN -
Pin 2	SPW STRB IN +	Pin 7	SPW STRB IN -
Pin 3	SHIELD	Pin 8	SPW STRB OUT +
Pin 4	SPW STRB OUT -	Pin 9	SPW DATA OUT +
Pin 5	SPW DATA OUT -		

Table 5-6 : Backplane External SpaceWire Connectors

5.5 MECHANICAL DESIGN

A suggested mechanical configuration for the backplane and the interfaces is shown in Figure 5-4.

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Figure 5-4 : Overall Backplane Layout

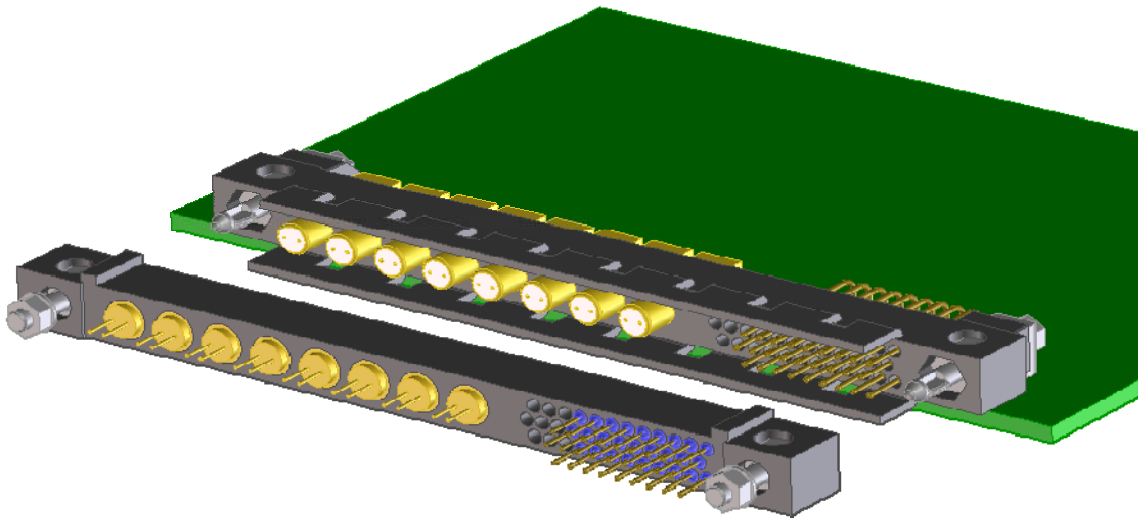

Figure 5-5 : Module interface with backplane connector