

# Protocol Validation System for On-Board Communications



## Project Status



13th SpaceWire Working Group Meeting, 14th-15th September 2009  
Noordwijk, Netherlands



## Presentation Contents

- PVS Project Rationale
- PVS Overall Objectives
- PVS Phase 1 Objectives (current contract)
- PVS Phase 1 Achievements
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## PVS Project Rationale



- Current **evolution of satellite on-board communications**, require the development & experimentation with new dedicated communication protocols and services (SpW, SOIS, etc.)
- **New generation of validation tools is required** to support advanced protocol development, test, integration & validation



- A **protocol validation tool** with more than 20 years of experience in the **telecommunication sector** & with hundreds of installations worldwide
- Has been widely used for testing various telecommunication networks (ISDN, V5, SS7, IN, GSM, UMTS, VoIP, custom)



The basic motivation is to provide an open, generic and fully integrated protocol validation system (PVS) for satellite on-board communications supporting multiple physical interfaces (SpW, MIL-STD-1553) and functionalities (emulation, validation, interworking testing).



## PVS Overall Objectives

- Provide an open, generic and integrated validation environment:
  - Support for multiple networks simultaneously (SpW, 1553, CAN)
  - Broad protocol support
  - Validated test suites library
  - Easily expandable to support new physical interfaces
  - Easily expandable to support new protocols/tests
  - Powerful and easy-to-use graphical tool chain (Protocol Editor, Analyser, test campaigner, protocol emulators, etc.)
  - Fast customization due to rapid prototyping



The PVS shall cover the needs of:

### ■ Rapid prototyping

- *R&D and feasibility studies (R&D section and academics)*
- *System analysis teams*

### ■ Functional testing

- *Device providers*
- *AIV teams*

### ■ Interoperability testing

- *Device providers*
- *AIT teams*

### ■ Stress testing

- *All users*

### ■ Protocol Analysis

- *All users*



## PVS usage scenarios

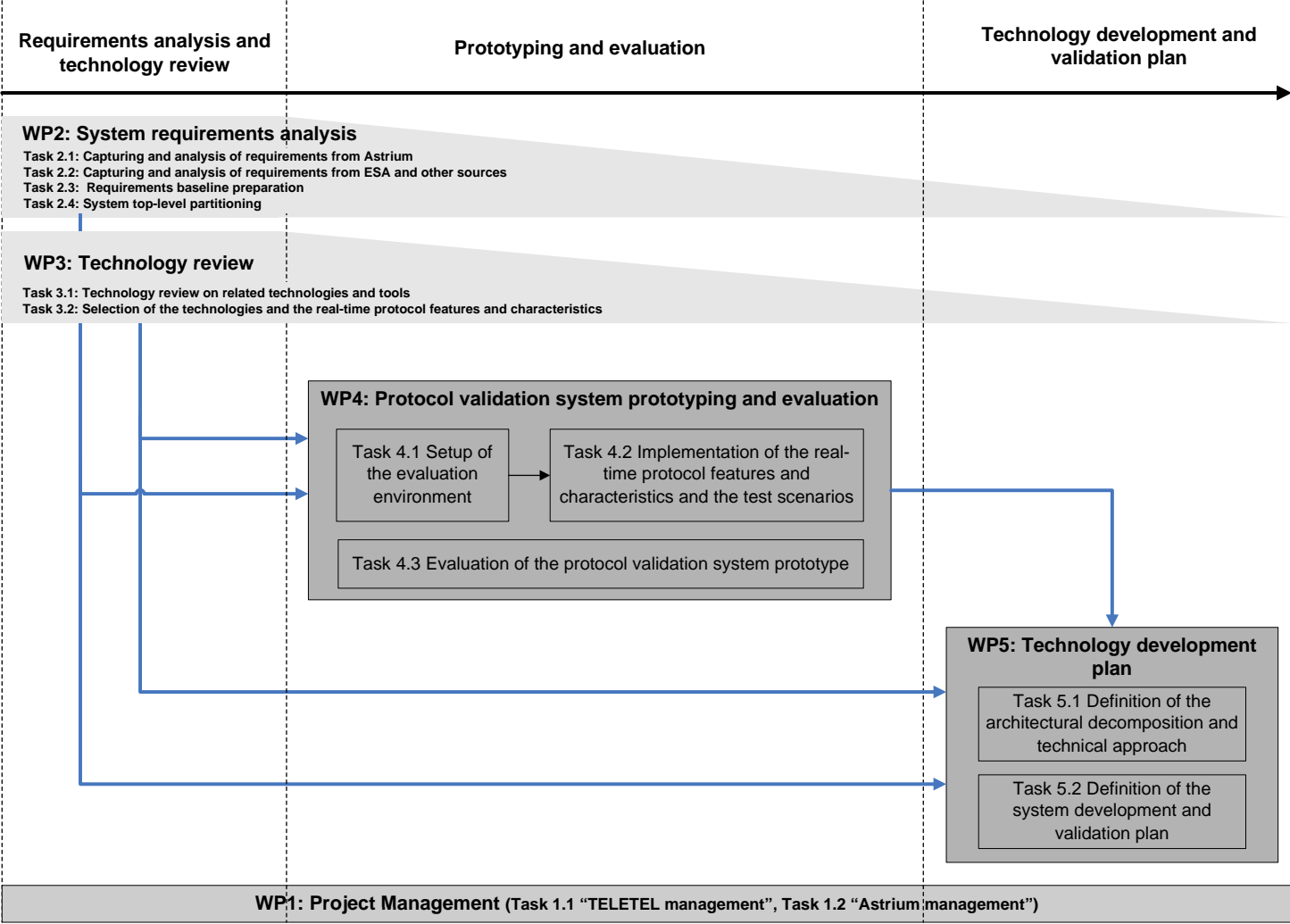
The PVS system shall support the following modes of operation:

- **PROTOCOL EMULATION:** experiments with various protocol features and assignment of values to the corresponding parameters.
- **PROTOCOL CONFORMANCE TESTING:** ensures that a device is operating in accordance with the applicable ECSS and CCSDS standards.
- **NETWORK MONITORING:** network monitoring, through direct physical traffic acquisition
- **FAULT-INJECTION:** injection of errors at various protocol layers to validate the response of the devices
- **TRAFFIC GENERATION:** generation of traffic for validation of higher layer protocols or bulk traffic injection at lower layers for performance testing and network dimensioning

## PVS Phase 1 Objectives

- Phase 1 (current contract):
  - Requirements capturing & analysis, based on requirements by ESA and Astrium, and PVS system top level partitioning
  - Technology review on related technologies, tools and protocols
  - Build a basic SpW development platform
  - Identification of SpW-RT features to validate
  - Realisation of the proof-of-concept prototype
  - Evaluation and demonstration of the PVS with SpW-RT and RMAP (or GAMMA)
  - Development plan definition for the full PVS

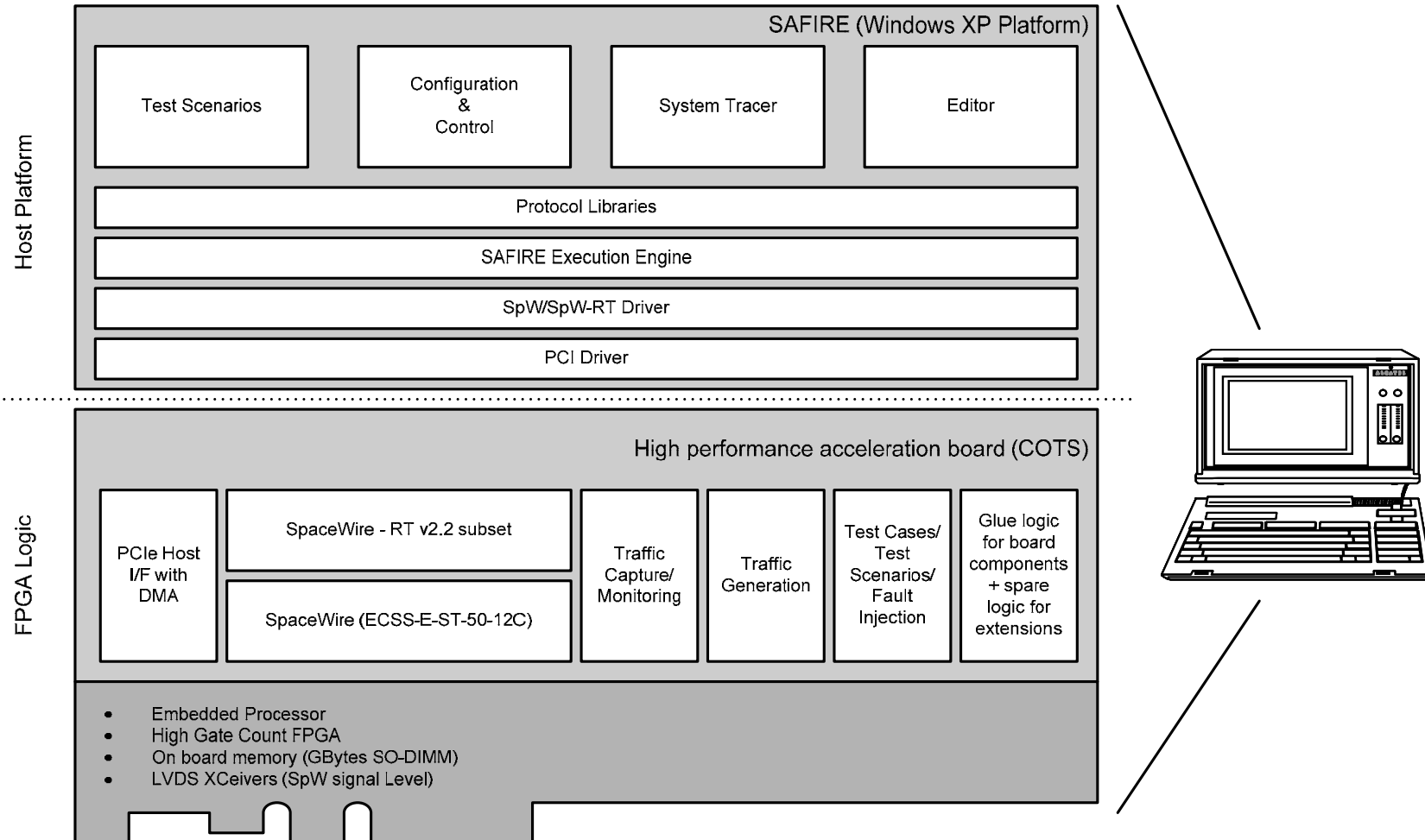
# Project Workplan





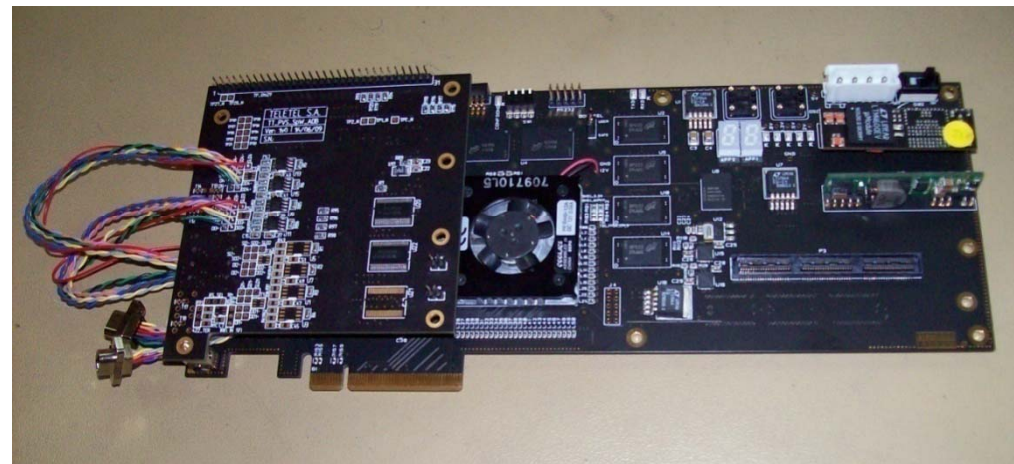
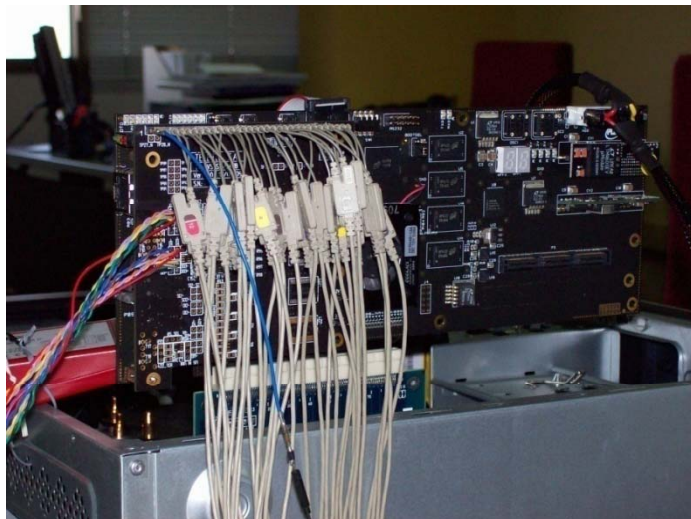
# PVS Phase 1 target system

Protocol Validation System for On-Board Communications



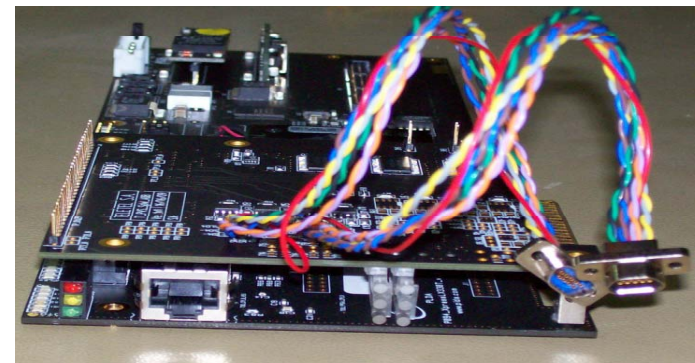
## PVS Phase 1 Achievements today

- Requirements for the envisaged PVS system defined
- Selection of technology components completed
- Selection & design of SpW-RT features to validate completed
- PVS SpW development platform integrated & verified
- Detailed Validation scenarios defined

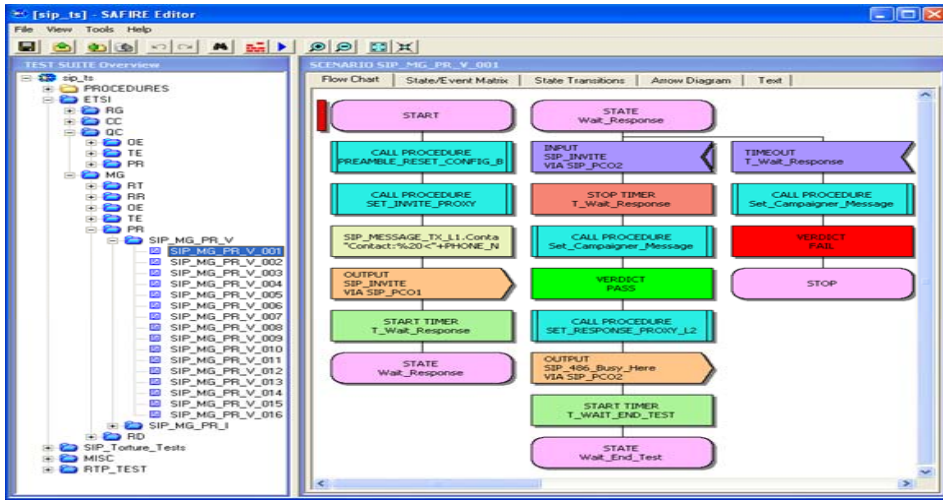


## PVS SpW Development Platform Main activities performed

- Selection and setup of a High capacity COTS FPGA development board with PCIe-DMA host I/F
- Design, production & verification of a 4-port SpW add-on-board with fine programmable transmission rates
- Integration of the DMA, PCIe IP cores
- Integration of the UoD SpW-b IP core
- Development of additional VHDL logic (DMA extensions, time-code logic, interrupt controller)
- Development of PC driver functions
- Development of configuration & control software
- Overall platform integration & tests
- Validation with SpW Conformance Tester successful (Athens 03 Sep 09)



# SAFIRE Graphical Environment (example)



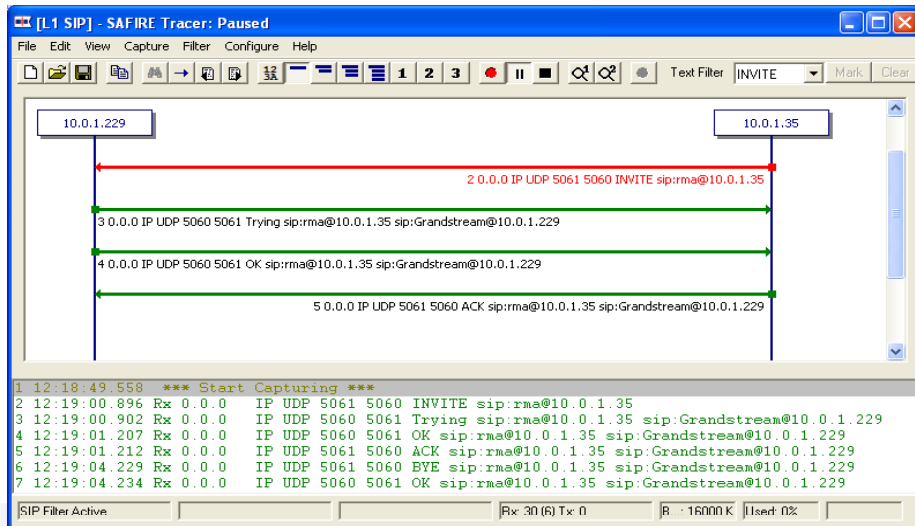
The screenshot shows the SAFIRE Campaigner interface. It displays a 'Log List' with the following entries:

- 13:50:49.866: Start campaign
- 13:50:49.866: Not using test suite configuration data
- 13:50:50.069: Load Act\_Master

Summary statistics: Current: 4, Total: 4, Pass: 4, Fail: 0, Inconc: 0, Stopped: 0. Below this is a 'Message from Testcase:' field and a 'Result List' table.

Test case	Group	Verdict	Reason	Start Time	Stop Time	Duration
Act_Master		PASS		13:50:50.069	13:50:50.069	10 ms
Act_Slave		PASS		13:50:50.388	13:50:50.399	10 ms
Deact_Slave		PASS		13:50:50.695	13:50:50.708	12 ms
Data_M2S		PASS		13:50:51.013	13:50:51.022	9 ms

Buttons at the bottom include Start, Repeat, Next, Stop, Soft Stop, Continue, and Animate.



The screenshot shows the SAFIRE Tracer interface displaying a 'Call Data Record' for a call. The record includes the following details:

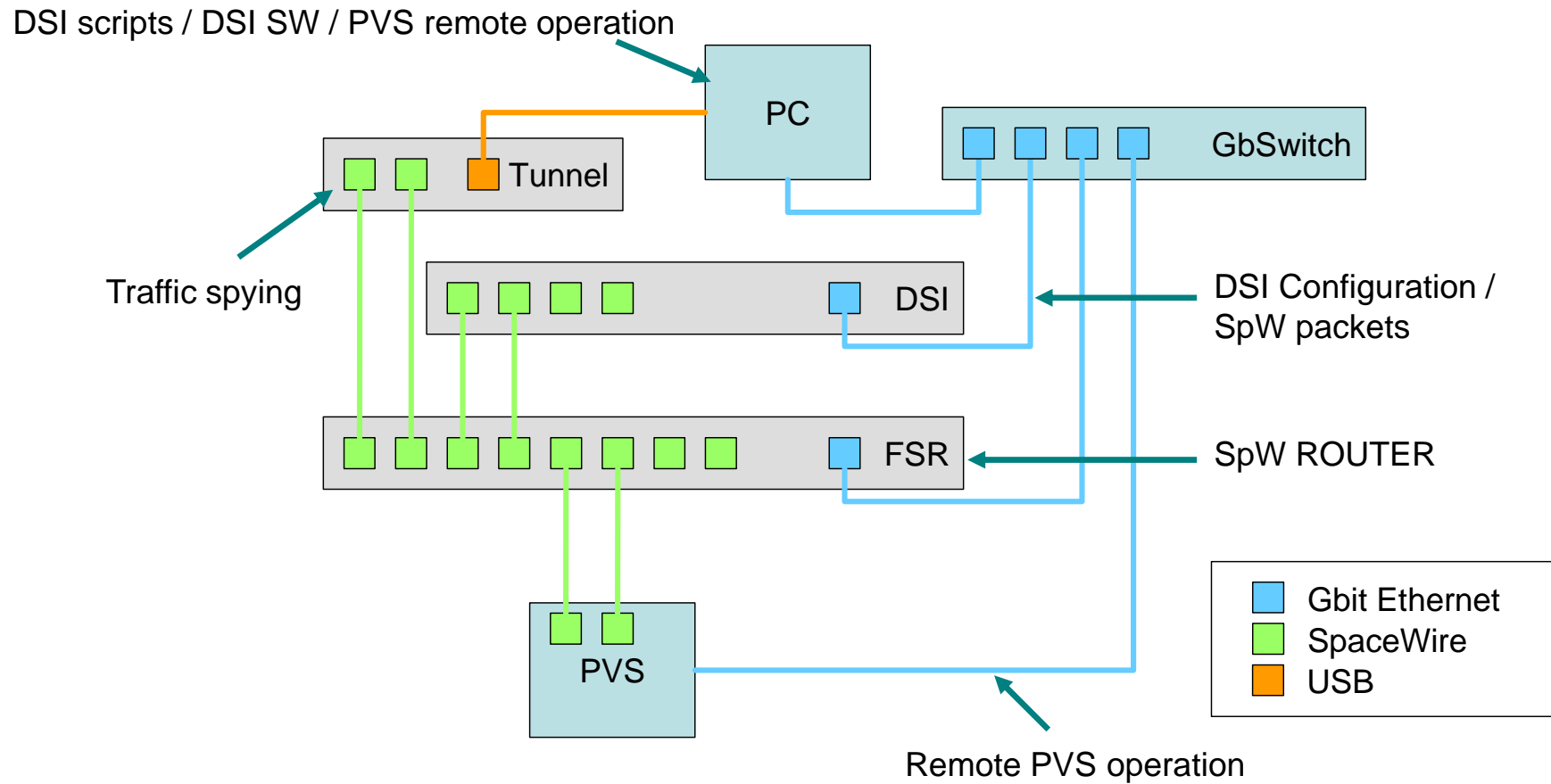
- Call ID: 2
- Calling: rma
- Called: rma
- Release Cause: Normal Call Clearing
- Time Info:
  - Start: 04:10:2007 12:19:00
  - Stop: 04:10:2007 12:19:00
  - Total: 3.338
  - Setup: 3.333
  - Post Dial Delay: 0.311
  - Connected: 0.005
  - Tear Down: 0.000
- Extra Info:
  - SIP:
    - Call ID: 176e3a8d-cdf9-1810-8209-0013e8803
    - From URI: rma@10.0.1.35
    - To URI: Grandstream@10.0.1.229
    - Media: audio
    - Payload Types: 'G.711 uLaw'
    - Silence Suppression: audio
  - Stream Info:
    - Calling to Called: 'G.711 uLaw'
    - Payload: '472E37313120754C6177'H
  - SWIQR:
    - Jitter: 992
    - Lost Packets: 4076
    - Burst Lost Packets: 0
    - Out Of Sequence Packets: 0
  - Called to Calling:
    - Payload: 'G.711 uLaw'
    - SWIQR:
      - Jitter: 994
      - Lost Packets: 213
      - Burst Lost Packets: 0
      - Out Of Sequence Packets: 0

At the bottom, it shows 'Filter Not Act...' and statistics: Rx: 1 Tx: 0, Buffer: 16000, Used: 0%.

## Selection of SpW-RT features to validate

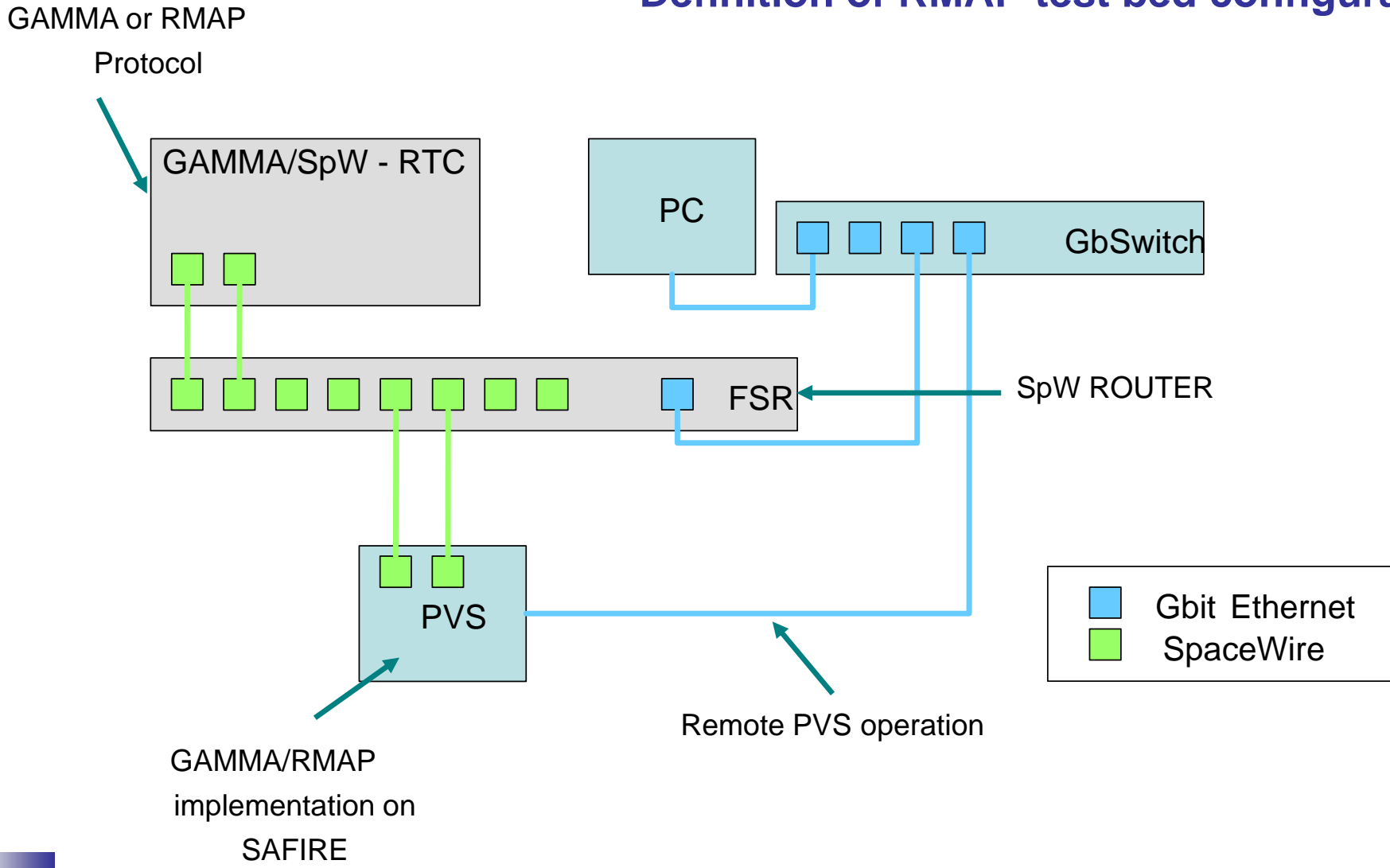
- ✓ Segmentation
- ✓ End to End flow Control
  - ✓ BFCT
  - ✓ BACK
  - ✗ SBFCT
  - ✓ SACK
- ✗ Retry
  - ✗ Automatic retransmission
  - ✓ ACK, ACK timeout
- ✓ Error Detection
  - ✓ Header/data CRC
  - ✓ Wrong destination address
  - ✓ Sequence Number
  - ✓ EEP
- ✗ Redundancy
  - ✗ Simultaneous retry
  - ✗ Autonomous/Managed switching
  - ✗ Managed switching
- ✓ Address Translation
- ✓ PDU Encapsulation
  - ✓ PDU
  - ✓ (S)ACK
  - ✓ BFCT
  - ✓ BACK
- ✓ Resource Reservation

# Definition of SpW-RT Validation test bed configuration





# Definition of RMAP test bed configuration



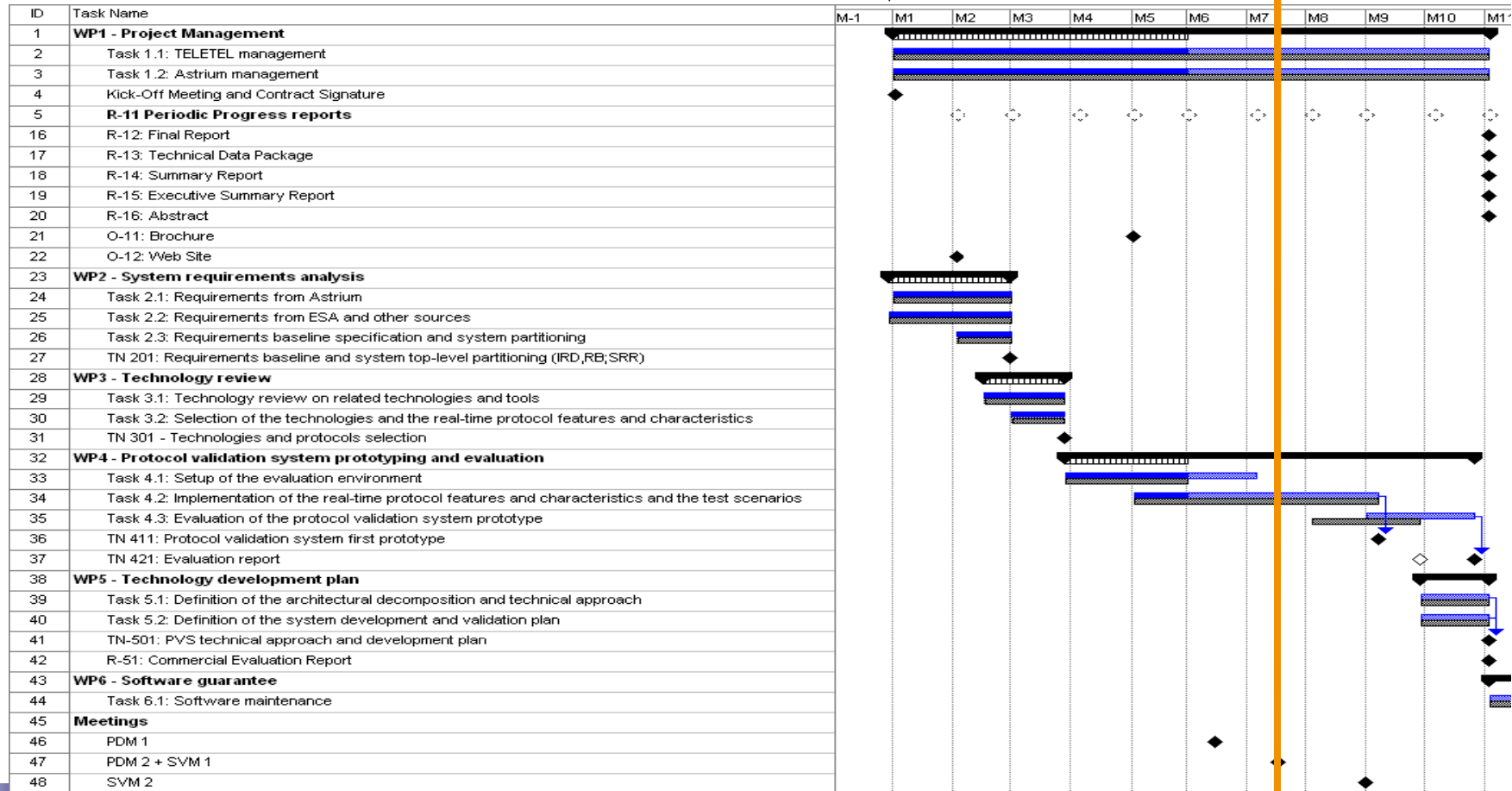
## Future activities

- Implementation of the SpW-RT terminal functionality in the FPGA (Oct-Nov)
- Implementation of the SpW-RT tests functionality in the FPGA (Oct-Nov)
- Implementation of PC test & control software (Oct)
- Integration of the PVS board with the SAFIRE environment (Oct)
- Implementation of RMAP test cases in SAFIRE (Oct)
- Verification and validation tests in Athens (Nov)
- Verification and validation tests in Toulouse (Dec)
- Definition of Phase 2 system features and development roadmap (Nov)



# Project Schedule

T0 – 16<sup>th</sup> February 2009



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[www.teletel.eu/esa\\_pvs\\_p1](http://www.teletel.eu/esa_pvs_p1)

login/passwd: same as for SpW WG web site



**teletel**