Galvanic Isolation of SpaceWire Links
Requirements, Design Options and Limitations

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Introduction

• The SpaceWire link Signal Level is based on LVDS as specified in ANSI/TIA/EIA-644
• LVDS provides in nominal operation a high impedance data connection between units
• There is currently no option for galvanic isolation specified in the SpaceWire standard
• This presentation will:
  – Review the need for galvanic isolation of data interfaces on board of spacecraft
  – Analyse the common potential shift tolerance of commonly used LVDS devices
  – Present and assess proposals to realise galvanic isolation for SpaceWire
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Need for Galvanic Isolation

- For some application galvanic isolation is desired to cope with the following effects:
  - Differences in the ground reference levels between units and interface circuits
  - Failure propagation due to over-voltage emission caused by power supply failures
  - Internal and external voltage building-up of spacecraft units when immersed in plasma
  - Electrostatic discharge resulting from spacecraft charging
  - Electrical transients induced by lightning in electrical circuits due to coupling of electromagnetic fields (e.g. for launcher applications)
  - Isolation of ground support equipment
  - Simplify the life of the system designer
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Possibility of Failure Propagation in Cross-strapped Systems due to Over-voltage Failures

Diagram by Sven Landström, TEC-EPC, ESA
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Common EMI Mitigation Techniques

• Adherence to the EMC space design rules should mitigate most of the described problems
  – Design of a controlled grounding scheme throughout the spacecraft
  – Control of local ground level after the power converter on PCBs and in units
  – Use of power converters with over voltage protection
  – Controlled discharge of spacecraft surfaces
  – Design of basic space vehicle structure as “Faraday cage”
  – Enclosure of electronic boxes
  – Shielding of cables
  – Over-shielding of cable bundles
Commercial LVDS are often quoted to be tolerant against “common mode voltage” drift of +/- 1V

This is only correct for the best case situation
Worse Case Common Potential Difference Tolerance

- Analysis based on worse case offset voltage specified in the LVDS driver data sheet
- Common mode voltage difference tolerance is reduced between +0.75V and -0.925V
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Fail Save Common Potential Difference Tolerance

• The fail save common potential difference tolerance has to consider the max/min failure voltage and the Absolute Maximum Ratings of the receiver
• For commonly used receiver circuits this is only +/- 0.3V beyond the maximum supply voltage
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LVDS Receiver with extended common-mode input voltage range

- The LVDS receiver SN55LVDS33-SP from Texas Instruments offers an extended common-mode input voltage range:
  - -4V to +5V Common-mode input voltage range
  - -5V to +6V Absolute Maximum Rating of input signal
  - 400-Mbps maximum signalling rate
  - 3.3V Supply voltage
  - Complies with TIA/EIA-644 (LVDS)
  - Receiver input ESD protection exceeds 15 kV Human-body Model and ±600 V Machine Model (MM) for electrostatic discharges with respect to ground
  - Inputs remain high-impedance on power down
  - Pin-compatible with other commonly used LVDS receivers like: AM26LS32, SN65LVDS32B, μA9637, SN65LVDS9637B
    - QML-V qualified, SMD 5962-07248
    - Military Temperature Range (–55°C to 125°C)
- LVDS receivers with extended common-mode input voltage range have the potential to solve the ground shift and fail safe problematic
- Possibly other manufacturers will follow the example of TI and offer similar devices
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Methods used for Galvanic Isolation

- Signal lines are often isolated through:
  - Transformer coupling
  - Capacitive coupling
  - Opto-couplers
- Transformer coupling is commonly used in space in Mil-bus
- Capacitive can support signal bandwidth is several GHz
- Opto-coupler performance can degrade over time and are often sensitive to radiation
- The applicability of a method depends not only on the signal bandwidth but also on the signal coding used
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Transformer Coupling for SpaceWire Links

- The following circuit has been proposed galvanic isolation of SpaceWire links
- It still needs to be verified with real SpaceWire signals

References:
- “A Step-by-Step Procedure to Integrate Transformer Coupled LVDS into SpaceWire Applications”, Larsen J., Components For Military and Space Electronics Conference & Exhibition, February 2009
SpaceWire Signals

- Data Strobe encoding:
  - Data are transmitted directly
  - Strobe signal changes whenever the Data signal is constant
- Receiver recovers the clock by XORing the Data and Strobe signals

\[
\begin{array}{ccccccccccc}
\text{Data} & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\
\hline \\
D & & & & & & & & & & \\
S & & & & & & & & & & \\
CLK & & & & & & & & & & \\
\end{array}
\]

- The D and S signals are not DC balanced
- The number of transitions and the signal spectrum strongly depends on the transmitted data.
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Worse Case Signal

- The Data Character 55Hex toggles every bit

<table>
<thead>
<tr>
<th>P</th>
<th>C</th>
<th>b0</th>
<th>b1</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>b5</th>
<th>b6</th>
<th>b7</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- C=0 marks a Data character and C=1 marks a Control character
- P is the parity bit which is set to produce an odd parity covers the previous character plus the following control bit

Data character  EOP  FCT

1st NULL + FCT + 10 Data characters + FCT + 7 Data Characters + EOP

- A sequence of 55Hex Data characters will toggle the D-line in every bit but will leave the S-line constant

Spice simulation was performed at 10Mbps with the sequence:
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Spice Simulation Differential Voltage Data Line
Spice Simulation Differential Voltage Strobe Line

Differential input threshold of LVDS receivers is +/- 100mV
Conclusion of the Spice Simulation

- The Spice simulation demonstrates the principle limitation of the proposed isolation of SpaceWire with transformers.
- The S-line can remain constant for certain legal sequences of data characters.
- Due to the elimination of the DC component in the signal the level of the S-line drops below the differential input threshold of the receiver.
- Noise will cause an unpredictable behaviour at the output of the LVDS receiver.
- The isolation of SpaceWire with transformers is therefore not recommended.

- Are there another solutions for the galvanic isolation of SpaceWire?
Capacitive Isolation using Bus-Holder Circuits

- The Bus-Holder circuit has been proposed by TI for the galvanic isolation of IEEE 1394-1995 serial bus
- A Bus-Holder is a weak latch circuit which holds last value on a tri-state bus
- This prevents the CMOS gate input from floating and keeps a valid logic input level without using pull-up or pull-down resistors
- The capacitors are used as galvanic isolation barrier
- Capacitor rating determines the maximum isolation performance
- This active isolation circuit requires an isolated power supply for the LVDS transceiver and two of the Bus-Holders

Reference:
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High Speed Digital Isolators

- There exist a number of integrated high speed digital isolator components from different vendors.
- The use integrated transformers or capacitors as isolation barrier.
- They cover a frequency range from DC to 150 Mbps.
- Multi-channel devices in all possible channel directionality configurations provide compact solutions.
- Additional jitter and skew has to be accounted when assessing the maximum link speed.

ADuM130x/ADuM140x Family from ANALOG Device

ISO72xx Family from Texas Instruments
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Digital Isolator Operation Principle

- The single-ended input signal is split into the differential signal components A and !A
- Each signal component is then differentiated into the transients B and !B
- Positive differential input to the comparator are used to set (C) or to reset (!C) the NOR-gate flip-flop
- Common mode changes at the primary side are efficiently filtered by the differential comparator
- The flip-flop is used to hold the output state value when input is unchanged
- A second low frequency channel is used to cover the frequencies 100kbps and to determine the correct state after power on
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Digital Isolator Performance

- Data rates up to 150Mbps
- Protection for very large potential differences:
  - Transient over voltage isolation 4000 V for 60 sec
  - Maximum working isolation voltage 560 V
- CMTI Common-mode transient immunity >25kV/µs
- Barrier capacitance input-to-output 1pF
- Isolation resistance >$10^{11}$ Ω
- Low channel to channel skew <1ns
Conclusions

- Currently the SpaceWire standard does not specify any option for galvanic link isolation.
- The earlier proposed galvanic isolation based on Pulse Transformers will fail if used with real SpaceWire traffic as signal.
- Galvanic isolation can still be achieved through the use of Bus-Holder circuits or digital isolators.
- Both solutions require a galvanic isolated power supply for the isolated LVDS transceiver.
- Due to the overall complexity their use is likely to be limited to use cases with a strong need for galvanic isolation.
- LVDS receivers with extended common-mode input voltage range should be considered as alternative for use cases with a smaller common mode shifts.
- The revised SpaceWire standard should specify requirements for an optional galvanic isolation of SpaceWire links.